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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373rct6

Contents

1 Introduction 9

2 Description 10

3 Functional overview 13

3.1 ARM® Cortex®-M4 core with embedded Flash and SRAM 13

3.2 Memory protection unit 13

3.3 Embedded Flash memory 14

3.4 Cyclic redundancy check (CRC) calculation unit 14

3.5 Embedded SRAM 14

3.6 Boot modes 14

3.7 Power management 15

3.7.1 Power supply schemes 15

3.7.2 Power supply supervisor 15

3.7.3 Voltage regulator 15

3.7.4 Low-power modes 16

3.8 Clocks and startup 16

3.9 General-purpose input/outputs (GPIOs) 16

3.10 Direct memory access (DMA) 17

3.11 Interrupts and events 17

3.11.1 Nested vectored interrupt controller (NVIC) 17

3.11.2 Extended interrupt/event controller (EXTI) 17

3.12 12-bit analog-to-digital converter (ADC) 18

3.12.1 Temperature sensor 18

3.12.2 Internal voltage reference (V_{REFINT}) 18

3.12.3 V_{BAT} battery voltage monitoring 18

3.13 16-bit sigma delta analog-to-digital converters (SDADC) 19

3.14 Digital-to-analog converter (DAC) 19

3.15 Fast comparators (COMP) 20

3.16 Touch sensing controller (TSC) 20

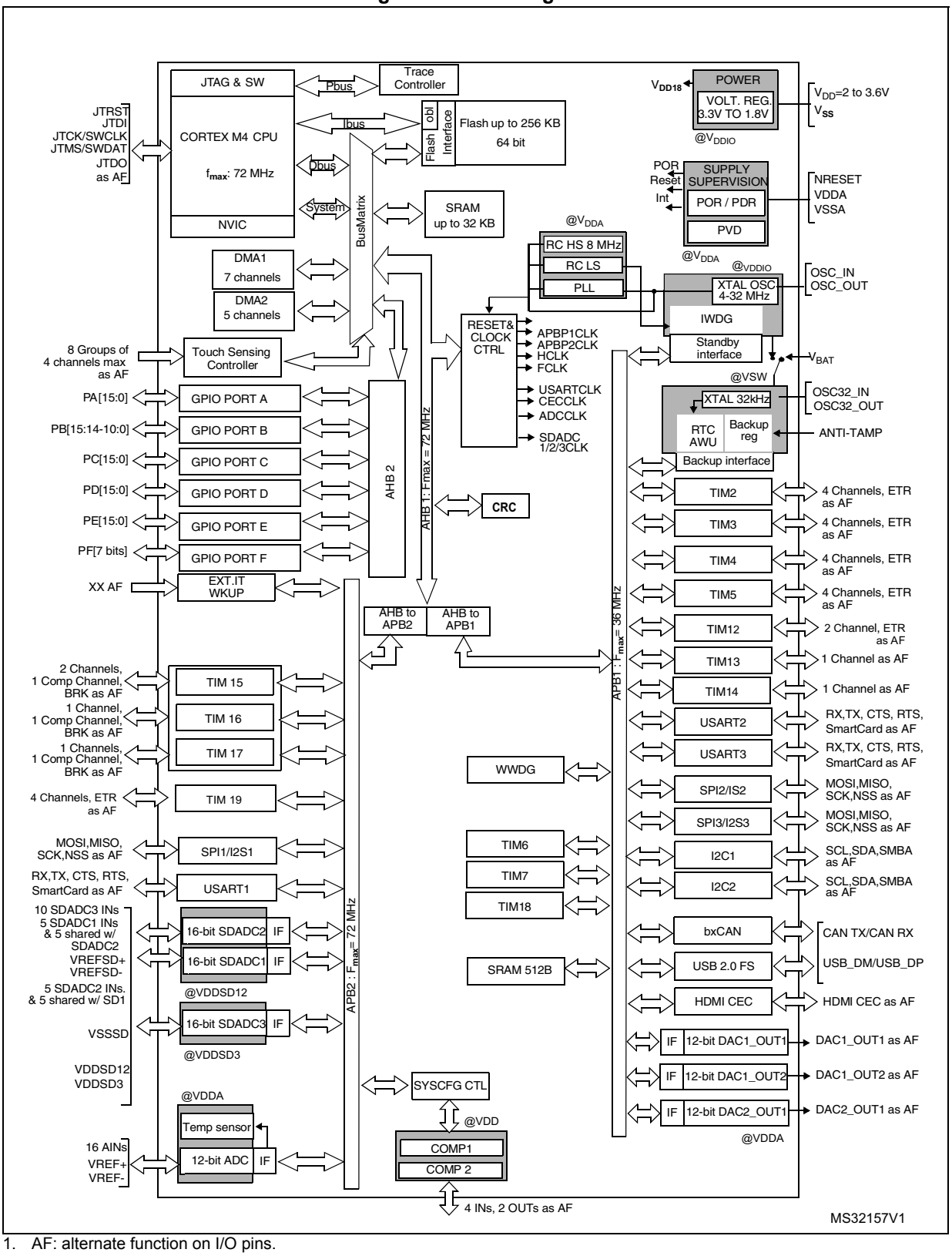
3.17 Timers and watchdogs 22

3.17.1 General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19) 23

List of figures

Figure 1. Block diagram . . . 12
Figure 2. STM32F373xx LQFP48 pinout . . . 29
Figure 3. STM32F373xx LQFP64 pinout . . . 30
Figure 4. STM32F373xx LQFP100 pinout . . . 31
Figure 5. STM32F373xx UFBGA100 ballout . . . 32
Figure 6. STM32F373xx memory map . . . 48
Figure 7. Pin loading conditions . . . 52
Figure 8. Pin input voltage . . . 52
Figure 9. Power supply scheme . . . 53
Figure 10. Current consumption measurement scheme . . . 54
Figure 11. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0]='00') . . . 65
Figure 12. High-speed external clock source AC timing diagram . . . 73
Figure 13. Low-speed external clock source AC timing diagram . . . 74
Figure 14. Typical application with an 8 MHz crystal . . . 75
Figure 15. Typical application with a 32.768 kHz crystal . . . 77
Figure 16. HSI oscillator accuracy characterization results . . . 78
Figure 17. TC and TTa I/O input characteristics - CMOS port . . . 85
Figure 18. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port . . . 86
Figure 19. I/O AC characteristics definition . . . 89
Figure 20. Recommended NRST pin protection . . . 90
Figure 21. I^2C bus AC waveforms and measurement circuit . . . 92
Figure 22. SPI timing diagram - slave mode and CPHA = 0 . . . 94
Figure 23. SPI timing diagram - slave mode and CPHA = 1(1) . . . 94
Figure 24. SPI timing diagram - master mode(1) . . . 95
Figure 25. I^2S slave timing diagram (Philips protocol)(1) . . . 97
Figure 26. I^2S master timing diagram (Philips protocol)(1) . . . 97
Figure 27. ADC accuracy characteristics . . . 100
Figure 28. Typical connection diagram using the ADC . . . 100
Figure 29. 12-bit buffered /non-buffered DAC . . . 102
Figure 30. Maximum V_{REFINT} scaler startup time from power down . . . 104
Figure 31. USB timings: definition of data signal rise and fall time . . . 108
Figure 32. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline . . . 115
Figure 33. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint . . . 116
Figure 34. UFBGA100 marking example (package top view) . . . 117
Figure 35. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline . . . 118
Figure 36. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint . . . 120
Figure 37. LQFP100 marking example (package top view) . . . 120
Figure 38. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline . . . 121
Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint . . . 123
Figure 40. LQFP64 marking example (package top view) . . . 123
Figure 41. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline . . . 124
Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint . . . 126
Figure 43. LQFP48 marking example (package top view) . . . 126

Figure 1. Block diagram



1. AF: alternate function on I/O pins.

3.7 Power management

3.7.1 Power supply schemes

- V_{DD}: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins, and can be 2.0 to 3.6 V.
- V_{DDA} = 2.0 to 3.6 V:
  - external analog power supplies for Reset blocks, RCs and PLL
  - supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to V_{DDA} is 2.4 V when the 12-bit ADC and DAC are used).
- V_{DDSD12} and V_{DDSD3} = 2.2 to 3.6 V: supply voltages for SDADC1/2 and SDADCD3 sigma delta ADCs. Independent from V_{DD}/V_{DDA}.
- V_{BAT}= 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers when V_{DD} is not present.

3.7.2 Power supply supervisor

- The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit. The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

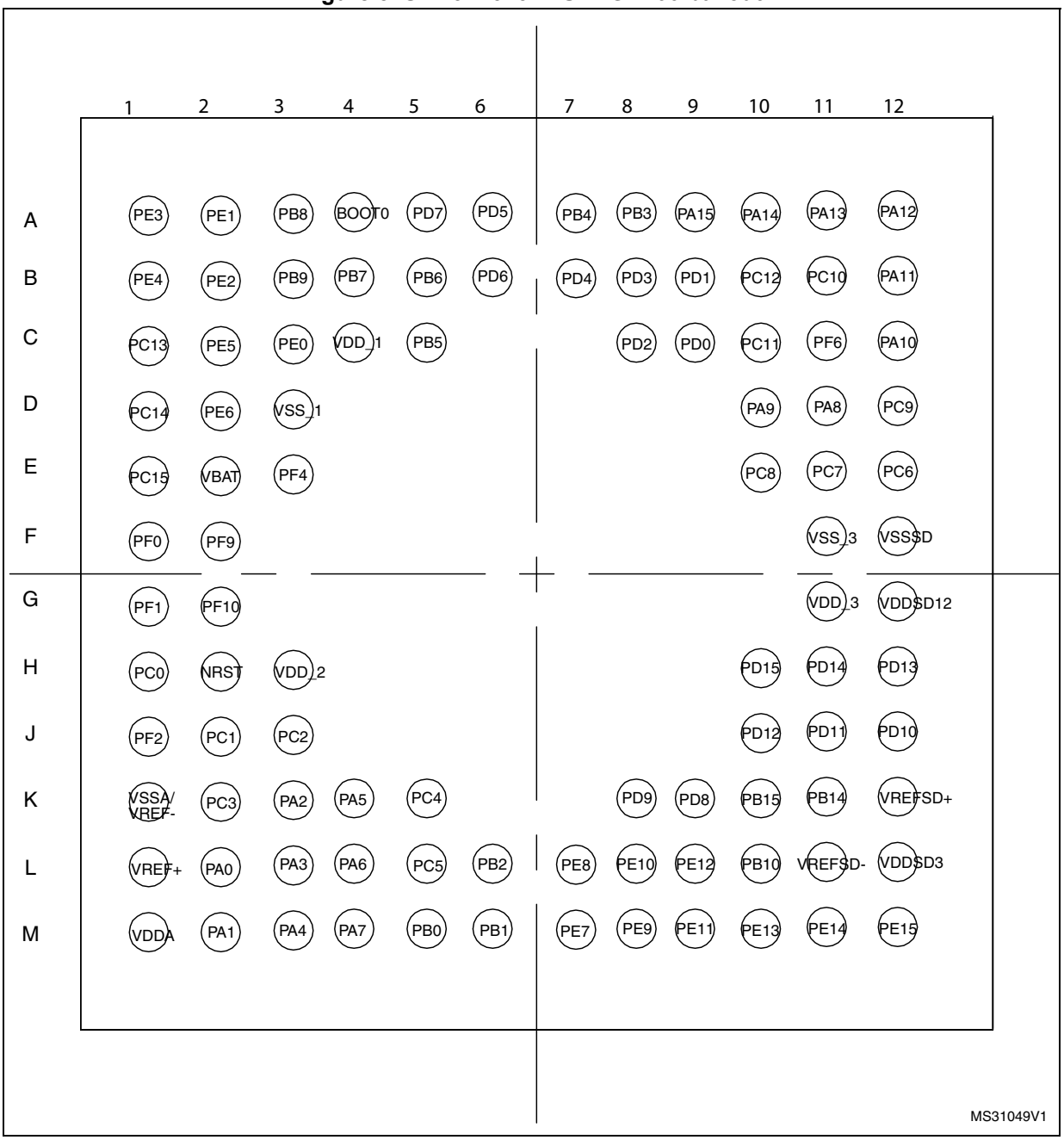
3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

Figure 5. STM32F373xx UFBGA100 ballout



1. The above figure shows the package top view.

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
25	K3	16	12	PA2	I/O	TTa	-	COMP2_OUT, SPI3_MISO/I2S3_MCK, USART2_TX, TIM2_CH3, TIM15_CH1, TIM5_CH3, TIM19_CH3, TSC_G1_IO3	ADC_IN2, COMP2_INM
26	L3	18	13	PA3	I/O	TTa	-	SPI3_MOSI/I2S3_SD, USART2_RX, TIM2_CH4, TIM15_CH2, TIM5_CH4, TIM19_CH4, TSC_G1_IO4	ADC_IN3, COMP2_INP
27	E3	-	-	PF4	I/O	FT	(2)	-	
28	H3	19	17	VDD_2	S	-	-	Digital power supply	
29	M3	20	14	PA4	I/O	TTa	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, TIM3_CH2, TIM12_CH1, TSC_G2_IO1,	ADC_IN4, DAC1_OUT1
30	K4	21	15	PA5	I/O	TTa	-	SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, TIM14_CH1, TIM12_CH2, TSC_G2_IO2	ADC_IN5, DAC1_OUT2
31	L4	22	16	PA6	I/O	TTa	-	SPI1_MISO/I2S1_MCK, COMP1_OUT, TIM3_CH1, TIM13_CH1, TIM16_CH1, TSC_G2_IO3	ADC_IN6, DAC2_OUT1,
32	M4	23	-	PA7	I/O	TTa	(2)	TSC_G2_IO4, TIM14_CH1, SPI1_MOSI/I2S1_SD, TIM17_CH1, TIM3_CH2, COMP2_OUT	ADC_IN7
33	K5	24	-	PC4	I/O	TTa	(2)	TIM13_CH1, TSC_G3_IO1, USART1_TX	ADC_IN14
34	L5	25	-	PC5	I/O	TTa	(2)	TSC_G3_IO2, USART1_RX	ADC_IN15
35	M5	26	18	PB0	I/O	TTa	-	SPI1_MOSI/I2S1_SD, TIM3_CH3, TSC_G3_IO3, TIM3_CH2	ADC_IN8, SDADC1_AIN6P
36	M6	27	19	PB1	I/O	TTa	-	TIM3_CH4, TSC_G3_IO4	ADC_IN9, SDADC1_AIN5P, SDADC1_AIN6M
37	L6	28	20	PB2	I/O	TC	(3)	-	SDADC1_AIN4P, SDADC2_AIN6P

Table 12. Alternate functions for port PA (continued)

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA13	SWDIO -JTMS	TIM16_ CH1N	TIM5_ CH4	TSC_ G4_IO3	-	IR-OUT	SPI1_MISO /I2S1_MCK	USART3_CTS	-	-	TIM4_ CH3	-	-	EVENT OUT
PA14	SWCLK -JTCK	-	-	TSC_ G4_IO4	I2C1_ SDA	-	-	-	-	-	TIM12 _CH1	-	-	EVENT OUT
PA15	JTDI	TIM2_ CH1_ETR	-	TSC_ SYNC	I2C1_ SCL	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	-	-	-	TIM12 _CH2	-	-	EVENT OUT

Table 16. Alternate functions for port PE

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0	-	EVENTOUT	TIM4_ETR	-	-	-	-	USART1_TX
PE1	-	EVENTOUT	-	-	-	-	-	USART1_RX
PE2	TRACECLK	EVENTOUT	-	TSC_G7_IO1	-	-	-	-
PE3	TRACED0	EVENTOUT	-	TSC_G7_IO2	-	-	-	-
PE4	TRACED1	EVENTOUT	-	TSC_G7_IO3	-	-	-	-
PE5	TRACED2	EVENTOUT	-	TSC_G7_IO4	-	-	-	-
PE6	TRACED3	EVENTOUT	-	-	-	-	-	-
PE7	-	EVENTOUT	-	-	-	-	-	-
PE8	-	EVENTOUT	-	-	-	-	-	-
PE9	-	EVENTOUT	-	-	-	-	-	-
PE10	-	EVENTOUT	-	-	-	-	-	-
PE11	-	EVENTOUT	-	-	-	-	-	-
PE12	-	EVENTOUT	-	-	-	-	-	-
PE13	-	EVENTOUT	-	-	-	-	-	-
PE14	-	EVENTOUT	-	-	-	-	-	-
PE15	-	EVENTOUT	-	-	-	-	-	USART3_RX

Table 17. Alternate functions for port PF

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	-	-	I2C2_SDA	-	-	-
PF1	-	-	-	-	I2C2_SCL	-	-	-
PF2	-	EVENTOUT	-	-	I2C2_SMBA	-	-	-
PF4	-	EVENTOUT	-	-	-	-	-	-
PF6	-	EVENTOUT	TIM4_CH4	-	I2C2_SCL	SPI1_MOSI/I2S1_SD	-	USART3_RTS
PF7	-	EVENTOUT	-	-	I2C2_SDA	-	-	USART2_CK
PF9	-	EVENTOUT	TIM14_CH1	-	-	-	-	-
PF10	-	EVENTOUT	-	-	-	-	-	-

5 Memory mapping

Figure 6. STM32F373xx memory map

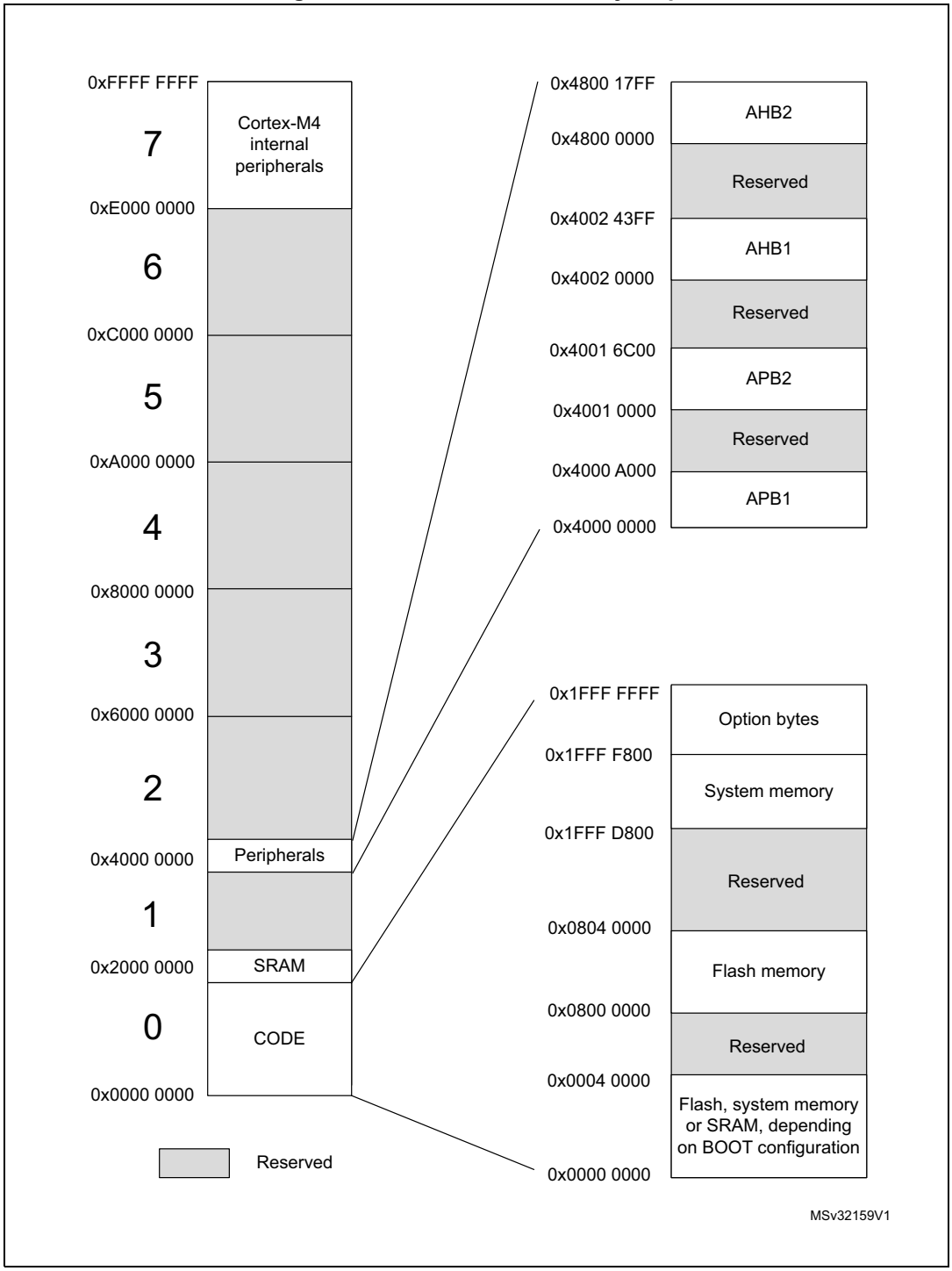


Table 18. STM32F373xx peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size	Peripheral
APB2	0x4001 6800 - 0x4001 6BFF	1 KB	SDADC3
	0x4001 6400 - 0x4001 67FF	1 KB	SDADC2
	0x4001 6000 - 0x4001 63FF	1 KB	SDADC1
	0x4001 5C00 - 0x4001 5FFF	1 KB	TIM19
	0x4001 4C00 - 0x4001 5BFF	4 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2800 - 0x4001 2FFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
-	0x4000 4000 - 0x4000 FFFF	24 KB	Reserved
APB1	0x4000 9C00 – 0x4000 9FFF	1 KB	TIM18
	0x4000 9800 - 0x4000 9BFF	1 KB	DAC2
	0x4000 7C00 - 0x4000 97FF	8 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC1
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	2 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN
	0x4000 6000 - 0x4000 63FF	1 KB	USB packet SRAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB FS

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{APB1} = f_{AHB}/2$, $f_{APB2} = f_{AHB}$
- When f_{HCLK} > 8 MHz PLL is ON and PLL inputs is equal to HSI/2 = 4 MHz (if internal clock is used) or HSE = 8 MHz (if HSE bypass mode is used)

The parameters given in *Table 28* to *Table 34* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V(1)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	HSE bypass, PLL on	72 MHz	63.1	70.7	71.5	73.4	29.2	31.1	31.7	34.2	mA
			64 MHz	56.3	63.3	64.1	64.9	26.1	27.8	28.4	30.4	
			48 MHz	42.5	48.5	48.0	50.1	19.9	22.6	21.9	23.1	
			32 MHz	28.8	31.4	32.2	34.3	13.1	16.1	14.9	16.2	
			24 MHz	21.9	24.4	24.4	25.8	10.1	10.9	11.9	12.4	
		HSE bypass, PLL off	8 MHz	7.3	8.0	9.3	9.3	3.7	4.1	4.4	5.0	
			1 MHz	1.1	1.5	1.8	2.3	0.8	1.1	1.4	1.9	
		HSI clock, PLL on	64 MHz	51.7	57.7	58.0	60.4	25.8	27.6	28.1	30.1	
			48 MHz	38.6	45.9	43.5	46.9	19.8	21.9	21.7	22.8	
			32 MHz	26.4	31.1	29.7	31.9	13.1	15.7	14.8	16.2	
			24 MHz	20.3	22.6	22.6	23.7	6.9	7.5	8.1	8.8	
		HSI clock, PLL off	8 MHz	7.0	7.6	8.8	8.8	3.7	4.1	4.4	5.0	

Table 36. Peripheral current consumption (continued)

Peripheral	Typical consumption[1]	Unit
APB1 peripherals		µA/MHz
APB1-Bridge[3]	6.9	
TIM2	47.9	
TIM3	36.8	
TIM4	36.9	
TIM5	45.5	
TIM6	8.4	
TIM7	8.2	
TIM12	21.3	
TIM13	14.2	
TIM14	14.4	
TIM18	10.1	
WWDG	4.7	
SPI2	24.3	
SPI3	25.3	
USART2	45.3	
USART3	43.1	
I2C1	14.0	
I2C2	13.9	
USB	27.9	
CAN	38.1	
DAC2	7.7	
PWR	5.4	
DAC1	14.8	
CEC	5.4	

1. When peripherals are enabled, power consumption of the analog part of peripherals such as ADC, DACs, Comparators, etc. is not included. Refer to those peripherals characteristics in the subsequent sections.
2. The BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx Bridge is automatically active when at least one peripheral is ON on the same Bus.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 37* are measured from the wakeup event trigger to the first instruction executed by the CPU. The clock source used to wake up the device depends from the current operating mode:

- Stop or sleep mode: the wakeup event is WFE.
- The WKUP1 (PA0) pin is used to wakeup from standby, stop and sleep modes.

Table 51. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	-0	NA	mA
	Injected current on PC0 pin	-0	+5	
	Injected current on TC type I/O pins on VDDSD12 power domain: PB2, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB10 with induced leakage current on other pins from this group less than -50 µA	-5	+5	
	Injected current on TC type I/O pins on VDDSD3 power domain: PB14, PB15, PD8, PD9, PD10, PD12, PD13, PD14, PD15 with induced leakage current on other pins from this group less than -50 µA	-5	+5	
	Injected current on TTa type pins: PA4, PA5, PA6 with induced leakage current on adjacent pins less than -10 µA	-5	+5	
	Injected current on any other FT and FTf pins	-5	NA	
	Injected current on any other pins	-5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.20 Temperature sensor characteristics

Table 65. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ± 5 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C ± 5 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

Table 66. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(2)(1)	ADC sampling time when reading the temperature	17.1	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.21 V_{BAT} monitoring characteristics

Table 67. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.22 Timer characteristics

The parameters given in *Table 68* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
V_{REFSD-}	Negative ref. voltage	-	-	V_{SSA}	-	V	-
I_{DDSDx}	Supply current (V_{DDSDx} = 3.3 V)	Normal mode (f_{ADC} = 6 MHz)	-	800	1200	µA	-
		Slow mode (f_{ADC} = 1.5 MHz)	-	-	600		-
		Standby	-	-	200		-
		Power down	-	-	2.5		-
		SD_ADC off	-	-	1		-
V_{AIN}	Common input voltage range	Single ended mode (zero reference)	V_{REFSD-}	-	V_{REFSD+} /gain	V	Voltage on AINP or AINN pin
		Single ended offset mode	V_{REFSD-}	-	V_{REFSD+}/ (gain*2)		
		Differential mode	V_{SSA}	-	V_{DDSDx}		
V_{DIFF}	Differential input voltage	Differential mode only	-V_{REFSD+}/ (gain*2)	-	V_{REFSD+}/ (gain*2)	-	Differential voltage between AINP and AINN
f_S	Sampling rate	Slow mode (f_{ADC} = 1.5 MHz)	-	4.166	-	kHz	f_{ADC}/360
		Slow mode one channel only (f_{ADC} = 1.5 MHz)	-	12.5	-		f_{ADC}/120
		Normal mode multiplexed channel (f_{ADC} = 6 MHz)	-	16.66	-		f_{ADC}/360
		Normal mode one channel only, FAST= 1 (f_{ADC} = 6 MHz)	-	50	-		f_{ADC}/120
t_{CONV}	Conversion time	-	-	1/fs	-	s	-
Rain	Analog input impedance	One channel, gain = 0.5, f_{ADC} = 1.5 MHz	-	540	-	kΩ	see reference manual for detailed description
		One channel, gain = 0.5, f_{ADC} = 6 MHz	-	135	-		
		One channel, gain = 8, f_{ADC} = 6 MHz	-	47	-		
t_{CALIB}	Calibration time	f_{ADC} = 6 MHz, one offset calibration	-	5120	-	µs	30720/f_{ADC}
t_{STAB}	Stabilization time	From power down f_{ADC} = 6 MHz	-	100	-	µs	600/f_{ADC}, 75/f_{ADC} if SLOWCK = 1
$t_{STANDBY}$	Wakeup from standby time	f_{ADC} = 6 MHz	-	50	-	µs	300/f_{ADC}
		f_{ADC} = 1.5 MHz	-	50	-		75/f_{ADC} if SLOWCK = 1

7.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Q_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Q_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = S (V_{OL} × I_{OL}) + S((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 81. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient UFBGA100 - 7 x 7 mm	59	

7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

Using the values obtained in *Table 81* T_{Jmax} is calculated as follows:

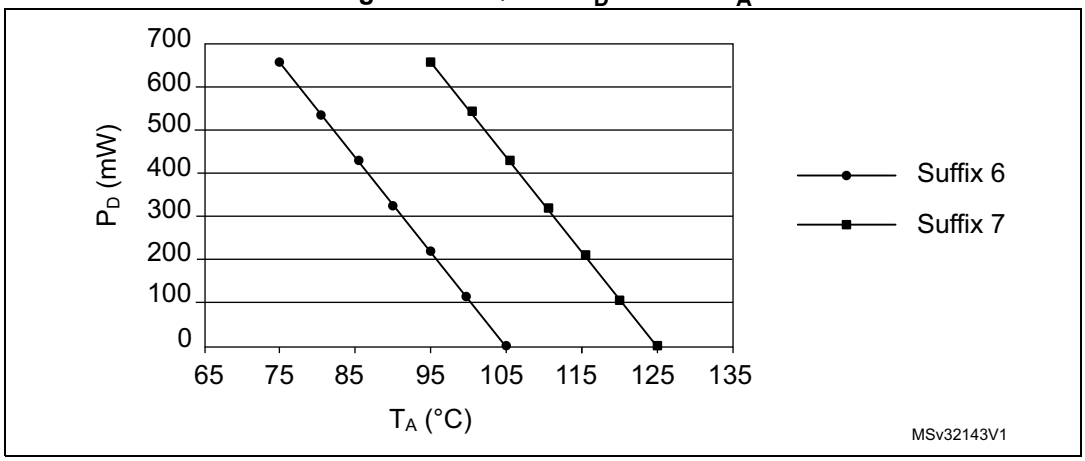
– For LQFP100, 46°C/W

T_{Jmax} = 115 °C + (46°C/W × 98.8 mW) = 115 °C + 4.54 °C = 119.5 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*).

Figure 44. LQFP64 P_D max vs. T_A



8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 82. Ordering information scheme

Example: STM32 F 373 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

373 = STM32F373xx

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Code size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel

Table 83. Document revision history (continued)

Date	Revision	Changes
19-Sep-2013	4	Replaced “Cortex-M4F” with “Cortex-M4” throughout the document. Removed part number STM32F372xx. Added “1.25 DMIPS/MHz (Dhrystone 2.1)” in *Features*. Updated *Introduction*. Added reference to the STMTouch touch sensing firmware library in *Section 3.16: Touch sensing controller (TSC)*. Added “All I2S interfaces can operate in half-duplex mode only.” in *Section 3.21: Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)*. Added row “I2S full-duplex mode” to *Table 9: STM32F373xx SPI/I2S implementation*. Modified introduction of *I2C interface characteristics*. Added alternate function RTC_REFIN and removed additional function RTC_REF_CLK_IN to pins PA1 and PB15. Replaced alternate function JNTRST with NJTRST for pin PB4. In *Table 12: Alternate functions for port PA*: replaced alternate function JTMS-SWDIO with SWDIO-JTMS for pin PA13, and JTCK-SWCLK with SWCLK-JTCK for pin PA14. Added rows V_{REF+} and V_{REFSD+} to *Table 22: General operating conditions*. Replaced "$f_{APB1} = f_{AHB/2}$" with "$f_{APB1} = f_{AHB}$" for “When the peripherals are enabled...” in *Typical current consumption*. Added COMP in *Table 36: Peripheral current consumption* Added conditions for f_{HSE_ext} in *Table 38: High-speed external user clock characteristics*. Added Min and Max values for ACC_{HSI} in *Table 42: HSI oscillator characteristics*. Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in *Table 49: ESD absolute maximum ratings*. Removed pins PB0 and PB1 in description of I_{INJ} in *Table 51: I/O current injection susceptibility*. Updated *Table 56: I2C characteristics*. Replaced all occurrences of “gain/2” with “gain*2” in *Table 74: SDADC characteristics*. Corrected typo in *Figure 19: I/O AC characteristics definition*. Replaced *Figure 21: I2C bus AC waveforms and measurement circuit*.. Added $I_{DDA(ADC)}$ and footnote 1 in *Table 60: ADC characteristics*