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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373rct6tr

2 Description

The STM32F373xx family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an Embedded Trace Macrocell™ (ETM). The family incorporates high-speed embedded memories (up to 256 Kbyte of Flash memory, up to 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F373xx devices offer one fast 12-bit ADC (1 Msps), three 16-bit Sigma delta ADCs, two comparators, two DACs (DAC1 with 2 channels and DAC2 with 1 channel), a low-power RTC, 9 general-purpose 16-bit timers, two general-purpose 32-bit timers, three basic timers.

They also feature standard and advanced communication interfaces: two I2Cs, three SPIs, all with muxed I2Ss, three USARTs, CAN and USB.

The STM32F373xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F373xx family offers devices in five packages ranging from 48 pins to 100 pins. The set of included peripherals changes with the device chosen.

Do not reconfigure GPIO pins which are not present on 48 and 64 pin packages to the analog mode. Additional current consumption in the range of tens of μA per pin can be observed if V_{DDA} is higher than V_{DDIO} .

3.10 Direct memory access (DMA)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The two DMAs can be used with the main peripherals: SPIs, I2Cs, USARTs, DACs, ADC, SDADCs, general-purpose timers.

3.11 Interrupts and events

3.11.1 Nested vectored interrupt controller (NVIC)

The STM32F373xx devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.11.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 84 GPIOs can be connected to the 16 external interrupt lines.

Table 7. STM32F373xx I²C implementation (continued)

I ² C features ⁽¹⁾	I2C1	I2C2
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F373xx embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smartcard mode (ISO/IEC 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to [Table 8](#) for the features of USART1, USART2 and USART3.

Table 8. STM32F373xx USART implementation

USART modes/features ⁽¹⁾	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X	X	X
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	X
LIN mode	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X
Receiver timeout interrupt	X	X	X
Modbus communication	X	X	X
Auto baud rate detection	X	X	X
Driver Enable	X	X	X

1. X = supported.



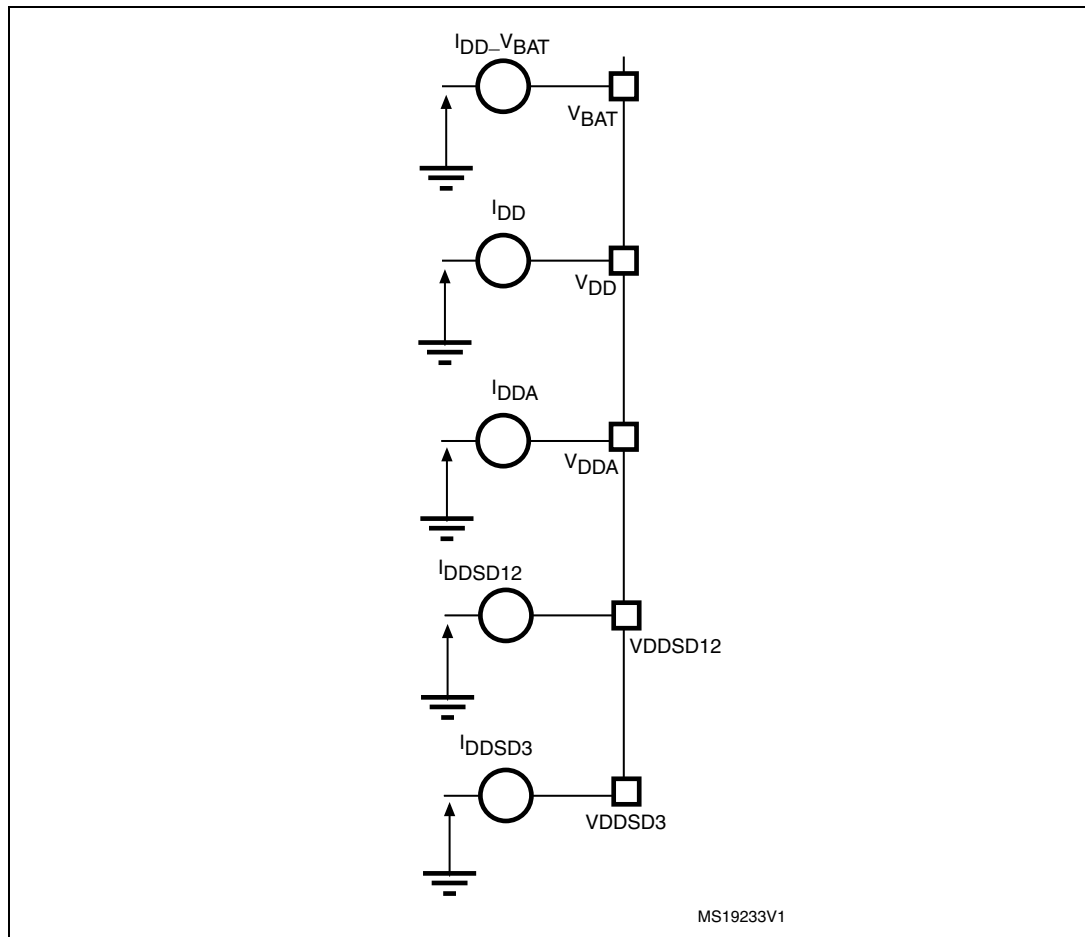
Table 14. Alternate functions for port PC

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	EVENTOUT	TIM5_CH1_ETR	-	-	-	-	-
PC1	-	EVENTOUT	TIM5_CH2	-	-	-	-	-
PC2	-	EVENTOUT	TIM5_CH3	-	-	SPI2_MISO/I2S2_MCK	-	-
PC3	-	EVENTOUT	TIM5_CH4	-	-	SPI2_MOSI/I2S2_SD	-	-
PC4	-	EVENTOUT	TIM13_CH1	TSC_G3_IO1	-	-	-	USART1_TX
PC5	-	EVENTOUT	-	TSC_G3_IO2	-	-	-	USART1_RX
PC6	-	EVENTOUT	TIM3_CH1	-	-	SPI1_NSS/I2S1_WS	-	-
PC7	-	EVENTOUT	TIM3_CH2	-	-	SPI1_SCK/I2S1_CK	-	-
PC8	-	EVENTOUT	TIM3_CH3	-	-	SPI1_MISO/I2S1_MCK	-	-
PC9	-	EVENTOUT	TIM3_CH4	-	-	SPI1_MOSI/I2S1_SD	-	-
PC10	-	EVENTOUT	TIM19_CH1	-	-	-	SPI3_SCK/I2S3_CK	USART3_TX
PC11	-	EVENTOUT	TIM19_CH2	-	-	-	SPI3_MISO/I2S3_MCK	USART3_RX
PC12	-	EVENTOUT	TIM19_CH3	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

Caution: Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



The following relationship must be respected between V_{REFSD+} and V_{DDSD12} , V_{DDSD3} :
 V_{REFSD+} must be lower than V_{DDSD3} .
 Depending on the SDADCx operation mode, there can be more constraints between V_{REFSD+} , V_{DDSD12} and V_{DDSD3} which are described in reference manual RM0313.

Table 20. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x and VDDSDx power lines (source) ⁽¹⁾	160	mA
ΣI_{VSS}	Total current out of sum of all VSS_x and VSSSD ground lines (sink) ⁽¹⁾	-160	
$I_{VDD(PIN)}$	Maximum current into each VDD_x or VDDSDx power pin (source) ⁽¹⁾	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x or VSSSD ground pin (sink) ⁽¹⁾	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins ⁽²⁾	80	
	Total output current sourced by sum of all IOs and control pins ⁽²⁾	-80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins ⁽³⁾	-5/+0	
	Injected current on TC and RST pin ⁽⁴⁾	± 5	
	Injected current on TTa pins ⁽⁵⁾	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	± 25	

- VDDSD12 is the external power supply for the PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to V_{SS}). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to V_{SS}). V_{DD} (VDD_x) is the external power supply for all remaining I/O pins (the I/O pin ground is internally connected to V_{SS}).
- This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
- Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
- A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 19: Voltage characteristics](#) for the maximum allowed input voltage values.
- A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to [Table 19: Voltage characteristics](#) for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note ⁽²⁾ below [Table 62](#).
- When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 24](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 22](#).

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}^{(1)}$	Power on/power down reset threshold	Falling edge	1.80 ⁽²⁾	1.88	1.96	V
		Rising edge	1.84	1.92	2.00	V
$V_{PDRhyst}^{(3)}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}^{(3)}$	POR reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} , V_{DDA} and V_{DDSD12} (if kept enabled in the option bytes). The POR detector monitors only V_{DD} .
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design.

Table 25. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.10	2.18	2.26	V
		Falling edge	2.00	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3.00	V
		Falling edge	2.66	2.78	2.90	V
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$I_{DD(PVD)}^{(2)}$	PVD current consumption	-	-	0.15	0.26	μ A

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 10: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{APB1} = f_{AHB}/2$, $f_{APB2} = f_{AHB}$
- When $f_{HCLK} > 8$ MHz PLL is ON and PLL inputs is equal to $HSI/2 = 4$ MHz (if internal clock is used) or HSE = 8 MHz (if HSE bypass mode is used)

The parameters given in [Table 28](#) to [Table 34](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 22](#).

Table 28. Typical and maximum current consumption from V_{DD} supply at $V_{DD} = 3.6$ V⁽¹⁾

Symbol	Parameter	Conditions	f _{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T _A ⁽²⁾			Typ	Max @ T _A ⁽²⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DD}	Supply current in Run mode, code executing from Flash	HSE bypass, PLL on	72 MHz	63.1	70.7	71.5	73.4	29.2	31.1	31.7	34.2	mA
			64 MHz	56.3	63.3	64.1	64.9	26.1	27.8	28.4	30.4	
			48 MHz	42.5	48.5	48.0	50.1	19.9	22.6	21.9	23.1	
			32 MHz	28.8	31.4	32.2	34.3	13.1	16.1	14.9	16.2	
			24 MHz	21.9	24.4	24.4	25.8	10.1	10.9	11.9	12.4	
		HSE bypass, PLL off	8 MHz	7.3	8.0	9.3	9.3	3.7	4.1	4.4	5.0	
			1 MHz	1.1	1.5	1.8	2.3	0.8	1.1	1.4	1.9	
		HSI clock, PLL on	64 MHz	51.7	57.7	58.0	60.4	25.8	27.6	28.1	30.1	
			48 MHz	38.6	45.9	43.5	46.9	19.8	21.9	21.7	22.8	
			32 MHz	26.4	31.1	29.7	31.9	13.1	15.7	14.8	16.2	
			24 MHz	20.3	22.6	22.6	23.7	6.9	7.5	8.1	8.8	
		HSI clock, PLL off	8 MHz	7.0	7.6	8.8	8.8	3.7	4.1	4.4	5.0	

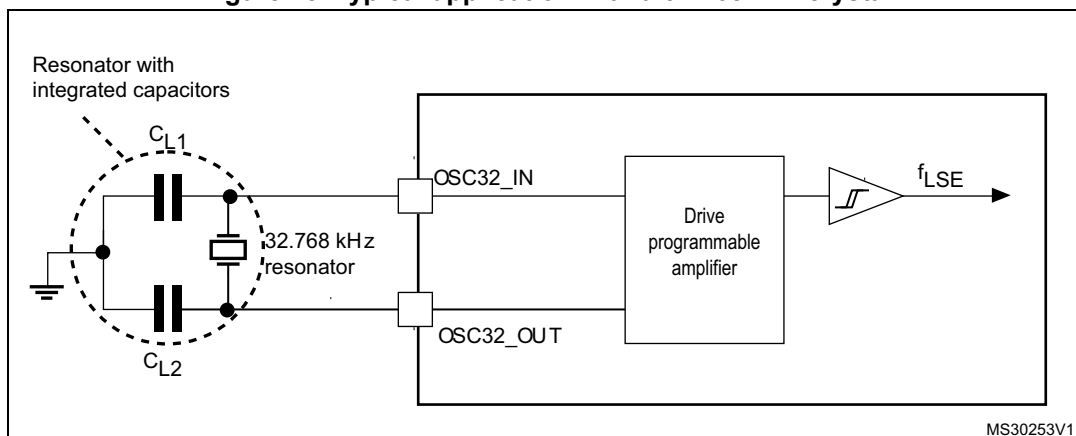
Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f _{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I _{DD}	Supply current in Run mode from V _{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	61.4	28.8	mA
			64 MHz	55.4	25.9	
			48 MHz	42.3	20.0	
			32 MHz	28.7	13.8	
			24 MHz	21.9	10.7	
			16 MHz	14.8	7.4	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	7.8	4.1	
			4 MHz	4.6	2.6	
			2 MHz	2.9	1.8	
			1 MHz	2.0	1.3	
			500 kHz	1.5	1.1	
			125 kHz	1.2	1.0	
I _{DDA} ⁽¹⁾⁽²⁾	Supply current in Run mode from V _{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	243.3	242.4	μA
			64 MHz	214.3	213.3	
			48 MHz	159.3	158.3	
			32 MHz	107.7	107.3	
			24 MHz	82.8	82.6	
			16 MHz	58.4	58.2	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	1.2	1.2	
			4 MHz	1.2	1.2	
			2 MHz	1.2	1.2	
			1 MHz	1.2	1.2	
			500 kHz	1.2	1.2	
			125 kHz	1.2	1.2	
I _{SDADC12} + I _{SDADC3}	Supply currents in Run mode from V _{DDSD12} and V _{DDSD3} (SDADCs are off)	-	-	2.5	1	μA

1. V_{DDA} monitoring is off, V_{DDSD12} monitoring is off.

2. When peripherals are enabled, power consumption of the analog part of peripherals such as ADC, DACs, Comparators, etc. is not included. Refer to those peripherals characteristics in the subsequent sections.

Figure 15. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between $OSC32_IN$ and $OSC32_OUT$ and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in [Table 42](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 22](#).

The provided curves are characterization results, not tested in production.

High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1 ⁽²⁾	%
$DuCy_{(HSI)}$	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	$T_A = -40$ to $105\text{ }^{\circ}\text{C}$	-3.8 ⁽³⁾	-	4.6 ⁽³⁾	%
		$T_A = -10$ to $85\text{ }^{\circ}\text{C}$	-2.9 ⁽³⁾	-	2.9 ⁽³⁾	%
		$T_A = 0$ to $70\text{ }^{\circ}\text{C}$	-2.3 ⁽³⁾	-	-2.2 ⁽³⁾	%
		$T_A = 25\text{ }^{\circ}\text{C}$	-1	-	1	%
$t_{su(HSI)}$	HSI oscillator startup time	-	1 ⁽³⁾	-	2 ⁽³⁾	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	100 ⁽³⁾	μA

1. $V_{DDA} = 3.3\text{ V}$, $T_A = -40$ to $105\text{ }^{\circ}\text{C}$ unless otherwise specified.

2. Guaranteed by design.

3. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 50. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105\text{ }^{\circ}\text{C}$ conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

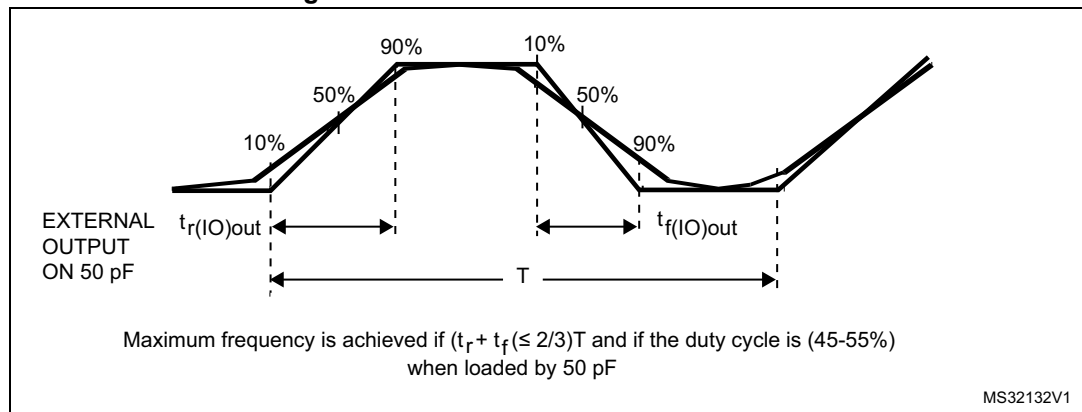
Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5\text{ }\mu\text{A}/+0\text{ }\mu\text{A}$ range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in [Table 51](#).

Figure 19. I/O AC characteristics definition



6.3.15 NRST characteristics

NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 52](#)).

Unless otherwise specified, the parameters given in [Table 55](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 22](#).

Table 55. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	-	-	-	$0.3V_{DD} + 0.07^{(1)}$	V
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage	-	$0.445V_{DD} + 0.398^{(1)}$	-	-	
$V_{hys(NRST)}^{(1)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse	-	500	-	-	ns

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.16 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in [Table 56](#). Refer also to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 56. I²C characteristics⁽¹⁾

Symbol	Parameter	Standard		Fast mode		Fast mode +		Unit
		Min	Max	Min	Max	Min	Max	
f _{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t _{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	μs
t _{HIGH}	High Period of the SCL clock	4	-	0.6	-	0.26	-	μs
t _r	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
t _f	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
t _{HD;DAT}	Data hold time	0	-	0	-	0	-	μs
t _{VD;DAT}	Data valid time	-	3.45 ⁽²⁾	-	0.9 ⁽²⁾	-	0.45 ⁽²⁾	μs
t _{VD;ACK}	Data valid acknowledge time	-	3.45 ⁽²⁾	-	0.9 ⁽²⁾	-	0.45 ⁽²⁾	μs
t _{SU;DAT}	Data setup time	250	-	100	-	50	-	ns
t _{HD;STA}	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	μs
t _{SU;STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	μs
t _{SU;STO}	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	μs
t _{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	μs
C _b	Capacitive load for each bus line	-	400	-	400	-	550	pF

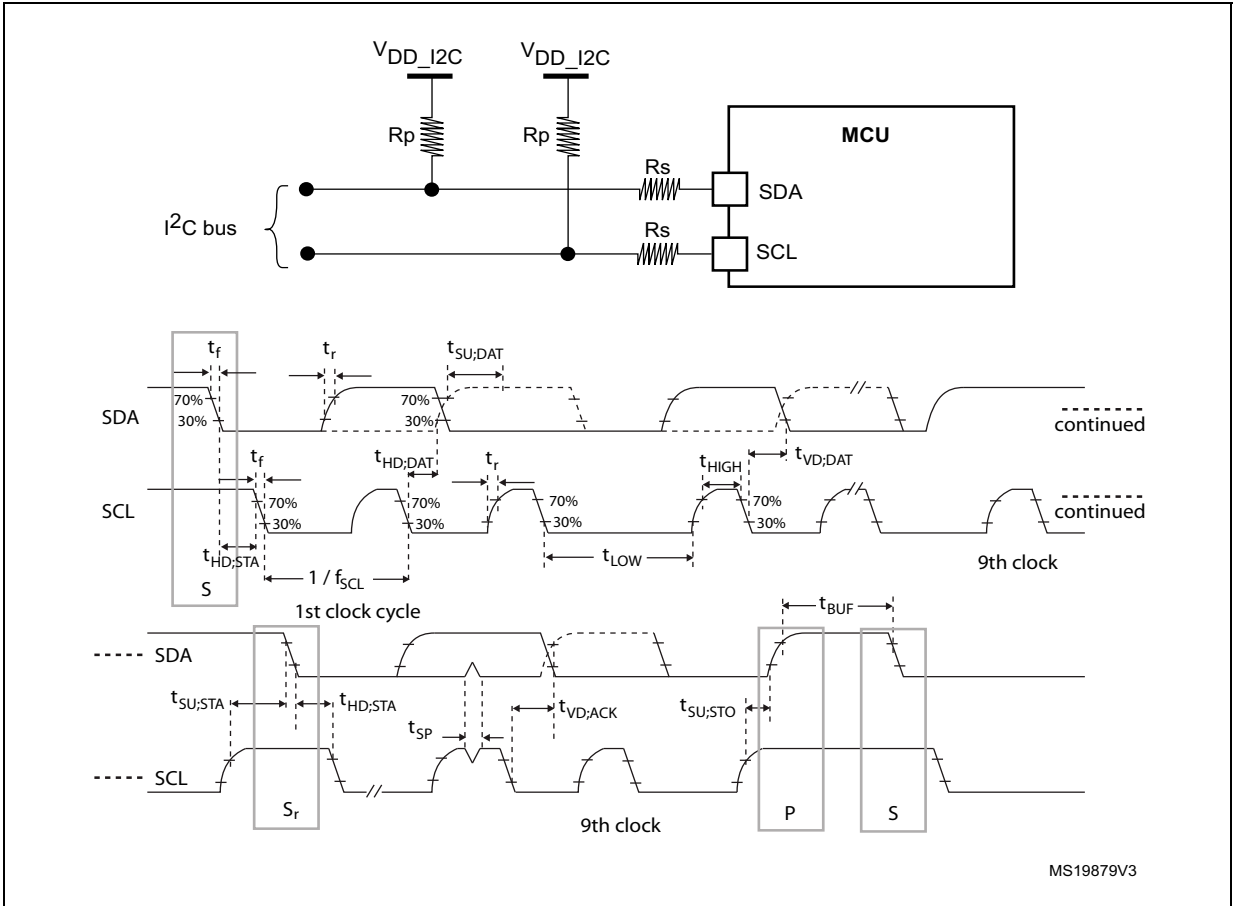
1. The I²C characteristics are the requirements from the I²C bus specification rev03. They are guaranteed by design when the I2Cx_TIMING register is correctly programmed (refer to reference manual). These characteristics are not tested in production.
2. The maximum t_{HD;DAT} could be 3.45 μs, 0.9 μs and 0.45 μs for standard mode, fast mode and fast mode plus, but must be less than the maximum of t_{VD;DAT} or t_{VD;ACK} by a transition time.

Table 57. I²C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

1. Guaranteed by design.
2. Spikes width below $t_{AF}(\min)$ are filtered.
3. Spikes width above $t_{AF}(\max)$ are not filtered.

Figure 21. I²C bus AC waveforms and measurement circuit



1. Legend: Rs: Series protection resistors. Rp: Pull-up resistors. V_{DD_I2C} : I2C bus supply.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in [Table 58](#) for SPI or in [Table 59](#) for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 22](#).

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 58. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}^{(1)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}^{(1)}$ $t_{f(SCK)}^{(1)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
$DuCy(SCK)^{(1)}$	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}^{(1)}$	NSS setup time	Slave mode	2T _{pclk}	-	ns
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode	4T _{pclk}	-	
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master mode, $f_{PCLK} = 36$ MHz, presc = 4	T _{pclk} /2 - 3	T _{pclk} /2 + 3	
$t_{su(MI)}^{(1)}$ $t_{su(SI)}^{(1)}$	Data input setup time	Master mode	5.5	-	
		Slave mode	6.5	-	
$t_{h(MI)}^{(1)}$ $t_{h(SI)}^{(1)}$	Data input hold time	Master mode	5	-	
		Slave mode	5	-	
$t_{a(SO)}^{(1)(2)}$	Data output access time	Slave mode, $f_{PCLK} = 24$ MHz	0	4T _{pclk}	
$t_{dis(SO)}^{(1)(3)}$	Data output disable time	Slave mode	0	24	
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	39	
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode (after enable edge)	-	3	
$t_{h(SO)}^{(1)}$ $t_{h(MO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	15	-	
		Master mode (after enable edge)	4	-	

1. Guaranteed by characterization results.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 60](#) are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 22](#).

Note: *It is recommended to perform a calibration after each power-up.*

Table 60. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0	-	-	V
$I_{DDA(ADC)}^{(1)}$	Current consumption from V_{DDA}	$V_{DD} = V_{DDA} = 3.3$ V	-	0.9	-	mA
I_{VREF}	Current on the V_{REF} input pin	-	-	160 ⁽²⁾	220 ⁽²⁾	μA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
$f_S^{(3)}$	Sampling rate	-	0.05	-	1	MHz
$f_{TRIG}^{(3)}$	External trigger frequency	$f_{ADC} = 14$ MHz	-	-	823	kHz
		-	-	-	17	1/ f_{ADC}
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
$R_{SRC}^{(3)}$	Signal source impedance	See Equation 1 and Table 61 for details	-	-	50	kΩ
$R_{ADC}^{(3)}$	Sampling switch resistance	-	-	-	1	kΩ
$C_{ADC}^{(3)}$	Internal sample and hold capacitor	-	-	-	8	pF
$t_{CAL}^{(3)}$	Calibration time	$f_{ADC} = 14$ MHz	5.9			μs
		-	83			1/ f_{ADC}
$t_{lat}^{(3)}$	Injection trigger conversion latency	$f_{ADC} = 14$ MHz	-	-	0.214	μs
		-	-	-	2 ⁽⁴⁾	1/ f_{ADC}
$t_{latr}^{(3)}$	Regular trigger conversion latency	$f_{ADC} = 14$ MHz	-	-	0.143	μs
		-	-	-	2 ⁽⁴⁾	1/ f_{ADC}
$t_S^{(3)}$	Sampling time	$f_{ADC} = 14$ MHz	0.107	-	17.1	μs
		-	1.5	-	239.5	1/ f_{ADC}
$t_{STAB}^{(3)}$	Power-up time	-	-	-	1	μs
$t_{CONV}^{(3)}$	Total conversion time (including sampling time)	$f_{ADC} = 14$ MHz	1	-	18	μs
		-	14 to 252 (t_S for sampling + 12.5 for successive approximation)			1/ f_{ADC}

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 μA on I_{DDA} and 60 μA on I_{DD} is present
2. Guaranteed by characterization results.
3. Guaranteed by design.
4. For external triggers, a delay of 1/ f_{PCLK2} must be added to the latency specified in [Table 60](#)

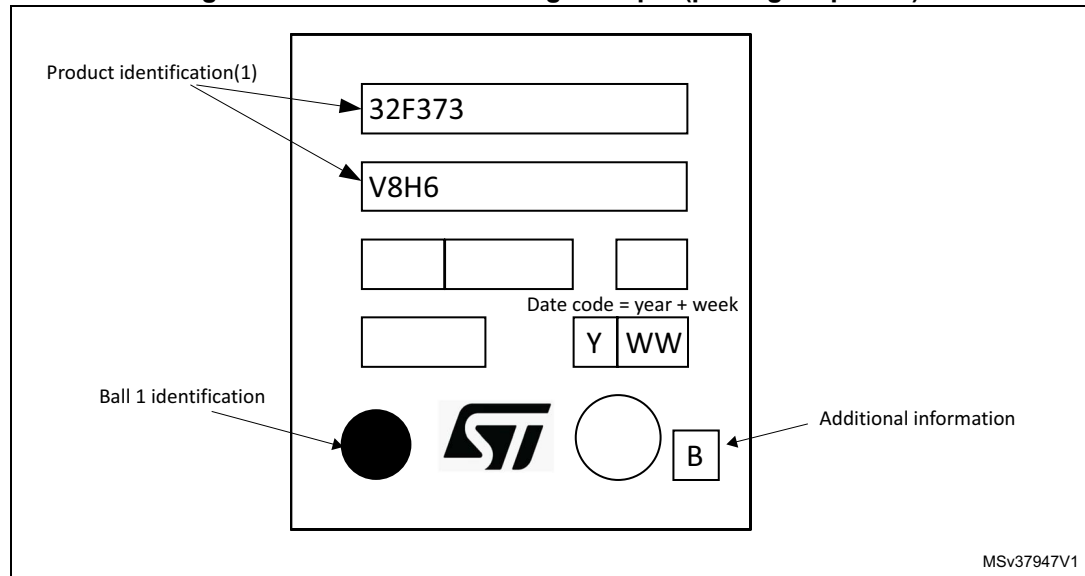
Table 74. SDADC characteristics (continued)⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
V_{REFSD-}	Negative ref. voltage	-	-	V_{SSA}	-	V	-
I_{DDSDx}	Supply current ($V_{DDSDx} = 3.3$ V)	Normal mode ($f_{ADC} = 6$ MHz)	-	800	1200	μA	-
		Slow mode ($f_{ADC} = 1.5$ MHz)	-	-	600		-
		Standby	-	-	200		-
		Power down	-	-	2.5		-
		SD_ADC off	-	-	1		-
V_{AIN}	Common input voltage range	Single ended mode (zero reference)	V_{REFSD-}	-	V_{REFSD+}/gain	V	Voltage on AINP or AINN pin
		Single ended offset mode	V_{REFSD-}	-	$V_{REFSD+}/(\text{gain} \times 2)$		
		Differential mode	V_{SSA}	-	V_{DDSDx}		
V_{DIFF}	Differential input voltage	Differential mode only	$-V_{REFSD+}/(\text{gain} \times 2)$	-	$V_{REFSD+}/(\text{gain} \times 2)$	-	Differential voltage between AINP and AINN
f_s	Sampling rate	Slow mode ($f_{ADC} = 1.5$ MHz)	-	4.166	-	kHz	$f_{ADC}/360$
		Slow mode one channel only ($f_{ADC} = 1.5$ MHz)	-	12.5	-		$f_{ADC}/120$
		Normal mode multiplexed channel ($f_{ADC} = 6$ MHz)	-	16.66	-		$f_{ADC}/360$
		Normal mode one channel only, FAST= 1 ($f_{ADC} = 6$ MHz)	-	50	-		$f_{ADC}/120$
t_{CONV}	Conversion time	-	-	1/fs	-	s	-
R_{AIN}	Analog input impedance	One channel, gain = 0.5, $f_{ADC} = 1.5$ MHz	-	540	-	k Ω	see reference manual for detailed description
		One channel, gain = 0.5, $f_{ADC} = 6$ MHz	-	135	-		
		One channel, gain = 8, $f_{ADC} = 6$ MHz	-	47	-		
t_{CALIB}	Calibration time	$f_{ADC} = 6$ MHz, one offset calibration	-	5120	-	μs	$30720/f_{ADC}$
t_{STAB}	Stabilization time	From power down $f_{ADC} = 6$ MHz	-	100	-	μs	$600/f_{ADC}$, $75/f_{ADC}$ if SLOWCK = 1
$t_{STANDBY}$	Wakeup from standby time	$f_{ADC} = 6$ MHz	-	50	-	μs	$300/f_{ADC}$
		$f_{ADC} = 1.5$ MHz	-	50	-		$75/f_{ADC}$ if SLOWCK = 1

Device Marking for UFBGA100

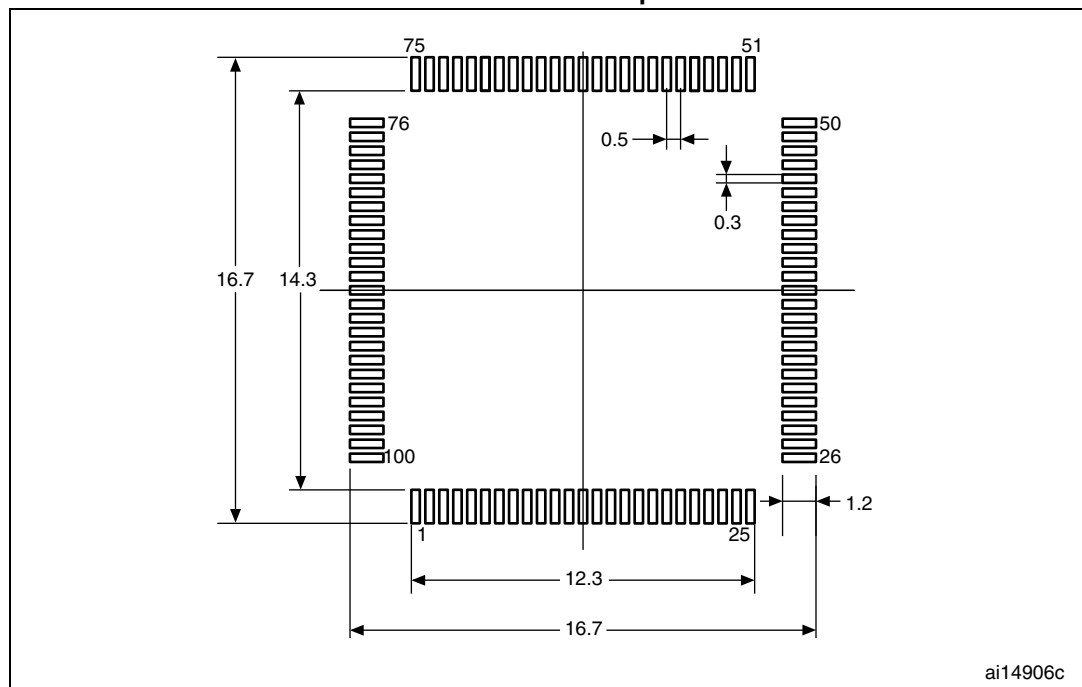
The following figure gives an example of topside marking orientation versus ball 1 identifier location.

Figure 34. UFBGA100 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 36. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

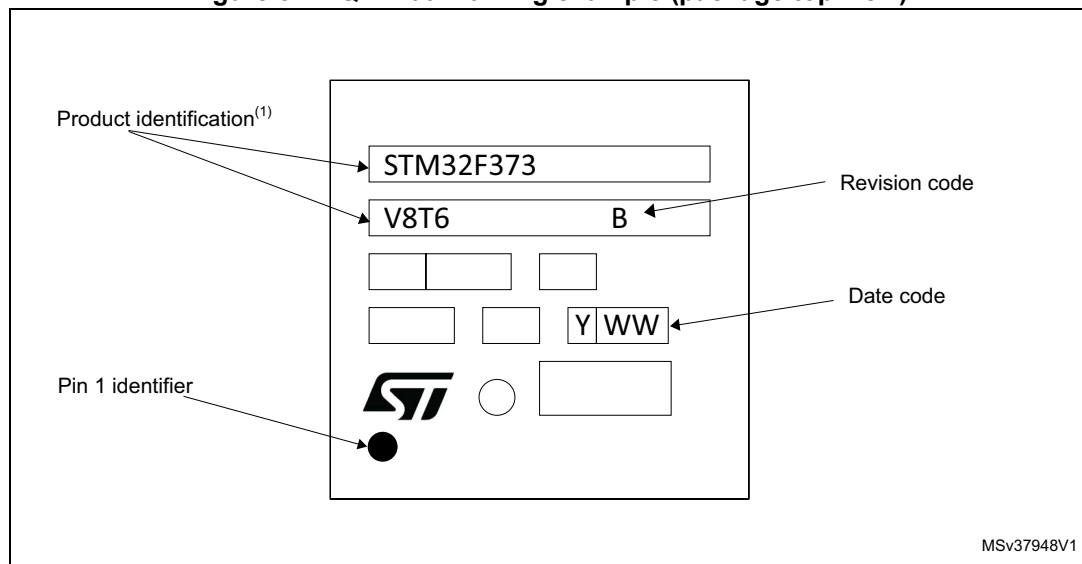


1. Dimensions are expressed in millimeters.

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 37. LQFP100 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 83. Document revision history (continued)

Date	Revision	Changes
19-Sep-2013	4	<p>Replaced "Cortex-M4F" with "Cortex-M4" throughout the document.</p> <p>Removed part number STM32F372xx.</p> <p>Added "1.25 DMIPS/MHz (Dhrystone 2.1)" in Features.</p> <p>Updated Introduction.</p> <p>Added reference to the STMTouch touch sensing firmware library in Section 3.16: Touch sensing controller (TSC).</p> <p>Added "All I2S interfaces can operate in half-duplex mode only." in Section 3.21: Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S).</p> <p>Added row "I2S full-duplex mode" to Table 9: STM32F373xx SPI/I2S implementation.</p> <p>Modified introduction of I2C interface characteristics.</p> <p>Added alternate function RTC_REFIN and removed additional function RTC_REF_CLK_IN to pins PA1 and PB15.</p> <p>Replaced alternate function JNTRST with NJTRST for pin PB4.</p> <p>In Table 12: Alternate functions for port PA: replaced alternate function JTMS-SWDIO with SWDIO-JTMS for pin PA13, and JTCK-SWCLK with SWCLK-JTCK for pin PA14.</p> <p>Added rows V_{REF+} and V_{REFSD+} to Table 22: General operating conditions.</p> <p>Replaced "$f_{APB1} = f_{AHB}/2$" with "$f_{APB1} = f_{AHB}$" for "When the peripherals are enabled..." in Typical current consumption.</p> <p>Added COMP in Table 36: Peripheral current consumption.</p> <p>Added conditions for f_{HSE_ext} in Table 38: High-speed external user clock characteristics.</p> <p>Added Min and Max values for ACC_{HISI} in Table 42: HSI oscillator characteristics.</p> <p>Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in Table 49: ESD absolute maximum ratings.</p> <p>Removed pins PB0 and PB1 in description of I_{INJ} in Table 51: I/O current injection susceptibility.</p> <p>Updated Table 56: I2C characteristics.</p> <p>Replaced all occurrences of "gain/2" with "gain*2" in Table 74: SDADC characteristics.</p> <p>Corrected typo in Figure 19: I/O AC characteristics definition.</p> <p>Replaced Figure 21: I2C bus AC waveforms and measurement circuit.</p> <p>Added $I_{DDA(ADC)}$ and footnote 1 in Table 60: ADC characteristics.</p>