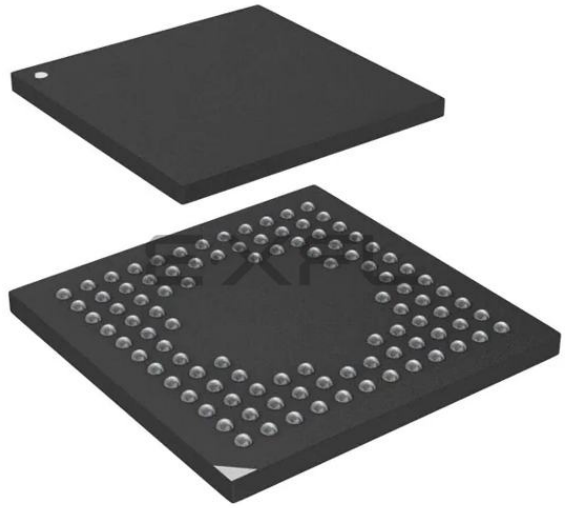

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373vbh6

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F373xx microcontrollers.

This STM32F373xx datasheet should be read in conjunction with the RM0313 reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 with FPU core, please refer to:

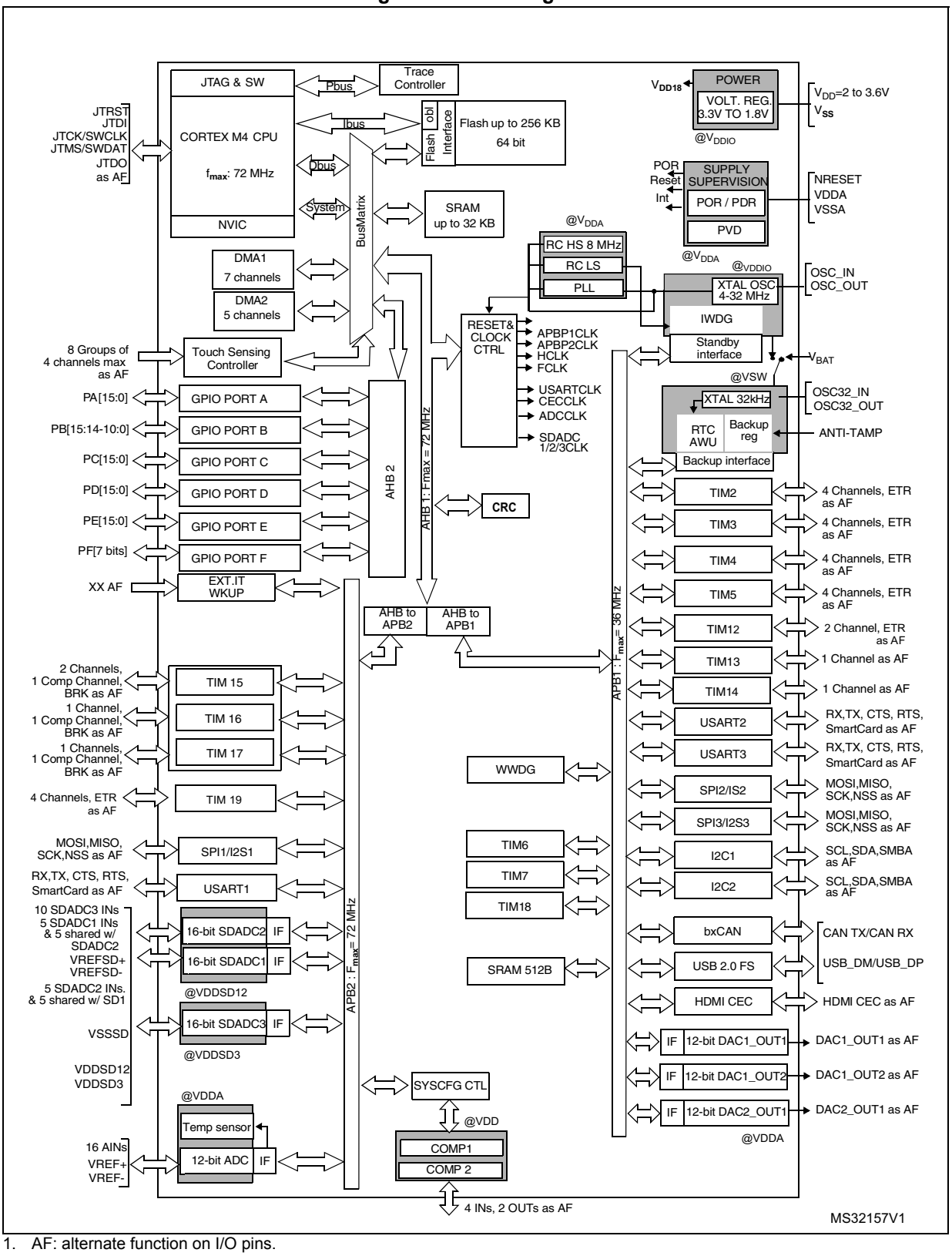
- Cortex®-M4 with FPU Technical Reference Manual, available from www.arm.com.
- STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

Table 2. Device overview

Peripheral		STM32F 373Cx			STM32F 373Rx			STM32F 373Vx		
Flash (Kbytes)		64	128	256	64	128	256	64	128	256
SRAM (Kbytes)		16	24	32	16	24	32	16	24	32
Timers	General purpose	9 (16-bit) 2 (32 bit)								
	Basic	3 (16-bit)								
Comm. interfaces	SPI/I2S	3								
	I^2C	2								
	USART	3								
	CAN	1								
	USB	1								
GPIOs	Normal I/Os (TC, TTa)	36			52			84		
	5 volts Tolerant I/Os (FT, Ftf)	20			28			45		
12-bit ADCs		1								
16-bit ADCs Sigma- Delta		3								
12-bit DACs outputs		3								
Analog comparator		2								
Capacitive sensing channels		14			17			24		
Max. CPU frequency		72 MHz								
Main operating voltage		2.0 to 3.6 V								
16-bit SDADC operating voltage		2.2 to 3.6 V								
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - -40 to 125 °C								
Packages		LQFP48			LQFP64			LQFP100, UFBGA100(1)		

1. UFBGA100 package available on 256-KB versions only.

Figure 1. Block diagram



1. AF: alternate function on I/O pins.

3.3 Embedded Flash memory

All STM32F373xx devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Embedded SRAM

All STM32F373xx devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.15 Fast comparators (COMP)

The STM32F373xx embeds 2 comparators with rail-to-rail inputs and high-speed output. The reference voltage can be internal or external (delivered by an I/O).

The threshold can be one of the following:

- DACs channel outputs
- External I/O
- Internal reference voltage (V_{REFINT}) or submultiple (1/4 V_{REFINT}, 1/2 V_{REFINT} and 3/4 V_{REFINT})

The comparators can be combined into a window comparator.

Both comparators can wake up the device from Stop mode and generate interrupts and breaks for the timers.

3.16 Touch sensing controller (TSC)

The devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Up to 24 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 8 acquisition groups, with up to 4 I/Os in each group.

Table 3. Capacitive sensing GPIOs available on STM32F373xx devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4(1)	6	TSC_G6_IO1	PB14
	TSC_G2_IO2	PA5(1)		TSC_G6_IO2	PB15
	TSC_G2_IO3	PA6(1)		TSC_G6_IO3	PD8
	TSC_G2_IO4	PA7		TSC_G6_IO4	PD9

- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.19 Inter-integrated circuit interface (I^2C)

Two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes with 20 mA output drive. They support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I^2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeout verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the application to wake up the MCU from Stop mode on address match.

The I^2C interfaces can be served by the DMA controller

Refer to *Table 7* for the differences between I2C1 and I2C2.

Table 7. STM32F373xx I^2C implementation

I^2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X

3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

Three SPIs are able to communicate at up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I2S interfaces can operate in half-duplex mode only.

Refer to *Table 9* for the features between SPI1, SPI2 and SPI3.

Table 9. STM32F373xx SPI/I2S implementation

SPI features(1)	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	X	X	X
TI mode	X	X	X
I2S full-duplex mode	-	-	-

1. X = supported.

3.22 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

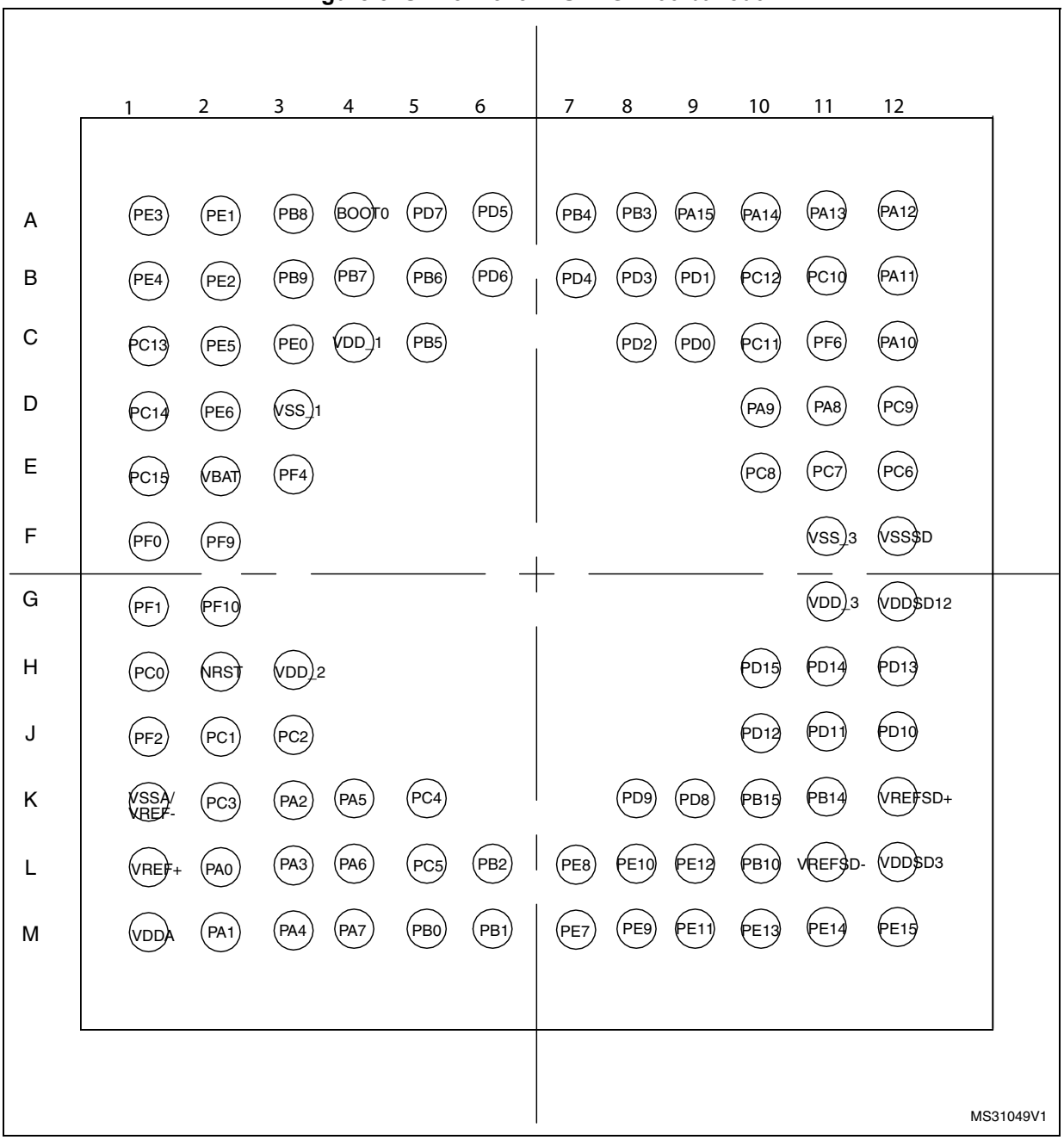
The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

Figure 5. STM32F373xx UFBGA100 ballout



1. The above figure shows the package top view.

Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. STM32F373xx pin definitions

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
1	B2	-	-	PE2	I/O	FT	(2)	TSC_G7_IO1, TRACECLK	-
2	A1	-	-	PE3	I/O	FT	(2)	TSC_G7_IO2, TRACED0	-
3	B1	-	-	PE4	I/O	FT	(2)	TSC_G7_IO3, TRACED1	-
4	C2	-	-	PE5	I/O	FT	(2)	TSC_G7_IO4, TRACED2	-
5	D2	-	-	PE6	I/O	FT	(2)	TRACED3	WKUP3, RTC_TAMPER3
6	E2	1	1	VBAT	S	-	-	Backup power supply	
7	C1	2	2	PC13(1)	I/O	TC	-	-	WKUP2, ALARM_OUT, CALIB_OUT, TIMESTAMP, RTC_TAMPER1

Table 17. Alternate functions for port PF

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	-	-	I2C2_SDA	-	-	-
PF1	-	-	-	-	I2C2_SCL	-	-	-
PF2	-	EVENTOUT	-	-	I2C2_SMBA	-	-	-
PF4	-	EVENTOUT	-	-	-	-	-	-
PF6	-	EVENTOUT	TIM4_CH4	-	I2C2_SCL	SPI1_MOSI/I2S1_SD	-	USART3_RTS
PF7	-	EVENTOUT	-	-	I2C2_SDA	-	-	USART2_CK
PF9	-	EVENTOUT	TIM14_CH1	-	-	-	-	-
PF10	-	EVENTOUT	-	-	-	-	-	-

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{APB1} = f_{AHB}/2$, $f_{APB2} = f_{AHB}$
- When f_{HCLK} > 8 MHz PLL is ON and PLL inputs is equal to HSI/2 = 4 MHz (if internal clock is used) or HSE = 8 MHz (if HSE bypass mode is used)

The parameters given in *Table 28* to *Table 34* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V(1)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	HSE bypass, PLL on	72 MHz	63.1	70.7	71.5	73.4	29.2	31.1	31.7	34.2	mA
			64 MHz	56.3	63.3	64.1	64.9	26.1	27.8	28.4	30.4	
			48 MHz	42.5	48.5	48.0	50.1	19.9	22.6	21.9	23.1	
			32 MHz	28.8	31.4	32.2	34.3	13.1	16.1	14.9	16.2	
			24 MHz	21.9	24.4	24.4	25.8	10.1	10.9	11.9	12.4	
		HSE bypass, PLL off	8 MHz	7.3	8.0	9.3	9.3	3.7	4.1	4.4	5.0	
			1 MHz	1.1	1.5	1.8	2.3	0.8	1.1	1.4	1.9	
		HSI clock, PLL on	64 MHz	51.7	57.7	58.0	60.4	25.8	27.6	28.1	30.1	
			48 MHz	38.6	45.9	43.5	46.9	19.8	21.9	21.7	22.8	
			32 MHz	26.4	31.1	29.7	31.9	13.1	15.7	14.8	16.2	
			24 MHz	20.3	22.6	22.6	23.7	6.9	7.5	8.1	8.8	
		HSI clock, PLL off	8 MHz	7.0	7.6	8.8	8.8	3.7	4.1	4.4	5.0	

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]= 10 medium low driving capability	-	-	1	
		LSEDRV[1:0] = 01 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]= 10 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 01 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 45. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 kB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design.

Table 46. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Table 51. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	-0	NA	mA
	Injected current on PC0 pin	-0	+5	
	Injected current on TC type I/O pins on VDDSD12 power domain: PB2, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB10 with induced leakage current on other pins from this group less than -50 µA	-5	+5	
	Injected current on TC type I/O pins on VDDSD3 power domain: PB14, PB15, PD8, PD9, PD10, PD12, PD13, PD14, PD15 with induced leakage current on other pins from this group less than -50 µA	-5	+5	
	Injected current on TTa type pins: PA4, PA5, PA6 with induced leakage current on adjacent pins less than -10 µA	-5	+5	
	Injected current on any other FT and FTf pins	-5	NA	
	Injected current on any other pins	-5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 58* for SPI or in *Table 59* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 58. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$ (1)	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$ (1)	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)(1)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	2Tpclk	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	4Tpclk	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 - 3	Tpclk/2 + 3	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5.5	-	
		Slave mode	6.5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$ (1)		Slave mode	5	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	4Tpclk	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	0	24	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	39	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	4	-	

1. Guaranteed by characterization results.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 60* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 22*.

Note: It is recommended to perform a calibration after each power-up.

Table 60. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0	-	-	V
$I_{DDA(ADC)}$(1)	Current consumption from V_{DDA}	$V_{DD} = V_{DDA} = 3.3$ V	-	0.9	-	mA
I_{VREF}	Current on the V_{REF} input pin	-	-	160(2)	220(2)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(3)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{SRC}(3)	Signal source impedance	See *Equation 1* and *Table 61* for details	-	-	50	kΩ
R_{ADC}(3)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(3)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(3)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_{latr}(3)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(3)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(3)	Power-up time	-	-	-	1	µs
t_{CONV}(3)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} is present
2. Guaranteed by characterization results.
3. Guaranteed by design.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 60*

6.3.20 Temperature sensor characteristics

Table 65. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ± 5 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C ± 5 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

Table 66. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(2)(1)	ADC sampling time when reading the temperature	17.1	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.21 V_{BAT} monitoring characteristics

Table 67. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.22 Timer characteristics

The parameters given in *Table 68* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 83. Document revision history (continued)

Date	Revision	Changes
19-Sep-2013	4	Replaced “Cortex-M4F” with “Cortex-M4” throughout the document. Removed part number STM32F372xx. Added “1.25 DMIPS/MHz (Dhrystone 2.1)” in *Features*. Updated *Introduction*. Added reference to the STMTouch touch sensing firmware library in *Section 3.16: Touch sensing controller (TSC)*. Added “All I2S interfaces can operate in half-duplex mode only.” in *Section 3.21: Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)*. Added row “I2S full-duplex mode” to *Table 9: STM32F373xx SPI/I2S implementation*. Modified introduction of *I2C interface characteristics*. Added alternate function RTC_REFIN and removed additional function RTC_REF_CLK_IN to pins PA1 and PB15. Replaced alternate function JNTRST with NJTRST for pin PB4. In *Table 12: Alternate functions for port PA*: replaced alternate function JTMS-SWDIO with SWDIO-JTMS for pin PA13, and JTCK-SWCLK with SWCLK-JTCK for pin PA14. Added rows V_{REF+} and V_{REFSD+} to *Table 22: General operating conditions*. Replaced "$f_{APB1} = f_{AHB/2}$" with "$f_{APB1} = f_{AHB}$" for “When the peripherals are enabled...” in *Typical current consumption*. Added COMP in *Table 36: Peripheral current consumption* Added conditions for f_{HSE_ext} in *Table 38: High-speed external user clock characteristics*. Added Min and Max values for ACC_{HSI} in *Table 42: HSI oscillator characteristics*. Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in *Table 49: ESD absolute maximum ratings*. Removed pins PB0 and PB1 in description of I_{INJ} in *Table 51: I/O current injection susceptibility*. Updated *Table 56: I2C characteristics*. Replaced all occurrences of “gain/2” with “gain*2” in *Table 74: SDADC characteristics*. Corrected typo in *Figure 19: I/O AC characteristics definition*. Replaced *Figure 21: I2C bus AC waveforms and measurement circuit*.. Added $I_{DDA(ADC)}$ and footnote 1 in *Table 60: ADC characteristics*