Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373vbt6

1 Introduction

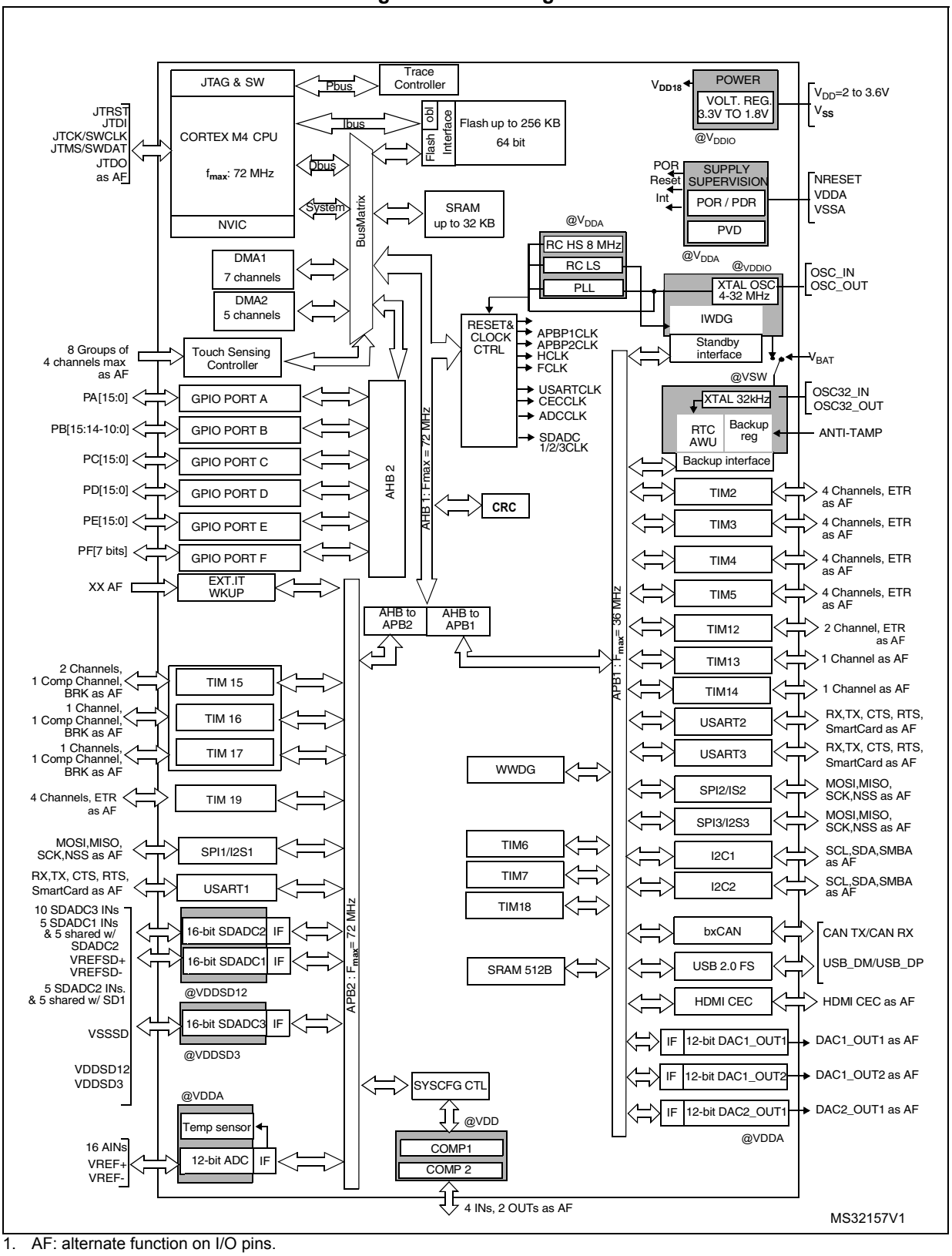
This datasheet provides the ordering information and mechanical device characteristics of the STM32F373xx microcontrollers.

This STM32F373xx datasheet should be read in conjunction with the RM0313 reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 with FPU core, please refer to:

- Cortex®-M4 with FPU Technical Reference Manual, available from www.arm.com.
- STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

Figure 1. Block diagram



1. AF: alternate function on I/O pins.

3.13 16-bit sigma delta analog-to-digital converters (SDADC)

Three 16-bit sigma-delta analog-to-digital converters are embedded in the STM32F373xx. They have up to two separate supply voltages allowing the analog function voltage range to be independent from the STM32F373xx power supply. They share up to 21 input pins which may be configured in any combination of single-ended (up to 21) or differential inputs (up to 11).

The conversion speed is up to 16.6 ksps for each SDADC when converting multiple channels and up to 50 ksps per SDADC if single channel conversion is used. There are two conversion modes: single conversion mode or continuous mode, capable of automatically scanning any number of channels. The data can be automatically stored in a system RAM buffer, reducing the software overhead.

A timer triggering system can be used in order to control the start of conversion of the three SDADCs and/or the 12-bit fast ADC. This timing control is very flexible, capable of triggering simultaneous conversions or inserting a programmable delay between the ADCs.

Up to two external reference pins (VREFSD+, VREFSD-) and an internal 1.2/1.8 V reference can be used in conjunction with a programmable gain (x0.5 to x32) in order to fine-tune the input voltage range of the SDADC. VREFSD - pin is used as negative signal reference in case of single-ended input mode.

3.14 Digital-to-analog converter (DAC)

The devices feature two 12-bit buffered DACs with three output channels that can be used to convert three digital signals into three analog voltage signal outputs. The internal structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital Interface supports the following features:

- Two DAC converters with three output channels:
  - DAC1 with two output channels
  - DAC2 with one output channel.
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation (DAC1 only)
- Triangular wave generation (DAC1 only)
- Dual DAC channel independent or simultaneous conversions (DAC1 only)
- DMA capability for each channel
- External triggers for conversion

3.17 Timers and watchdogs

The STM32F373xx includes two 32-bit and nine 16-bit general-purpose timers, three basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM2 TIM5	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM3, TIM4, TIM19	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	0
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	0
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7, TIM18	16-bit	Up	Any integer between 1 and 65536	Yes	0	0

- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.19 Inter-integrated circuit interface (I^2C)

Two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes with 20 mA output drive. They support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I^2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeout verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the application to wake up the MCU from Stop mode on address match.

The I^2C interfaces can be served by the DMA controller

Refer to *Table 7* for the differences between I2C1 and I2C2.

Table 7. STM32F373xx I^2C implementation

I^2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X

Table 17. Alternate functions for port PF

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	-	-	I2C2_SDA	-	-	-
PF1	-	-	-	-	I2C2_SCL	-	-	-
PF2	-	EVENTOUT	-	-	I2C2_SMBA	-	-	-
PF4	-	EVENTOUT	-	-	-	-	-	-
PF6	-	EVENTOUT	TIM4_CH4	-	I2C2_SCL	SPI1_MOSI/I2S1_SD	-	USART3_RTS
PF7	-	EVENTOUT	-	-	I2C2_SDA	-	-	USART2_CK
PF9	-	EVENTOUT	TIM14_CH1	-	-	-	-	-
PF10	-	EVENTOUT	-	-	-	-	-	-

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DDSDx}, V_{BAT} and V_{DD})	- 0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for V_{DD} > V_{DDA}	-	0.4	
V_{DDSDx} – V_{DDA}	Allowed voltage difference for V_{DDSDx} > V_{DDA}	-	0.4	
V_{REFSD+} – V_{DDSD3}	Allowed voltage difference for V_{REFSD+} > V_{DDSD3}	-	0.4	
V_{REF+} – V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on TTa pins	V_{SS} - 0.3	4.0	
	Input voltage on TC pins on SDADCx channels inputs(3)	V_{SS} - 0.3	4.0	
	Input voltage on any other pin	V_{SS} - 0.3	4.0	
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$\lvert V_{REFSD-} - V_{SSx}\rvert$		-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (I/O ground pin is internally connected to V_{SS}). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (I/O ground pin is internally connected to V_{SS}).

All main power (V_{DD}, V_{DDSD12}, V_{DDSD3} and V_{DDA}) and ground (V_{SS}, V_{SSSD}, and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

The following relationship must be respected between V_{DDA} and V_{DD}: V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence. V_{DDA} must be greater than or equal to V_{DD}.

The following relationship must be respected between V_{DDA} and V_{DDSD12}: V_{DDA} must power on before or at the same time as V_{DDSD12} or V_{DDSD3} in the power up sequence. V_{DDA} must be greater than or equal to V_{DDSD12} or V_{DDSD3}.

The following relationship must be respected between V_{DDSD12} and V_{DDSD3}: V_{DDSD3} must power on before or at the same time as V_{DDSD12} in the power up sequence.
After power up (V_{DDSD12} > Vrefint = 1.2 V) V_{DDSD3} can be higher or lower than V_{DDSD12}.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 37. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = V_{DDA}					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.1	3.9	3.8	3.7	3.6	4.5	µs
		Regulator in low power mode	7.9	6.7	6.1	5.7	5.4	8.6	
$t_{WUSTANDBY}$	Wakeup from Standby mode	LSI and IWDG off	62.6	53.7	49.2	45.7	42.7	100	
$t_{WUSLEEP}$	Wakeup from Sleep mode	After WFE instruction	6						CPU clock cycles

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 12*.

Table 38. High-speed external user clock characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	-	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	-	20	

1. Guaranteed by design.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 47*. They are based on the EMS levels and classes defined in application note AN1709.

Table 47. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

Figure 22. SPI timing diagram - slave mode and CPHA = 0

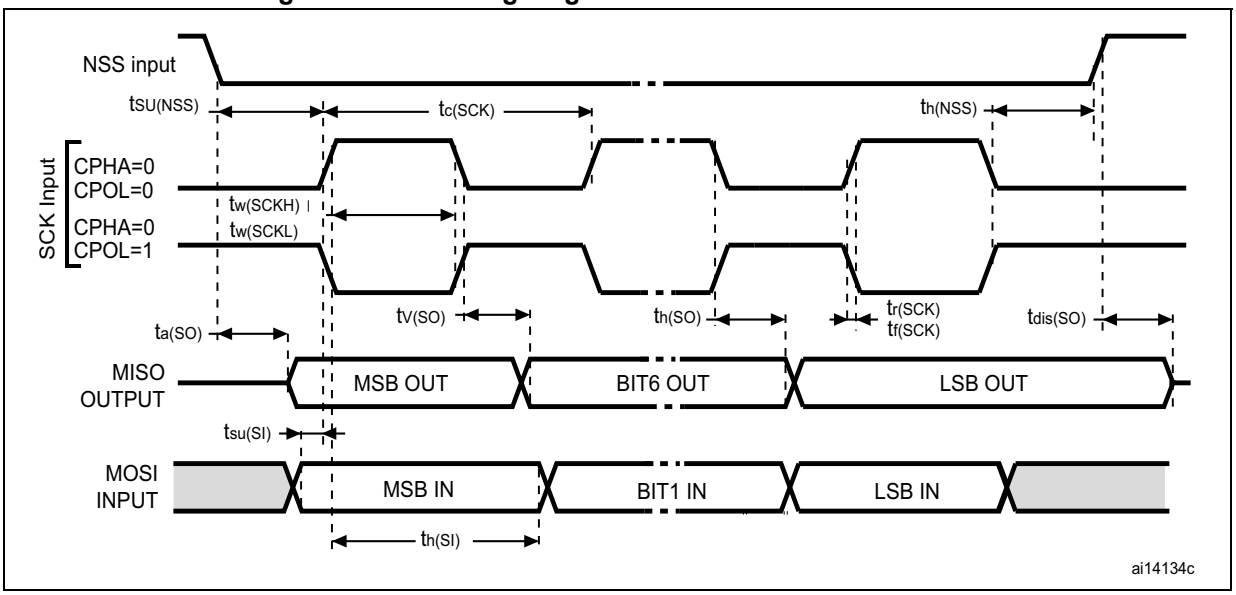
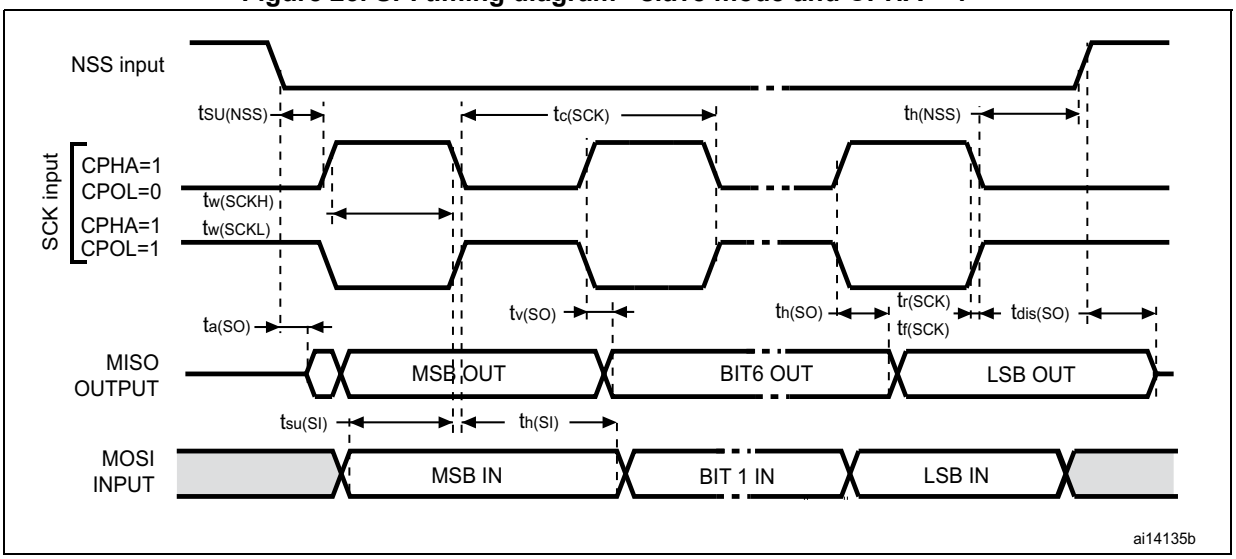
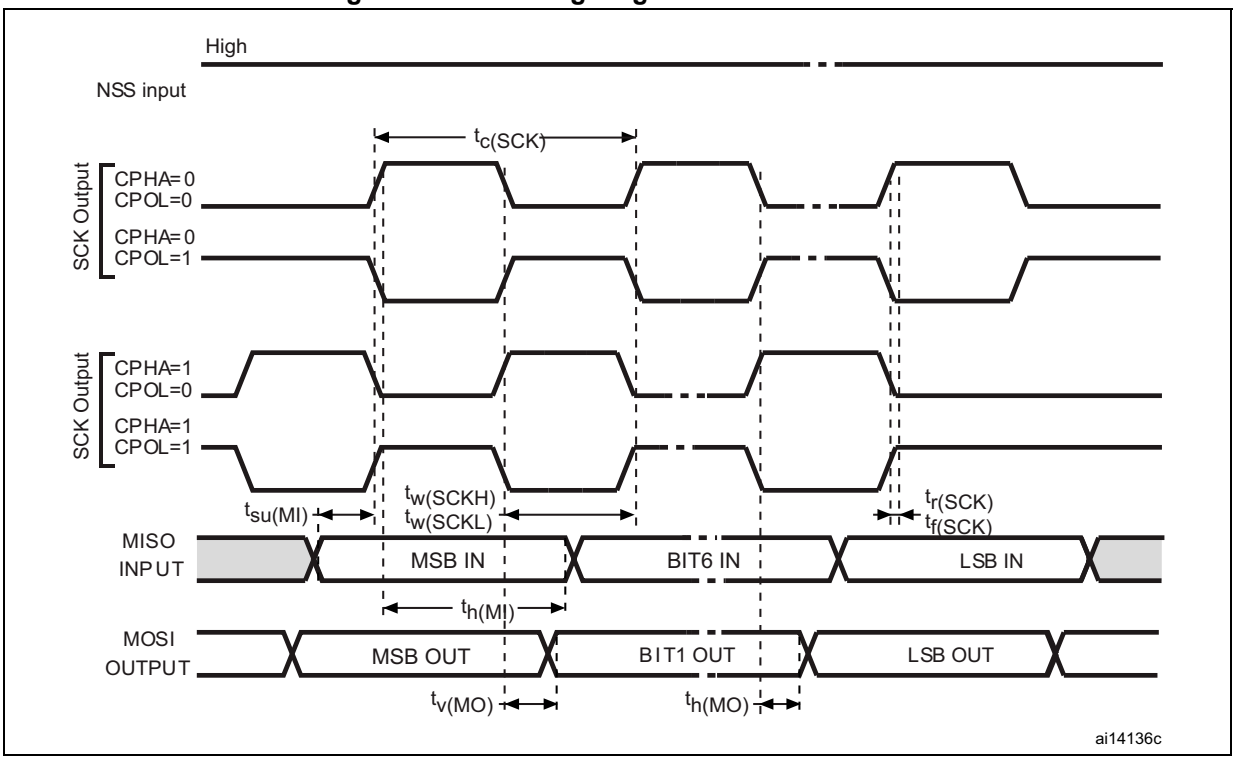


Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.

Figure 24. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.

6.3.18 DAC electrical specifications

Table 63. DAC characteristics

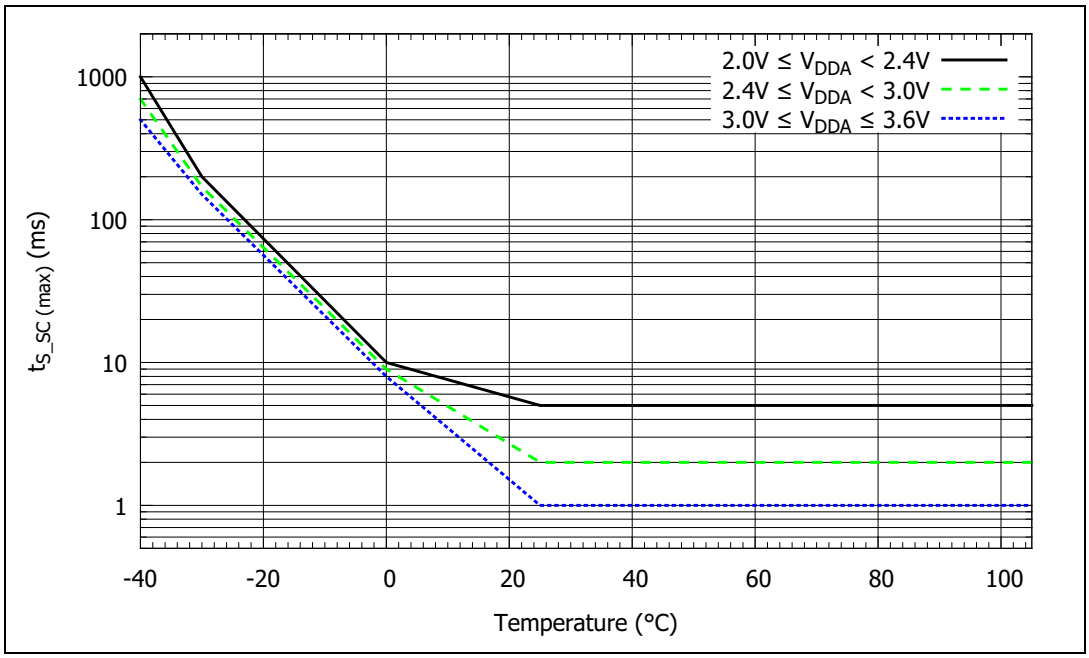
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.4	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}		2.4	-	3.6	V
V_{SSA}	Ground		-	0	-	0	V
R_{LOAD}(1)	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
R_O(1)	Output Impedance	DAC output buffer OFF		-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).		-	-	50	pF
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) and (0xEAB) at V_{REF+} = 2.4 V		0.2	-	-	V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON			-	-	V_{DDA} – 0.2	V
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	It gives the maximum output excursion of the DAC.		-	0.5	-	mV
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF			-	-	V_{REF+} – 1LSB	V
$I_{DDVREF+}$(3)	DAC DC current consumption in quiescent mode (Standby mode)	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs		-	-	220	µA
I_{DDA}(3)	DAC DC current consumption in quiescent mode(2)	With no load, middle code (0x800) on the inputs		-	-	380	µA
		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs		-	-	480	µA
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for the DAC in 10-bit configuration		-	-	± 0.5	LSB
		Given for the DAC in 12-bit configuration		-	-	± 2	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	Given for the DAC in 10-bit configuration		-	-	± 1	LSB
		Given for the DAC in 12-bit configuration		-	-	± 4	LSB

Table 64. Comparator characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

1. Guaranteed by design.
2. For more details and conditions see *Figure 30: Maximum VREFINT scaler startup time from power down*

Figure 30. Maximum V_{REFINT} scaler startup time from power down



6.3.23 USB characteristics

Table 71. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 72. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity (for USB compliance)	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers

Table 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 33. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

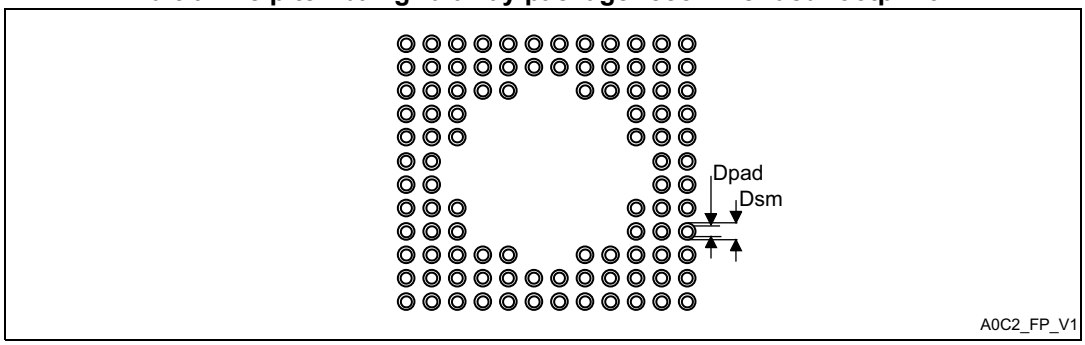
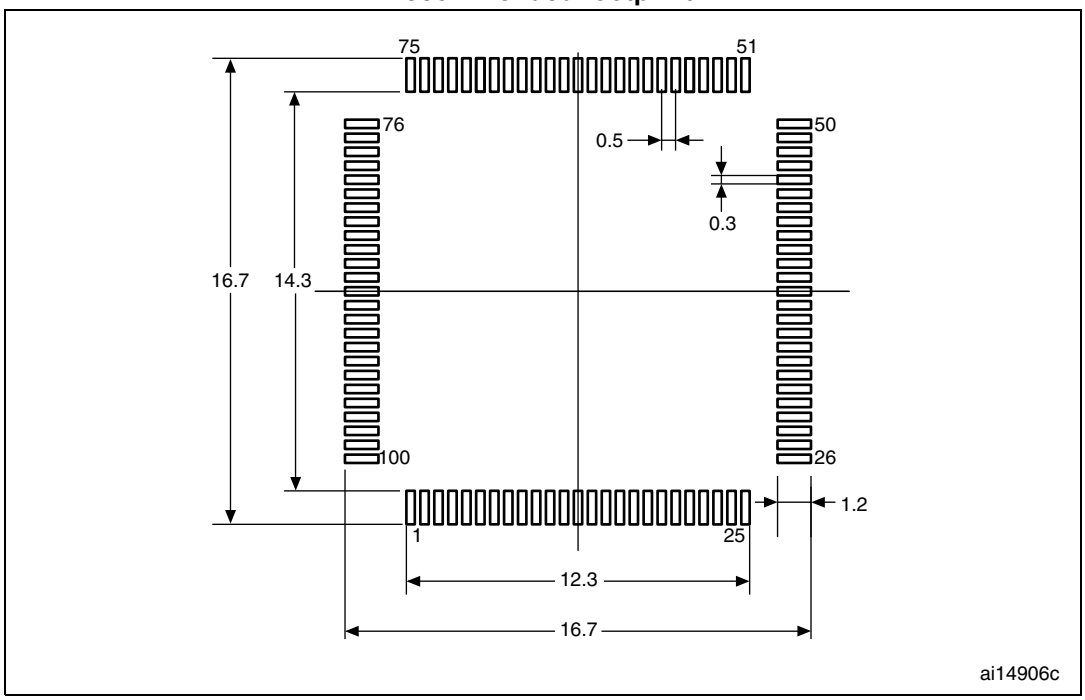


Table 77. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Figure 36. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

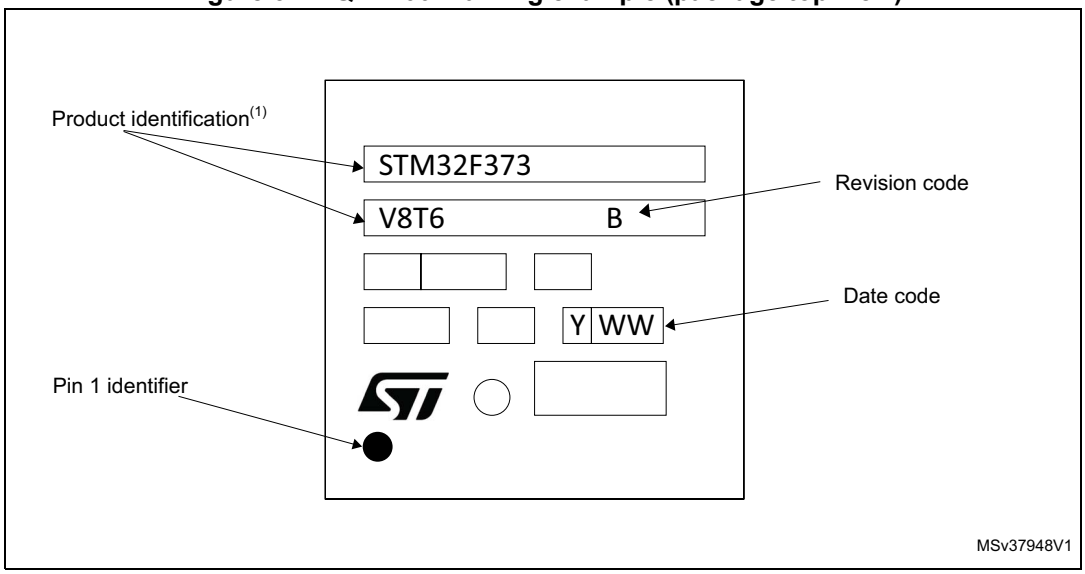


1. Dimensions are expressed in millimeters.

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

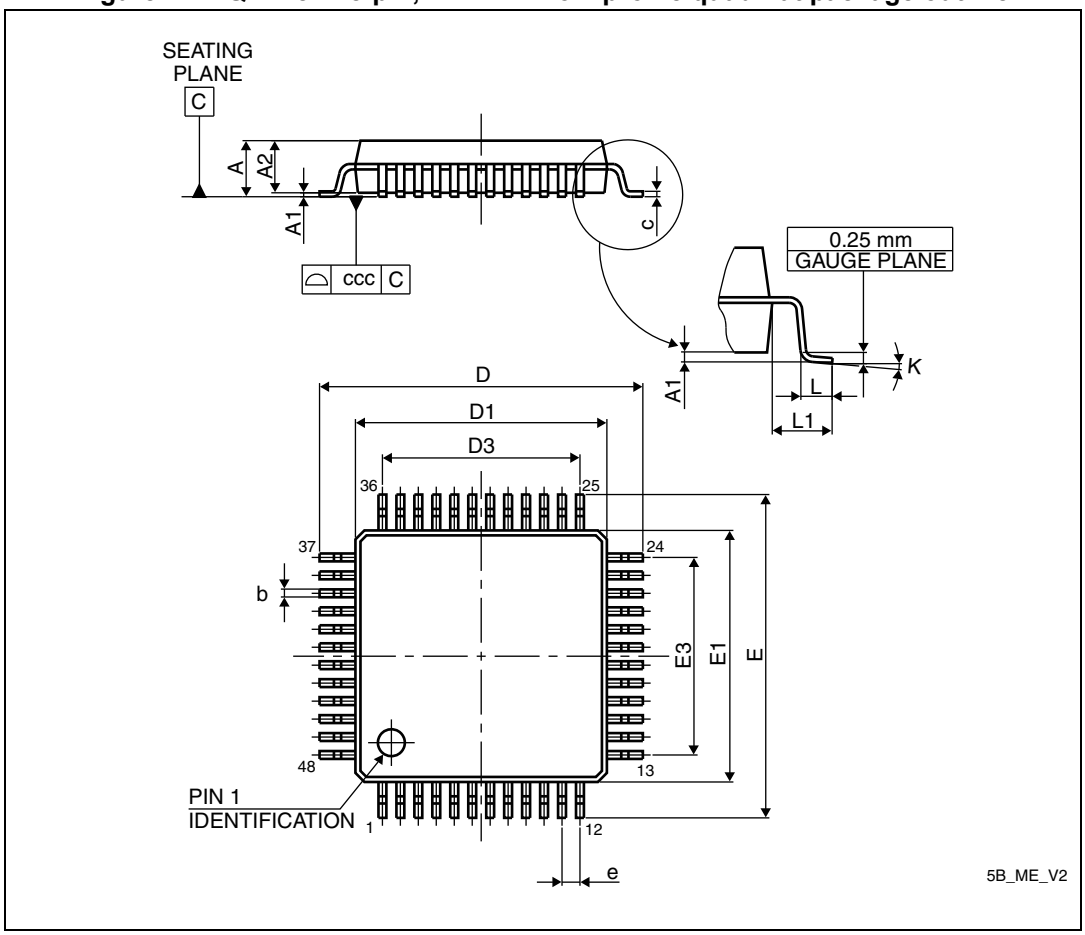
Figure 37. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 LQFP48 package information

Figure 41. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 82. Ordering information scheme

Example: STM32 F 373 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

373 = STM32F373xx

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Code size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel