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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 84 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 24K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 1x12b, 3x16b; D/A 3x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373vbt7 |

# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F373xx microcontrollers.

This STM32F373xx datasheet should be read in conjunction with the RM0313 reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 with FPU core, please refer to:

- Cortex®-M4 with FPU Technical Reference Manual, available from www.arm.com.
- STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

## 3.12 12-bit analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter is based on a successive approximation register (SAR) architecture. It has up to 16 external channels (AIN15:0) and 3 internal channels (temperature sensor, voltage reference, $V_{BAT}$ voltage measurement) performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers (TIMx) can be internally connected to the ADC start and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

### 3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See *Table 65: Temperature sensor calibration values on page 105*.

### 3.12.2 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and Comparators. $V_{REFINT}$ is internally connected to the ADC_IN17 input channel. The precise voltage of $V_{REFINT}$ is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

### 3.12.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the $V_{BAT}$ battery voltage using the internal ADC channel ADC_IN18. As the $V_{BAT}$ voltage may be higher than $V_{DDA}$, and thus outside the ADC input range, the $V_{BAT}$ pin is internally connected to a divider by 2. As a consequence, the converted digital value is half the $V_{BAT}$ voltage.

## 3.17 Timers and watchdogs

The STM32F373xx includes two 32-bit and nine 16-bit general-purpose timers, three basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

**Table 5. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| General-purpose | TIM2 TIM5 | 32-bit | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes | 4 | 0 |
| General-purpose | TIM3, TIM4, TIM19 | 16-bit | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes | 4 | 0 |
| General-purpose | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | 0 |
| General-purpose | TIM15 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | 1 |
| General-purpose | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | 0 |
| General-purpose | TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | 1 |
| Basic | TIM6, TIM7, TIM18 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | 0 |

**Table 12. Alternate functions for port PA**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA0 | - | TIM2_CH1_ETR | TIM5_CH1_ETR | TSC_G1_IO1 | - | - | - | USART2_CTS | COMP1_OUT | - | - | TIM19_CH1 | - | EVENTOUT |
| PA1 | RTC_REFIN | TIM2_CH2 | TIM5_CH2 | TSC_G1_IO2 | - | - | SPI3_SCK/I2S3_CK | USART2_RTS | - | TIM15_CH1N | - | TIM19_CH2 | - | EVENTOUT |
| PA2 | - | TIM2_CH3 | TIM5_CH3 | TSC_G1_IO3 | - | - | SPI3_MISO/I2S3_MCK | USART2_TX | COMP2_OUT | TIM15_CH1 | - | TIM19_CH3 | - | EVENTOUT |
| PA3 | - | TIM2_CH4 | TIM5_CH4 | TSC_G1_IO4 | - | - | SPI3_MOSI/I2S3_SD | USART2_RX | - | TIM15_CH2 | - | TIM19_CH4 | - | EVENTOUT |
| PA4 | - | - | TIM3_CH2 | TSC_G2_IO1 | - | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | USART2_CK | - | - | TIM12_CH1 | - | - | EVENTOUT |
| PA5 | - | TIM2_CH1_ETR | - | TSC_G2_IO2 | - | SPI1_SCK/I2S1_CK | - | CEC | - | TIM14_CH1 | TIM12_CH2 | - | - | EVENTOUT |
| PA6 | - | TIM16_CH1 | TIM3_CH1 | TSC_G2_IO3 | - | SPI1_MISO/I2S1_MCK | - | - | COMP1_OUT | TIM13_CH1 | - | - | - | EVENTOUT |
| PA7 | - | TIM17_CH1 | TIM3_CH2 | TSC_G2_IO4 | - | SPI1_MOSI/I2S1_SD | - | - | COMP2_OUT | TIM14_CH1 | - | - | - | EVENTOUT |
| PA8 | MCO | - | TIM5_CH1_ETR | - | I2C2_SMBA | SPI2_SCK/I2S2_CK | - | USART1_CK | - | - | TIM4_ETR | - | - | EVENTOUT |
| PA9 | - | - | TIM13_CH1 | TSC_G4_IO1 | I2C2_SCL | SPI2_MISO/I2S2_MCK | - | USART1_TX | - | TIM15_BKIN | TIM2_CH3 | - | - | EVENTOUT |
| PA10 | - | TIM17_BKIN | - | TSC_G4_IO2 | I2C2_SDA | SPI2_MOSI/I2S2_SD | - | USART1_RX | - | TIM14_CH1 | TIM2_CH4 | - | - | EVENTOUT |
| PA11 | - | - | TIM5_CH2 | - | - | SPI2_NSS/I2S2_WS | SPI1_NSS/I2S1_WS | USART1_CTS | COMP1_OUT | CAN_RX | TIM4_CH1 | - | - | EVENTOUT |
| PA12 | - | TIM16_CH1 | TIM5_CH3 | - | - | - | SPI1_SCK/I2S1_CK | USART1_RTS | COMP2_OUT | CAN_TX | TIM4_CH2 | - | - | EVENTOUT |

**Table 17. Alternate functions for port PF**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|
| PF0 | - | - | - | - | I2C2_SDA | - | - | - |
| PF1 | - | - | - | - | I2C2_SCL | - | - | - |
| PF2 | - | EVENTOUT | - | - | I2C2_SMBA | - | - | - |
| PF4 | - | EVENTOUT | - | - | - | - | - | - |
| PF6 | - | EVENTOUT | TIM4_CH4 | - | I2C2_SCL | SPI1_MOSI/I2S1_SD | - | USART3_RTS |
| PF7 | - | EVENTOUT | - | - | I2C2_SDA | - | - | USART2_CK |
| PF9 | - | EVENTOUT | TIM14_CH1 | - | - | - | - | - |
| PF10 | - | EVENTOUT | - | - | - | - | - | - |

### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 52: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC and SDADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode. Under reset conditions all I/Os are configured in input floating mode - so if some inputs do not have a defined voltage level then they can generate additional consumption. This consumption is visible on $V_{DD}$ supply and also on $V_{DDSDx}$ supply because some I/Os are powered from SDADCx supply (all I/Os which have SDADC analog input functionality).

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

$C_S$ is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

All timings are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22*.

**Table 37. Low-power mode wakeup timings**

| Symbol | Parameter | Conditions | Typ @$V_{DD}$ = $V_{DDA}$ | | | | | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | = 2.0 V | = 2.4 V | = 2.7 V | = 3 V | = 3.3 V | | |
| $t_{WUSTOP}$ | Wakeup from Stop mode | Regulator in run mode | 4.1 | 3.9 | 3.8 | 3.7 | 3.6 | 4.5 | µs |
| | | Regulator in low power mode | 7.9 | 6.7 | 6.1 | 5.7 | 5.4 | 8.6 | |
| $t_{WUSTANDBY}$ | Wakeup from Standby mode | LSI and IWDG off | 62.6 | 53.7 | 49.2 | 45.7 | 42.7 | 100 | |
| $t_{WUSLEEP}$ | Wakeup from Sleep mode | After WFE instruction | 6 | | | | | | CPU clock cycles |

## 6.3.7 External clock source characteristics

### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

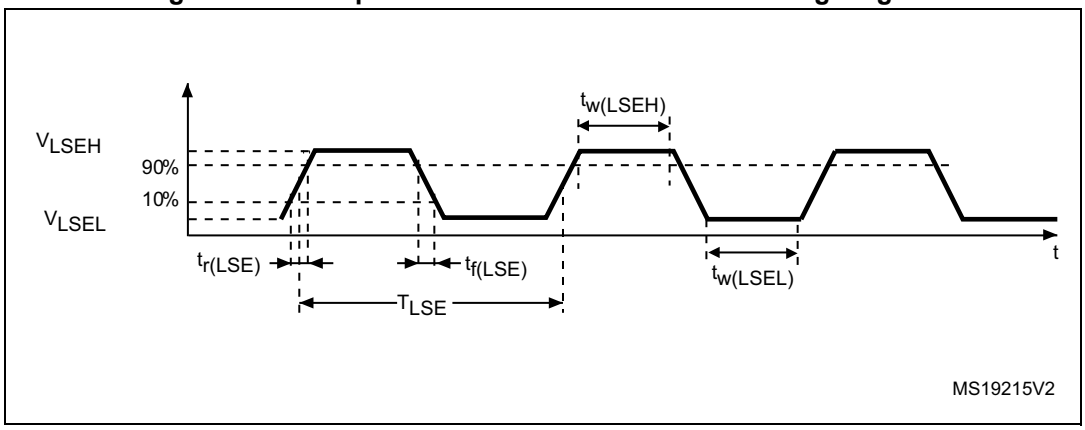
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 12*.

**Table 38. High-speed external user clock characteristics**

| Symbol | Parameter[1] | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency | CSS is on or PLL is used | 1 | 8 | 32 | MHz |
| | | CSS is off, PLL not used | 0 | | | |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | - | 0.7 $V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | - | $V_{SS}$ | - | 0.3 $V_{DD}$ | |
| $t_{w(HSEH)}$ $t_{w(HSEL)}$ | OSC_IN high or low time | - | 15 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time | - | - | - | 20 | |

1. Guaranteed by design.

**Figure 13. Low-speed external clock source AC timing diagram**




## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 40. HSE oscillator characteristics**

| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | - | 4 | 8 | 32 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| $I_{DD}$ | HSE current consumption | During startup(3) | - | - | 8.5 | mA |
| | | $V_{DD}$ = 3.3 V, Rm= 30 Ω, CL= 10 pF@8 MHz | - | 0.4 | - | |
| | | $V_{DD}$ = 3.3 V, Rm= 45 Ω, CL= 10 pF@8 MHz | - | 0.5 | - | |
| | | $V_{DD}$ = 3.3 V, Rm= 30 Ω, CL=5 pF@32 MHz | - | 0.8 | - | |
| | | $V_{DD}$ = 3.3 V, Rm= 30 Ω, CL= 10 pF@32 MHz | - | 1 | - | |
| | | $V_{DD}$ = 3.3 V, Rm= 30 Ω, CL= 20 pF@32 MHz | - | 1.5 | - | |
| $g_m$ | Oscillator transconductance | Startup | 10 | - | - | mA/V |
| $t_{SU(HSE)}$(4) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 50. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 51*.

*Note: I/O pins are powered from $V_{DD}$ voltage except pins which can be used as SDADC inputs:*

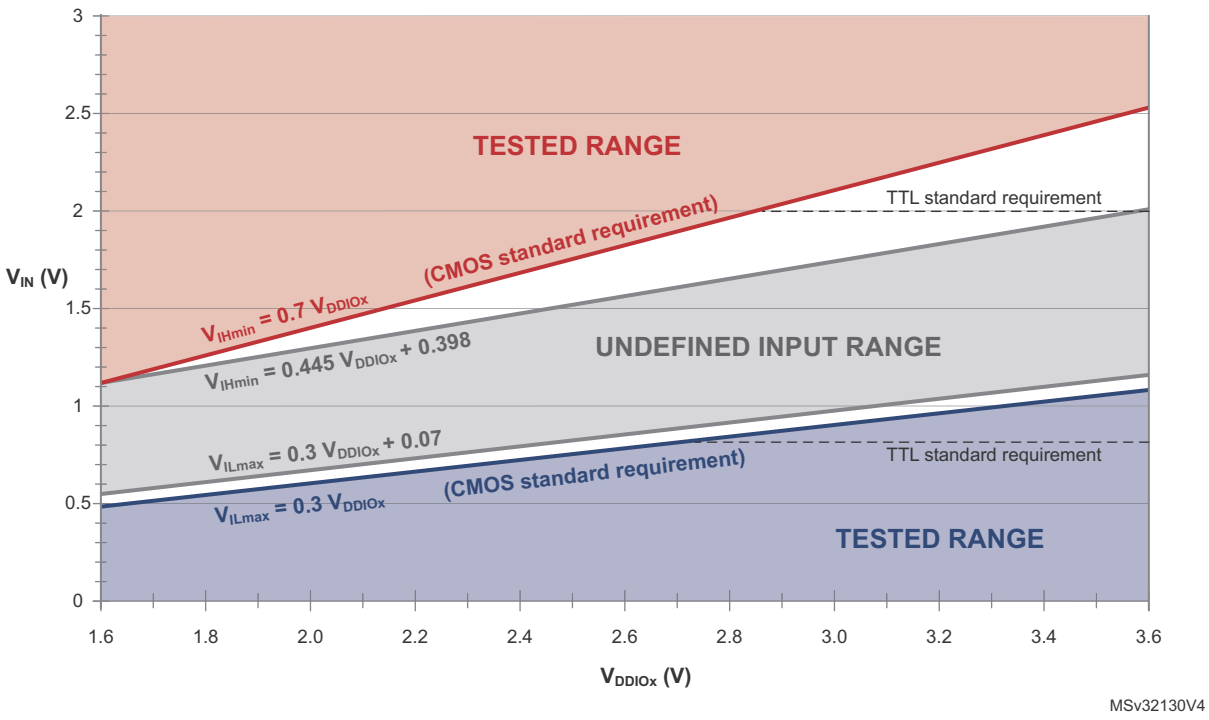
*- The PB2, PB10 and PE7 to PE15 I/O pins are powered from $V_{DDSD12}$.*

*- PB14 to PB15 and PD8 to PD15 I/O pins are powered from $V_{DDSD3}$. All I/O pin ground is internally connected to $V_{SS}$.*

*$V_{DD}$ mentioned in the Table 52 represents power voltage for a given I/O pin ($V_{DD}$ or $V_{DDSD12}$ or $V_{DDSD3}$).*

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 17* for standard I/Os, and in *Figure 18* for 5 V tolerant I/Os. The following curves are design simulation results, not tested in production.

**Figure 17. TC and TTa I/O input characteristics - CMOS port**



## SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 58* for SPI or in *Table 59* for I²S are derived from tests performed under ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

**Table 58. SPI characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ (1) | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 18 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ (1) | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 8 | ns |
| DuCy(SCK)(1) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$ (1) | NSS setup time | Slave mode | 2Tpclk | - | ns |
| $t_{h(NSS)}$ (1) | NSS hold time | Slave mode | 4Tpclk | - | |
| $t_{w(SCKH)}$ (1)<br>$t_{w(SCKL)}$ (1) | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | Tpclk/2 - 3 | Tpclk/2 + 3 | |
| $t_{su(MI)}$ (1)<br>$t_{su(SI)}$ (1) | Data input setup time | Master mode | 5.5 | - | |
| | | Slave mode | 6.5 | - | |
| $t_{h(MI)}$ (1) | Data input hold time | Master mode | 5 | - | |
| $t_{h(SI)}$ (1) | | Slave mode | 5 | - | |
| $t_{a(SO)}$ (1)(2) | Data output access time | Slave mode, $f_{PCLK}$ = 24 MHz | 0 | 4Tpclk | |
| $t_{dis(SO)}$ (1)(3) | Data output disable time | Slave mode | 0 | 24 | |
| $t_{v(SO)}$ (1) | Data output valid time | Slave mode (after enable edge) | - | 39 | |
| $t_{v(MO)}$ (1) | Data output valid time | Master mode (after enable edge) | - | 3 | |
| $t_{h(SO)}$ (1) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$ (1) | | Master mode (after enable edge) | 4 | - | |

1. Guaranteed by characterization results.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

**Figure 22. SPI timing diagram - slave mode and CPHA = 0**

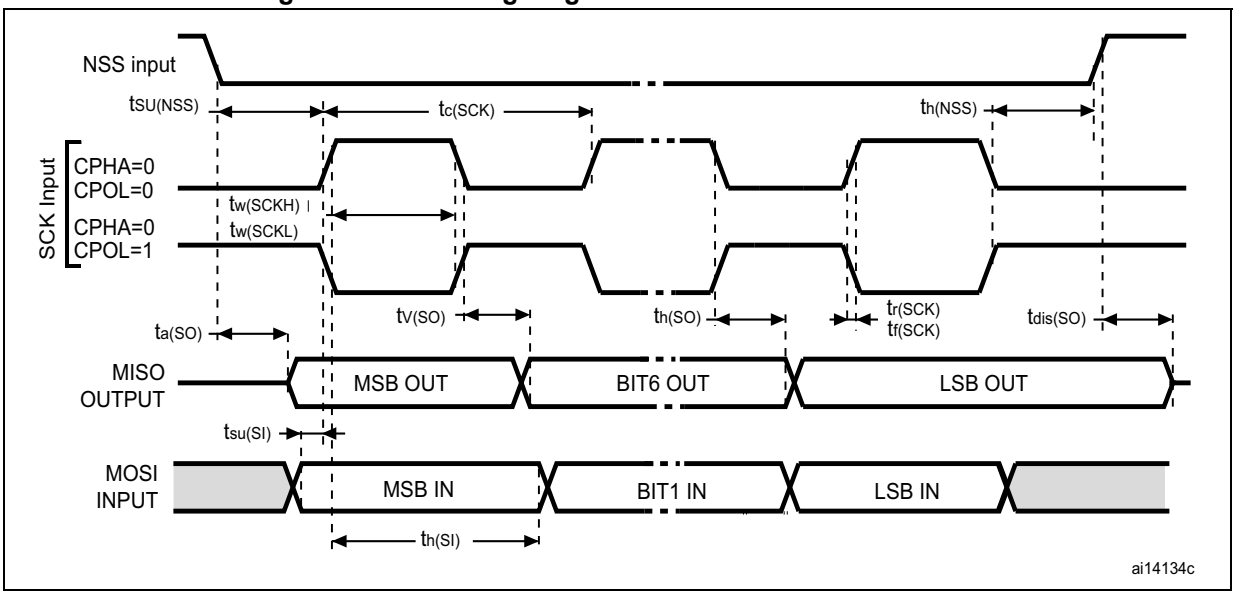
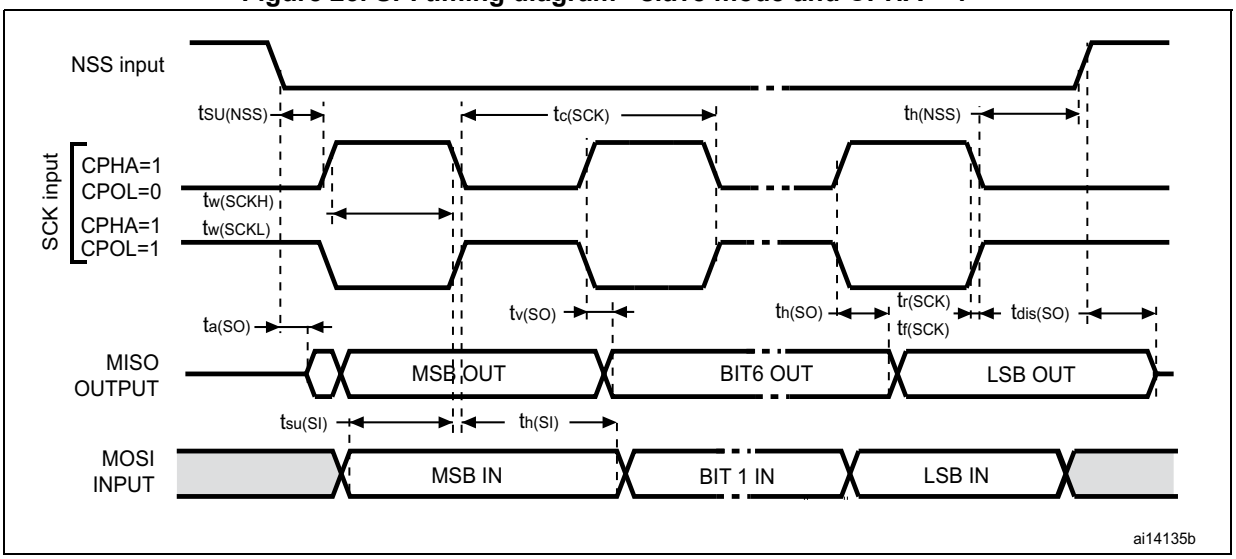



**Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at $0.5V_{DD}$ level and with external $C_L$ = 30 pF.

**Table 59. $I^2S$ characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| DuCy(SCK)(1) | I2S slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $f_{CK}$(1) $1/t_{c(CK)}$ | $I^2S$ clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | 1.528 | 1.539 | MHz |
| | | Slave mode | 0 | 12.288 | |
| $t_{r(CK)}$(1) $t_{f(CK)}$ | $I^2S$ clock rise and fall time | Capacitive load $C_L$ = 30 pF | - | 8 | ns |
| $t_{v(WS)}$ (1) | WS valid time | Master mode | 4 | - | |
| $t_{h(WS)}$ (1) | WS hold time | Master mode | 4 | - | |
| $t_{su(WS)}$ (1) | WS setup time | Slave mode | 2 | - | |
| $t_{h(WS)}$ (1) | WS hold time | Slave mode | - | - | |
| $t_{w(CKH)}$ (1) | I2S clock high time | Master $f_{PCLK}$= 16 MHz, audio frequency = 48 kHz | 306 | - | |
| $t_{w(CKL)}$ (1) | I2S clock low time | | 312 | - | |
| $t_{su(SD\_MR)}$ (1) | Data input setup time | Master receiver | 6 | - | |
| $t_{su(SD\_SR)}$ (1) | | Slave receiver | 3 | - | |
| $t_{h(SD\_MR)}$(1) | Data input hold time | Master receiver | 1.5 | - | |
| $t_{h(SD\_SR)}$ (1) | | Slave receiver | 1.5 | - | |
| $t_{v(SD\_ST)}$ (1) | Data output valid time | Slave transmitter (after enable edge) | - | 16 | |
| $t_{h(SD\_ST)}$ (1) | Data output hold time | Slave transmitter (after enable edge) | 16 | - | |
| $t_{v(SD\_MT)}$ (1) | Data output valid time | Master transmitter (after enable edge) | - | 2 | |
| $t_{h(SD\_MT)}$ (1) | Data output hold time | Master transmitter (after enable edge) | 0 | - | |

1. Guaranteed by characterization results.

**Equation 1: $R_{SRC}$ max formula**

$$R_{SRC} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external signal source impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 61. $R_{SRC}$ max for $f_{ADC}$ = 14 MHz(1)**

| $T_s$ (cycles) | $t_S$ (µs) | $R_{SRC}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | 50 |
| 239.5 | 17.1 | 50 |

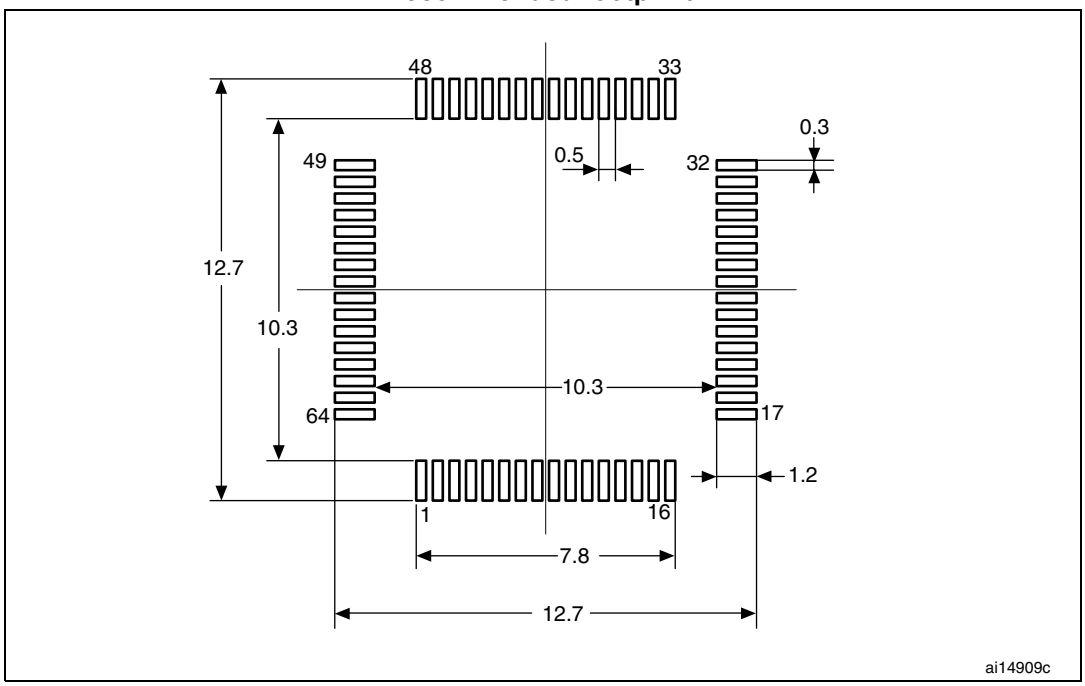
1. Guaranteed by design.

**Table 62. ADC accuracy(1)(2) (3)**

| Symbol | Parameter | Test conditions | Typ | Max(4) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ = 14 MHz, $R_{SRC}$ < 10 kΩ, $V_{DDA}$ = 3 V to 3.6 V, $T_A$ = 25 °C | ±1.3 | ±3 | LSB |
| EO | Offset error | | ±1 | ±2 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±0.7 | ±1 | |
| EL | Integral linearity error | | ±0.8 | ±1.5 | |
| ET | Total unadjusted error | $f_{ADC}$ = 14 MHz, $R_{SRC}$ < 10 kΩ, $V_{DDA}$ = 2.7 V to 3.6 V, $T_A$ = -40 to 105 °C | ±3.3 | ±4 | LSB |
| EO | Offset error | | ±1.9 | ±2.8 | |
| EG | Gain error | | ±2.8 | ±3 | |
| ED | Differential linearity error | | ±0.7 | ±1.3 | |
| EL | Integral linearity error | | ±1.2 | ±1.7 | |
| ET | Total unadjusted error | $f_{ADC}$ = 14 MHz, $R_{SRC}$ < 10 kΩ, $V_{DDA}$ = 2.4 V to 3.6 V, $T_A$ = 25 °C | ±3.3 | ±4 | LSB |
| EO | Offset error | | ±1.9 | ±2.8 | |
| EG | Gain error | | ±2.8 | ±3 | |
| ED | Differential linearity error | | ±0.7 | ±1.3 | |
| EL | Integral linearity error | | ±1.2 | ±1.7 | |

1. ADC DC accuracy values are measured after internal calibration.

**Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint**

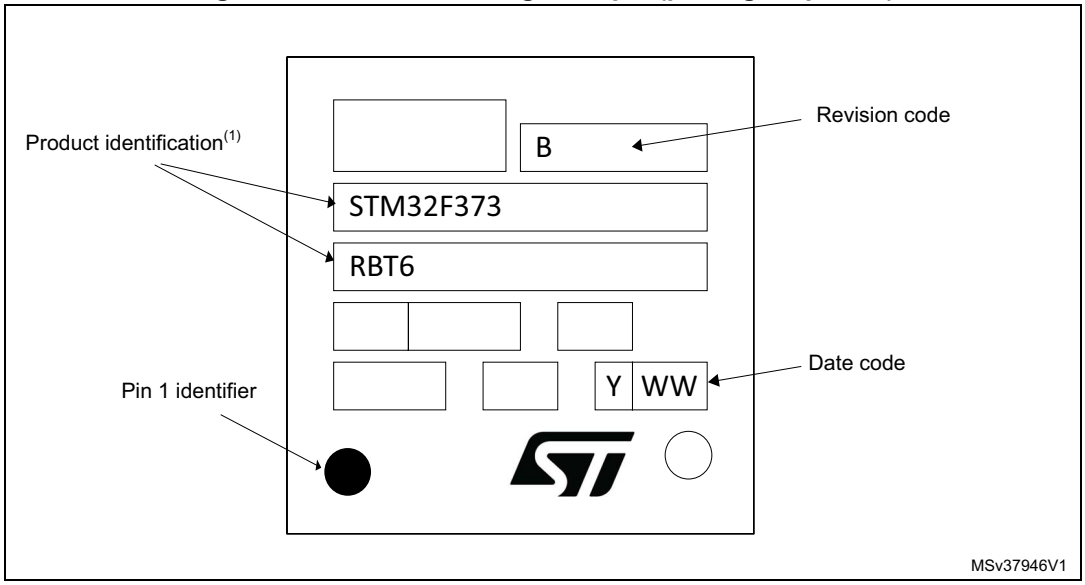



1. Dimensions are expressed in millimeters.

## Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 40. LQFP64 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

# 8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

**Table 82. Ordering information scheme**

**Example**: STM32 F 373 R 8 T 6 x

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = General-purpose

**Sub-family**

373 = STM32F373xx

**Pin count**

C = 48 pins

R = 64 pins

V = 100 pins

**Code size**

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

**Package**

T = LQFP

H = BGA

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

**Options**

xxx = programmed parts

TR = tape and reel

Table 83. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 21-Dec-2012 | 3 | Updated *Table 2: Device overview*, capacitive sensing channels peripheral added.<br>Updated *Table 3: Capacitive sensing GPIOs available on STM32F373xx devices*<br>Updated *Section 3.19: Inter-integrated circuit interface (I2C)*<br>Updated the function names in *Table 11: STM32F373 pin definitions*<br>Updated *Table 20: Current characteristics*<br>Updated *Table 22: General operating conditions*<br>Updated *Table 30: Typical and maximum VDD consumption in Stop and Standby modes*<br>Updated *Table 32: Typical and maximum current consumption from VBAT supply*<br>Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')*<br>Updated *Table 33: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 34: Typical current consumption in Sleep mode, code running from Flash or RAM*<br>Added *Table 35: Switching output I/O current consumption*<br>Added *Table 36: Peripheral current consumption*, *Figure 16: HSI oscillator accuracy characterization results*<br>Updated *Section 6.3.6: Wakeup time from low-power mode*<br>Updated *Table 37: Low-power mode wakeup timings*<br>Updated *Table 47: EMS characteristics*<br>Updated *Table 51: I/O current injection susceptibility*<br>Updated *Table 52: I/O static characteristics*<br>Updated , *Figure 18: TC and TTa I/O input characteristics - TTL port*, *Figure 18: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port* and *Figure 20: Five volt tolerant (FT and FTf) I/O input characteristics - TTL port*<br>Updated *Table 53: Output voltage characteristics*<br>Updated *Table 54: I/O AC characteristics*<br>Updated *Table 55: NRST pin characteristics*<br>Updated *Table 63: DAC characteristics*<br>Updated *Table 74: SDADC characteristics*<br>Updated *Figure 32: LQFP100 –14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 35: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Figure 38: LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline*<br>Updated *Table 72: LQPF100 – 14 x 14 mm low-profile quad flat package mechanical data*, *Table 73: LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data* and *Table 74: LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data*<br>Added *Figure 16: HSI oscillator accuracy characterization results* |

Table 83. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 19-Sep-2013 | 4 | Replaced “Cortex-M4F” with “Cortex-M4” throughout the document.<br>Removed part number STM32F372xx.<br>Added “1.25 DMIPS/MHz (Dhrystone 2.1)” in *Features*.<br>Updated *Introduction*.<br>Added reference to the STMTouch touch sensing firmware library in *Section 3.16: Touch sensing controller (TSC)*.<br>Added “All I2S interfaces can operate in half-duplex mode only.” in *Section 3.21: Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)*.<br>Added row “I2S full-duplex mode” to *Table 9: STM32F373xx SPI/I2S implementation*.<br>Modified introduction of *I2C interface characteristics*.<br>Added alternate function RTC_REFIN and removed additional function RTC_REF_CLK_IN to pins PA1 and PB15.<br>Replaced alternate function JNTRST with NJTRST for pin PB4.<br>In *Table 12: Alternate functions for port PA*: replaced alternate function JTMS-SWDIO with SWDIO-JTMS for pin PA13, and JTCK-SWCLK with SWCLK-JTCK for pin PA14.<br>Added rows $V_{REF+}$ and $V_{REFSD+}$ to *Table 22: General operating conditions*.<br>Replaced "$f_{APB1} = f_{AHB/2}$" with "$f_{APB1} = f_{AHB}$" for “When the peripherals are enabled...” in *Typical current consumption*.<br>Added COMP in *Table 36: Peripheral current consumption*<br>Added conditions for $f_{HSE\_ext}$ in *Table 38: High-speed external user clock characteristics*.<br>Added Min and Max values for $ACC_{HSI}$ in *Table 42: HSI oscillator characteristics*.<br>Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in *Table 49: ESD absolute maximum ratings*.<br>Removed pins PB0 and PB1 in description of $I_{INJ}$ in *Table 51: I/O current injection susceptibility*.<br>Updated *Table 56: I2C characteristics*.<br>Replaced all occurrences of “gain/2” with “gain*2” in *Table 74: SDADC characteristics*.<br>Corrected typo in *Figure 19: I/O AC characteristics definition*.<br>Replaced *Figure 21: I2C bus AC waveforms and measurement circuit*..<br>Added $I_{DDA(ADC)}$ and footnote 1 in *Table 60: ADC characteristics* |