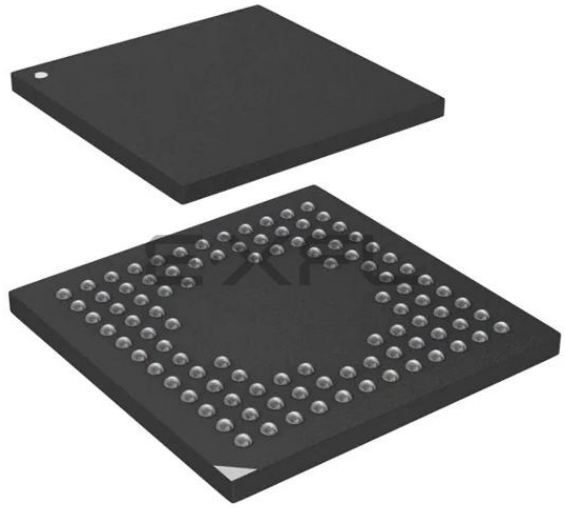

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 84 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 1x12b, 3x16b; D/A 3x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-UFBGA |
| Supplier Device Package | 100-UFBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373vch7 |

## 3.13 16-bit sigma delta analog-to-digital converters (SDADC)

Three 16-bit sigma-delta analog-to-digital converters are embedded in the STM32F373xx. They have up to two separate supply voltages allowing the analog function voltage range to be independent from the STM32F373xx power supply. They share up to 21 input pins which may be configured in any combination of single-ended (up to 21) or differential inputs (up to 11).

The conversion speed is up to 16.6 ksps for each SDADC when converting multiple channels and up to 50 ksps per SDADC if single channel conversion is used. There are two conversion modes: single conversion mode or continuous mode, capable of automatically scanning any number of channels. The data can be automatically stored in a system RAM buffer, reducing the software overhead.

A timer triggering system can be used in order to control the start of conversion of the three SDADCs and/or the 12-bit fast ADC. This timing control is very flexible, capable of triggering simultaneous conversions or inserting a programmable delay between the ADCs.

Up to two external reference pins (VREFSD+, VREFSD-) and an internal 1.2/1.8 V reference can be used in conjunction with a programmable gain (x0.5 to x32) in order to fine-tune the input voltage range of the SDADC. VREFSD - pin is used as negative signal reference in case of single-ended input mode.

## 3.14 Digital-to-analog converter (DAC)

The devices feature two 12-bit buffered DACs with three output channels that can be used to convert three digital signals into three analog voltage signal outputs. The internal structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital Interface supports the following features:

- Two DAC converters with three output channels:
  - DAC1 with two output channels
  - DAC2 with one output channel.
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation (DAC1 only)
- Triangular wave generation (DAC1 only)
- Dual DAC channel independent or simultaneous conversions (DAC1 only)
- DMA capability for each channel
- External triggers for conversion

### 3.17.3 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.17.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB1 clock (PCLK1) derived from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.17.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

## 3.18 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either from $V_{DD}$ supply when present or through the $V_{BAT}$ pin. The backup registers are thirty two 32-bit registers used to store 128 bytes of user application data.

They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28th, 29th (leap year), 30th and 31st day of the month.
- 2 programmable alarms with wake up from Stop and Standby mode capability.
- Periodic wakeup unit with programmable resolution and period.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 3 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

Table 11. STM32F373xx pin definitions (continued)

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | UFBGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 25 | K3 | 16 | 12 | PA2 | I/O | TTa | - | COMP2_OUT, SPI3_MISO/I2S3_MCK, USART2_TX, TIM2_CH3, TIM15_CH1, TIM5_CH3, TIM19_CH3, TSC_G1_IO3 | ADC_IN2, COMP2_INM |
| 26 | L3 | 18 | 13 | PA3 | I/O | TTa | - | SPI3_MOSI/I2S3_SD, USART2_RX, TIM2_CH4, TIM15_CH2, TIM5_CH4, TIM19_CH4, TSC_G1_IO4 | ADC_IN3, COMP2_INP |
| 27 | E3 | - | - | PF4 | I/O | FT | (2) | - | |
| 28 | H3 | 19 | 17 | VDD_2 | S | - | - | Digital power supply | |
| 29 | M3 | 20 | 14 | PA4 | I/O | TTa | - | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, TIM3_CH2, TIM12_CH1, TSC_G2_IO1, | ADC_IN4, DAC1_OUT1 |
| 30 | K4 | 21 | 15 | PA5 | I/O | TTa | - | SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, TIM14_CH1, TIM12_CH2, TSC_G2_IO2 | ADC_IN5, DAC1_OUT2 |
| 31 | L4 | 22 | 16 | PA6 | I/O | TTa | - | SPI1_MISO/I2S1_MCK, COMP1_OUT, TIM3_CH1, TIM13_CH1, TIM16_CH1, TSC_G2_IO3 | ADC_IN6, DAC2_OUT1, |
| 32 | M4 | 23 | - | PA7 | I/O | TTa | (2) | TSC_G2_IO4, TIM14_CH1, SPI1_MOSI/I2S1_SD, TIM17_CH1, TIM3_CH2, COMP2_OUT | ADC_IN7 |
| 33 | K5 | 24 | - | PC4 | I/O | TTa | (2) | TIM13_CH1, TSC_G3_IO1, USART1_TX | ADC_IN14 |
| 34 | L5 | 25 | - | PC5 | I/O | TTa | (2) | TSC_G3_IO2, USART1_RX | ADC_IN15 |
| 35 | M5 | 26 | 18 | PB0 | I/O | TTa | - | SPI1_MOSI/I2S1_SD, TIM3_CH3, TSC_G3_IO3, TIM3_CH2 | ADC_IN8, SDADC1_AIN6P |
| 36 | M6 | 27 | 19 | PB1 | I/O | TTa | - | TIM3_CH4, TSC_G3_IO4 | ADC_IN9, SDADC1_AIN5P, SDADC1_AIN6M |
| 37 | L6 | 28 | 20 | PB2 | I/O | TC | (3) | - | SDADC1_AIN4P, SDADC2_AIN6P |

Table 18. STM32F373xx peripheral register boundary addresses(1) (continued)

| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| APB1 | 0x4000 5800 - 0x4000 5BFF | 1 KB | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | 1 KB | I2C1 |
| | 0x4000 4C00 - 0x4000 53FF | 2 KB | Reserved |
| | 0x4000 4800 - 0x4000 4BFF | 1 KB | USART3 |
| | 0x4000 4400 - 0x4000 47FF | 1 KB | USART2 |
| | 0x4000 4000 - 0x4000 43FF | 1 KB | Reserved |
| | 0x4000 3C00 - 0x4000 3FFF | 1 KB | SPI3/I2S3 |
| | 0x4000 3800 - 0x4000 3BFF | 1 KB | SPI2/I2S2 |
| | 0x4000 3400 - 0x4000 37FF | 1 KB | Reserved |
| | 0x4000 3000 - 0x4000 33FF | 1 KB | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | 1 KB | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | 1 KB | RTC |
| | 0x4000 2400 - 0x4000 27FF | 1 KB | Reserved |
| | 0x4000 2000 - 0x4000 23FF | 1 KB | TIM14 |
| | 0x4000 1C00 - 0x4000 1FFF | 1 KB | TIM13 |
| | 0x4000 1800 - 0x4000 1BFF | 1 KB | TIM12 |
| | 0x4000 1400 - 0x4000 17FF | 1 KB | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | 1 KB | TIM6 |
| | 0x4000 0C00 - 0x4000 0FFF | 1 KB | TIM5 |
| | 0x4000 0800 - 0x4000 0BFF | 1 KB | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | 1 KB | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | 1 KB | TIM2 |

1. Cells in gray indicate Reserved memory locations.

## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 19. Voltage characteristics(1)**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$, $V_{DDSDx}$, $V_{BAT}$ and $V_{DD}$) | - 0.3 | 4.0 | V |
| $V_{DD}$–$V_{DDA}$ | Allowed voltage difference for $V_{DD}$ > $V_{DDA}$ | - | 0.4 | |
| $V_{DDSDx}$ – $V_{DDA}$ | Allowed voltage difference for $V_{DDSDx}$ > $V_{DDA}$ | - | 0.4 | |
| $V_{REFSD+}$ – $V_{DDSD3}$ | Allowed voltage difference for $V_{REFSD+}$ > $V_{DDSD3}$ | - | 0.4 | |
| $V_{REF+}$ – $V_{DDA}$ | Allowed voltage difference for $V_{REF+}$ > $V_{DDA}$ | - | 0.4 | |
| $V_{IN}$(2) | Input voltage on FT and FTf pins | $V_{SS}$ - 0.3 | $V_{DD}$ + 4.0 | |
| | Input voltage on TTa pins | $V_{SS}$ - 0.3 | 4.0 | |
| | Input voltage on TC pins on SDADCx channels inputs(3) | $V_{SS}$ - 0.3 | 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ - 0.3 | 4.0 | |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins | - | 50 | mV |
| $\lvert V_{REFSD-} - V_{SSx}\rvert$ | | - | 50 | mV |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.12: Electrical sensitivity characteristics* | | - |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (I/O ground pin is internally connected to $V_{SS}$). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (I/O ground pin is internally connected to $V_{SS}$).

All main power ($V_{DD}$, $V_{DDSD12}$, $V_{DDSD3}$ and $V_{DDA}$) and ground ($V_{SS}$, $V_{SSSD}$, and $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.

The following relationship must be respected between $V_{DDA}$ and $V_{DD}$: $V_{DDA}$ must power on before or at the same time as $V_{DD}$ in the power up sequence. $V_{DDA}$ must be greater than or equal to $V_{DD}$.

The following relationship must be respected between $V_{DDA}$ and $V_{DDSD12}$: $V_{DDA}$ must power on before or at the same time as $V_{DDSD12}$ or $V_{DDSD3}$ in the power up sequence. $V_{DDA}$ must be greater than or equal to $V_{DDSD12}$ or $V_{DDSD3}$.

The following relationship must be respected between $V_{DDSD12}$ and $V_{DDSD3}$: $V_{DDSD3}$ must power on before or at the same time as $V_{DDSD12}$ in the power up sequence.
After power up ($V_{DDSD12}$ > Vrefint = 1.2 V) $V_{DDSD3}$ can be higher or lower than $V_{DDSD12}$.

**Table 31. Typical and maximum $V_{DDA}$ consumption in Stop and Standby modes**

| Symbol | Parameter | Conditions | | Typ@$V_{DD}$ ($V_{DD}$=$V_{DDA}$) | | | | | | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | $T_A$= 25 °C | $T_A$= 85 °C | $T_A$= 105 °C | |
| $I_{DDA}$ | Supply current in Stop mode | $V_{DDA}$ and $V_{DDSD12}$ | Regulator in run mode, all oscillators OFF | 1.99 | 2.07 | 2.19 | 2.33 | 2.46 | 2.64 | 10.8 | 11.8 | 12.4 | µA |
| | | | Regulator in low-power mode, all oscillators OFF | 1.99 | 2.07 | 2.18 | 2.32 | 2.47 | 2.63 | 10.6 | 11.5 | 12.5 | |
| | Supply current in Standby mode | | LSI ON and IWDG ON | 2.44 | 2.53 | 2.7 | 2.89 | 3.09 | 3.33 | - | - | - | |
| | | | LSI OFF and IWDG OFF | 1.87 | 1.94 | 2.06 | 2.19 | 2.35 | 2.51 | 4.1 | 4.5 | 4.8 | |
| IDDAmon | Supply current for $V_{DDA}$ and $V_{DDSD12}$ monitoring | - | | 0.95 | 1.02 | 1.12 | 1.2 | 1.27 | 1.4 | - | - | - | |

1. Data based on characterization results and tested in production.
2. To obtain data with monitoring OFF is necessary to substract the IDDAmon current.

**Table 32. Typical and maximum current consumption from $V_{BAT}$ supply(1)**

| Symbol | Parameter | Conditions | Typ @ $V_{BAT}$ | | | | | | | Max(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | = 1.65 V | = 1.8 V | = 2.0 V | = 2.4 V | = 2.7 V | = 3.3 V | = 3.6 V | $T_A$= 25 °C | $T_A$= 85 °C | $T_A$= 105 °C | |
| $I_{DD\_VBAT}$ | Backup domain supply current | LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00' | 0.50 | 0.52 | 0.55 | 0.63 | 0.70 | 0.87 | 0.95 | 1.1 | 1.6 | 2.2 | µA |
| | | LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11' | 0.85 | 0.90 | 0.93 | 1.02 | 1.10 | 1.27 | 1.38 | 1.6 | 2.4 | 3.0 | |

1. Crystal used: Abracon ABS07-120-32.768kHz-T with 6 pF of CL for typical values.
2. Guaranteed by characterization results.

### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 52: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC and SDADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode. Under reset conditions all I/Os are configured in input floating mode - so if some inputs do not have a defined voltage level then they can generate additional consumption. This consumption is visible on $V_{DD}$ supply and also on $V_{DDSDx}$ supply because some I/Os are powered from SDADCx supply (all I/Os which have SDADC analog input functionality).

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

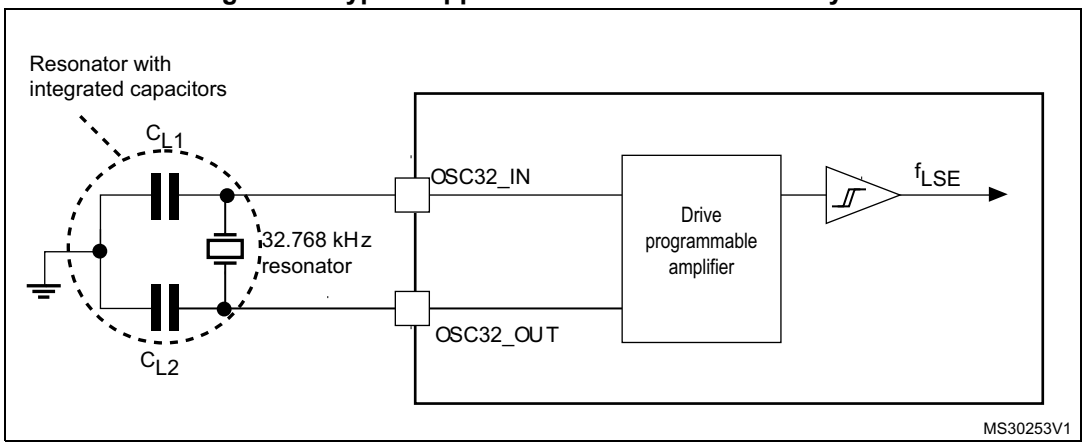
$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

$C_S$ is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Figure 15. Typical application with a 32.768 kHz crystal**




*Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

## 6.3.8 Internal clock source characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

The provided curves are characterization results, not tested in production.

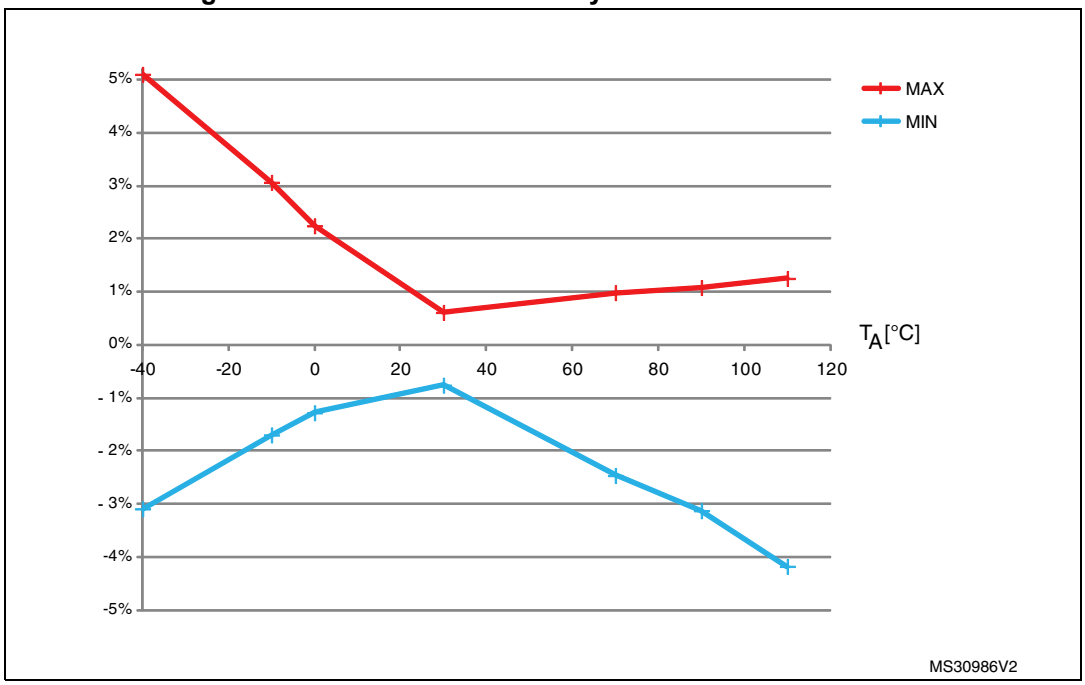
### High-speed internal (HSI) RC oscillator

**Table 42. HSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 8 | - | MHz |
| TRIM | HSI user trimming step | - | - | - | 1(2) | % |
| $DuCy_{(HSI)}$ | Duty cycle | - | 45(2) | - | 55(2) | % |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator (factory calibrated) | $T_A$ = –40 to 105 °C | –3.8(3) | - | 4.6(3) | % |
| | | $T_A$ = –10 to 85 °C | –2.9(3) | - | 2.9(3) | % |
| | | $T_A$ = 0 to 70 °C | –2.3(3) | - | –2.2(3) | % |
| | | $T_A$ = 25 °C | –1 | - | 1 | % |
| $t_{su(HSI)}$ | HSI oscillator startup time | - | 1(3) | - | 2(3) | µs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | - | - | 80 | 100(3) | µA |

1. $V_{DDA}$ =3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Figure 16. HSI oscillator accuracy characterization results




### Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics(1)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$ | Frequency | 30 | 40 | 60 | kHz |
| $t_{su(LSI)}$(2) | LSI oscillator startup time | - | - | 85 | µs |
| $I_{DD(LSI)}$(2) | LSI oscillator power consumption | - | 0.75 | 1.2 | µA |

1. $V_{DDA}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.

## 6.3.9 PLL characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 44. PLL characteristics

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $f_{PLL\_IN}$ | PLL input clock(1) | 1(2) | - | 24(2) | MHz |
| | PLL input clock duty cycle | 40(2) | - | 60(2) | % |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | 16(2) | - | 72 | MHz |
| $t_{LOCK}$ | PLL lock time | - | - | 200(2) | µs |
| Jitter | Cycle-to-cycle jitter | - | - | 300(2) | ps |

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL\_OUT}$.
2. Guaranteed by design.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 48. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/72 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ - 3.3 V, $T_A$ - 25 °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | 9 | dBµV |
| | | | 30 to 130 MHz | 26 | |
| | | | 130 MHz to 1 GHz | 30 | |
| | | | SAE EMI Level | 4 | - |

## 6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 49. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to ANSI/ESD STM5.3.1, LQFP100, LQFP64, LQFP48 and UFBGA100 packages | II | 500 | |

1. Guaranteed by characterization results.

*Note: I/O pins are powered from $V_{DD}$ voltage except pins which can be used as SDADC inputs:*

*- The PB2, PB10 and PE7 to PE15 I/O pins are powered from $V_{DDSD12}$.*

*- PB14 to PB15 and PD8 to PD15 I/O pins are powered from $V_{DDSD3}$. All I/O pin ground is internally connected to $V_{SS}$.*

*$V_{DD}$ mentioned in the Table 52 represents power voltage for a given I/O pin ($V_{DD}$ or $V_{DDSD12}$ or $V_{DDSD3}$).*

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 17* for standard I/Os, and in *Figure 18* for 5 V tolerant I/Os. The following curves are design simulation results, not tested in production.

**Figure 17. TC and TTa I/O input characteristics - CMOS port**

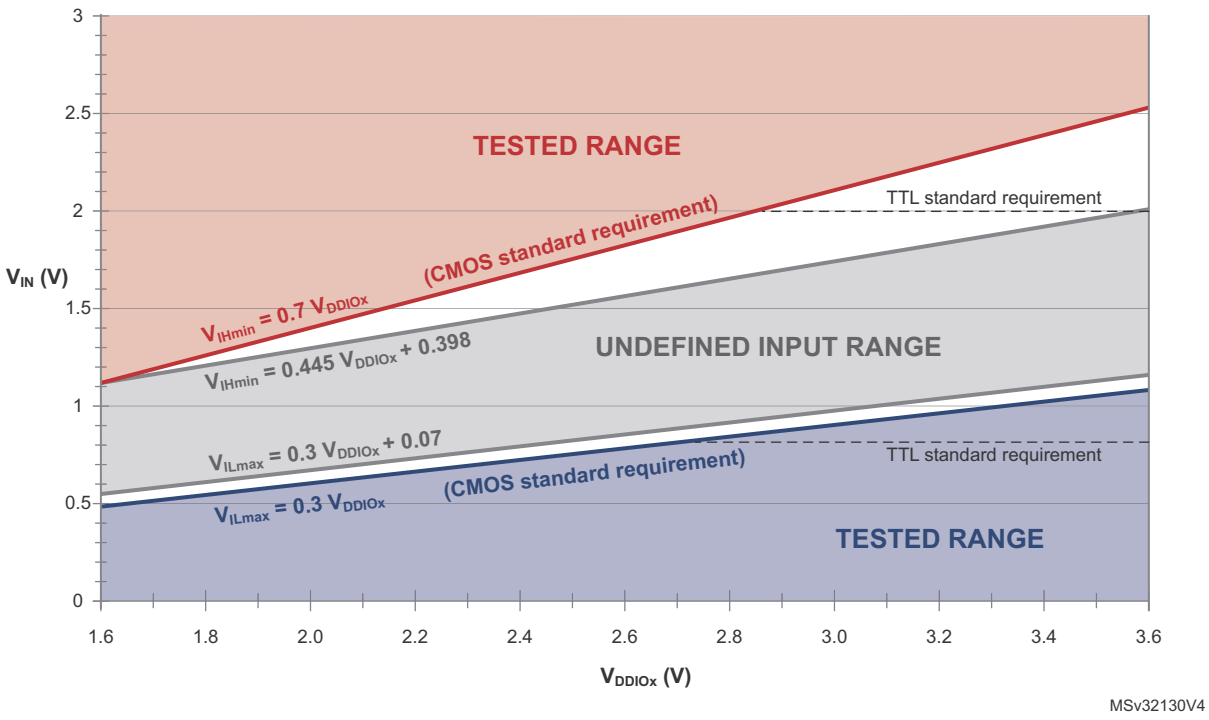


**Figure 22. SPI timing diagram - slave mode and CPHA = 0**

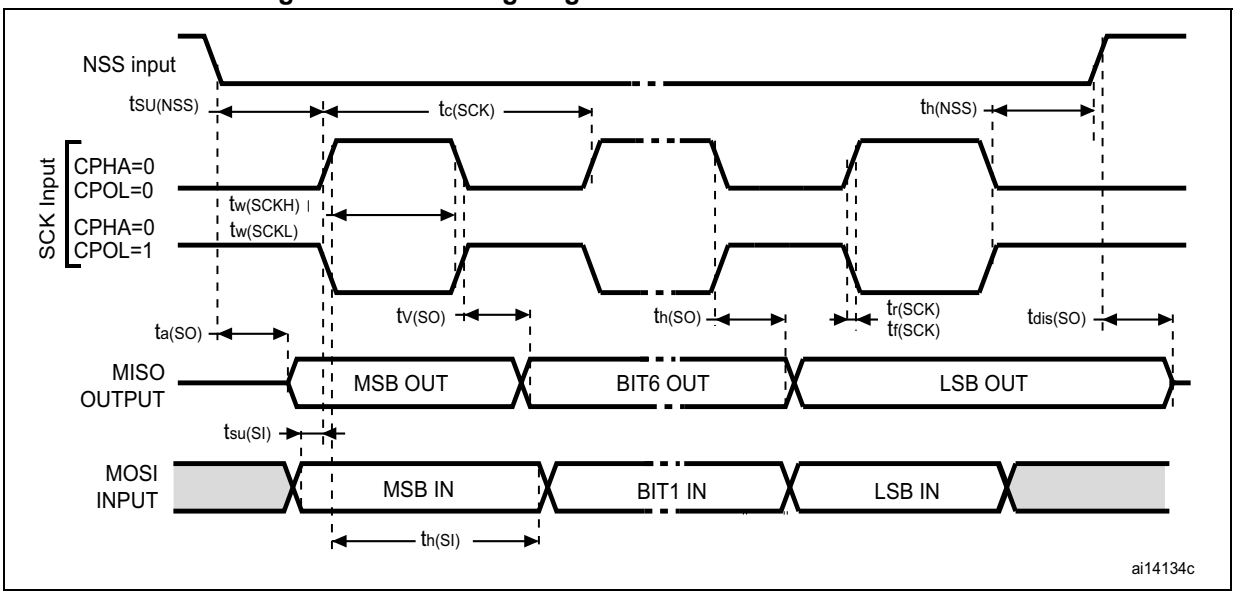
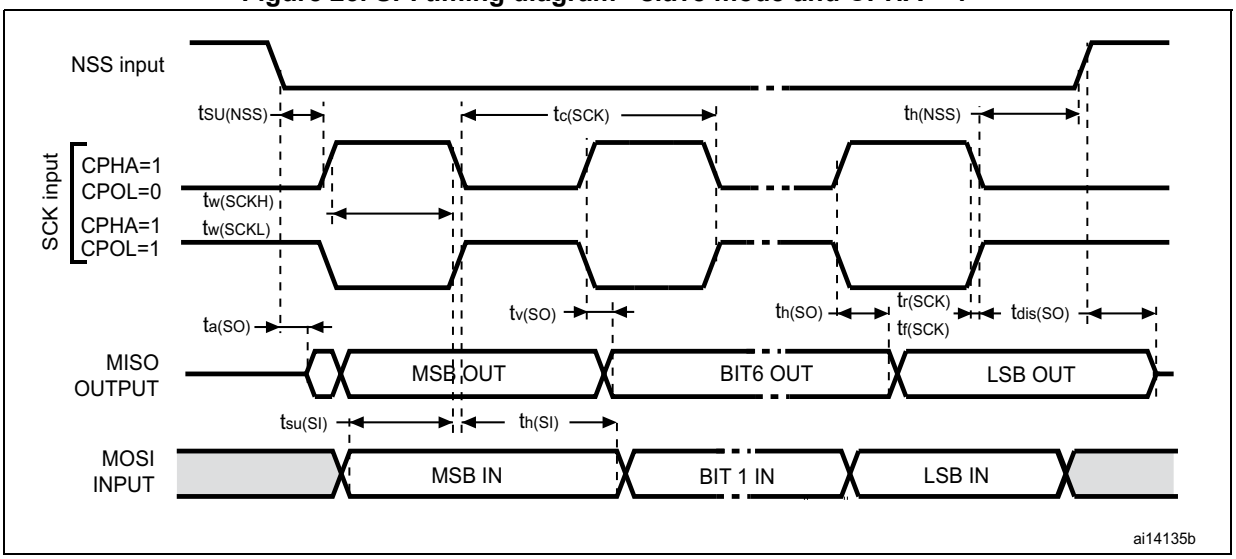



**Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)**



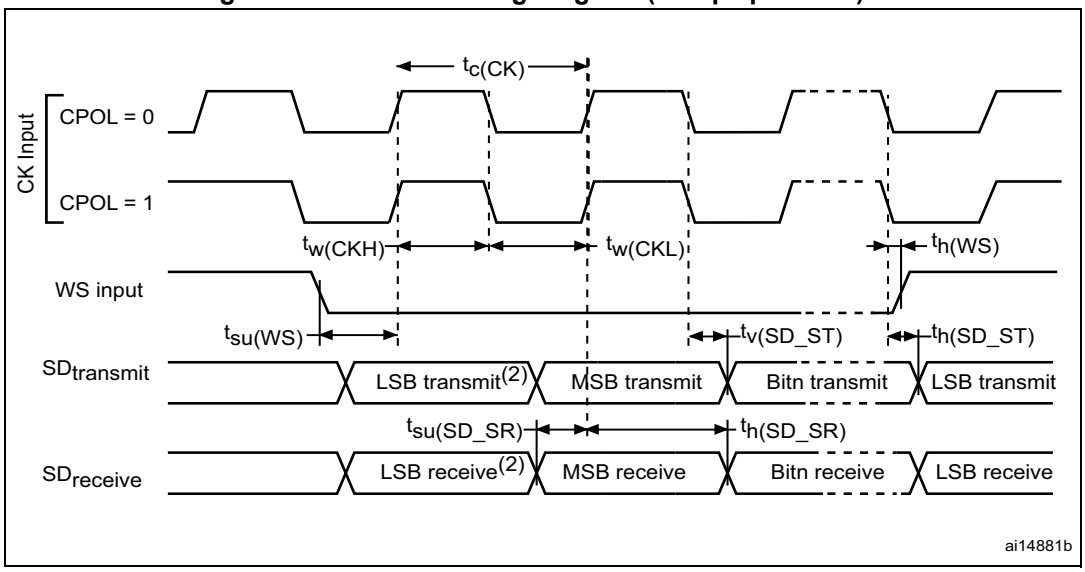

1. Measurement points are done at $0.5V_{DD}$ level and with external $C_L$ = 30 pF.

**Table 59. $I^2S$ characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| DuCy(SCK)(1) | I2S slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $f_{CK}$(1) $1/t_{c(CK)}$ | $I^2S$ clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | 1.528 | 1.539 | MHz |
| | | Slave mode | 0 | 12.288 | |
| $t_{r(CK)}$(1) $t_{f(CK)}$ | $I^2S$ clock rise and fall time | Capacitive load $C_L$ = 30 pF | - | 8 | ns |
| $t_{v(WS)}$ (1) | WS valid time | Master mode | 4 | - | |
| $t_{h(WS)}$ (1) | WS hold time | Master mode | 4 | - | |
| $t_{su(WS)}$ (1) | WS setup time | Slave mode | 2 | - | |
| $t_{h(WS)}$ (1) | WS hold time | Slave mode | - | - | |
| $t_{w(CKH)}$ (1) | I2S clock high time | Master $f_{PCLK}$= 16 MHz, audio frequency = 48 kHz | 306 | - | |
| $t_{w(CKL)}$ (1) | I2S clock low time | | 312 | - | |
| $t_{su(SD\_MR)}$ (1) | Data input setup time | Master receiver | 6 | - | |
| $t_{su(SD\_SR)}$ (1) | | Slave receiver | 3 | - | |
| $t_{h(SD\_MR)}$(1) | Data input hold time | Master receiver | 1.5 | - | |
| $t_{h(SD\_SR)}$ (1) | | Slave receiver | 1.5 | - | |
| $t_{v(SD\_ST)}$ (1) | Data output valid time | Slave transmitter (after enable edge) | - | 16 | |
| $t_{h(SD\_ST)}$ (1) | Data output hold time | Slave transmitter (after enable edge) | 16 | - | |
| $t_{v(SD\_MT)}$ (1) | Data output valid time | Master transmitter (after enable edge) | - | 2 | |
| $t_{h(SD\_MT)}$ (1) | Data output hold time | Master transmitter (after enable edge) | 0 | - | |

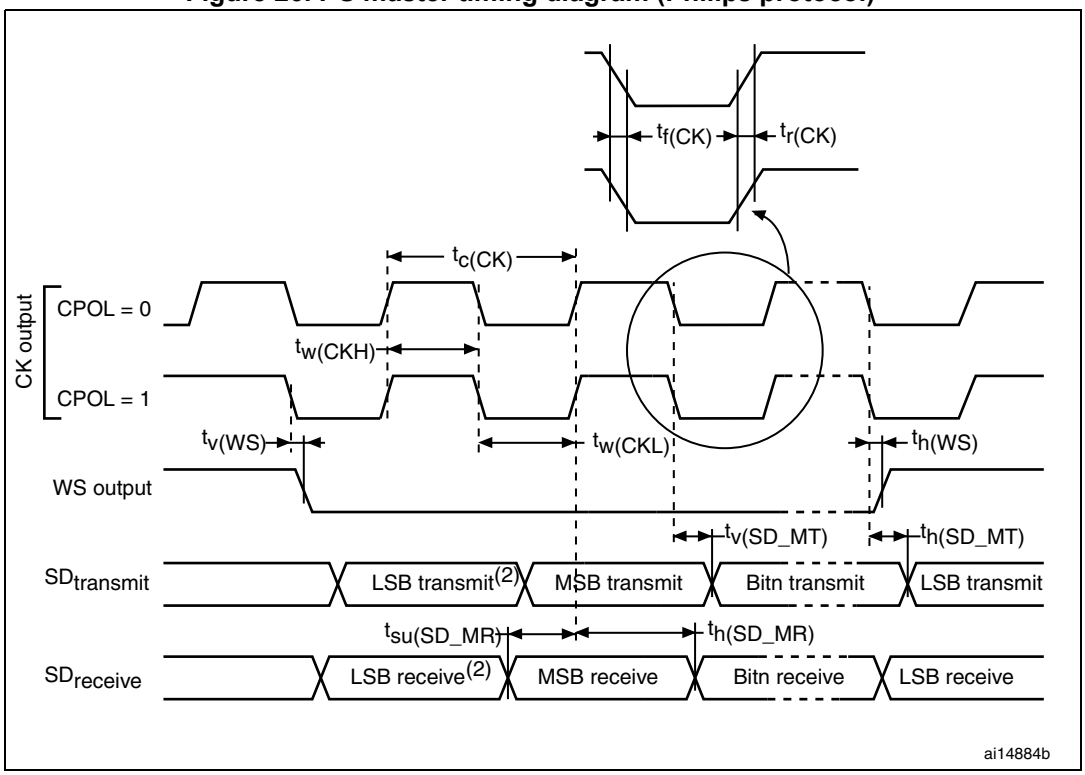
1. Guaranteed by characterization results.

**Figure 25. I²S slave timing diagram (Philips protocol)(1)**




1. Measurement points are done at 0.5 $V_{DD}$ level and with external $C_L$ = 30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 26. I²S master timing diagram (Philips protocol)(1)**




1. Measurement points are done at 0.5 $V_{DD}$ level and with external $C_L$ = 30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Table 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| D | 6.950 | 7.000 | 7.050 | 0.2736 | 0.2756 | 0.2776 |
| D1 | 5.450 | 5.500 | 5.550 | 0.2146 | 0.2165 | 0.2185 |
| E | 6.950 | 7.000 | 7.050 | 0.2736 | 0.2756 | 0.2776 |
| E1 | 5.450 | 5.500 | 5.550 | 0.2146 | 0.2165 | 0.2185 |
| e | - | 0.500 | - | - | 0.0197 | - |
| F | 0.700 | 0.750 | 0.800 | 0.0276 | 0.0295 | 0.0315 |
| ddd | - | - | 0.100 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 33. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint**

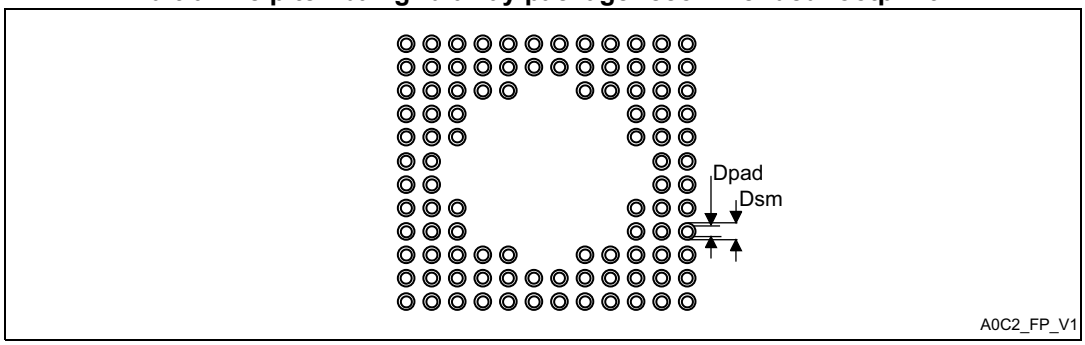
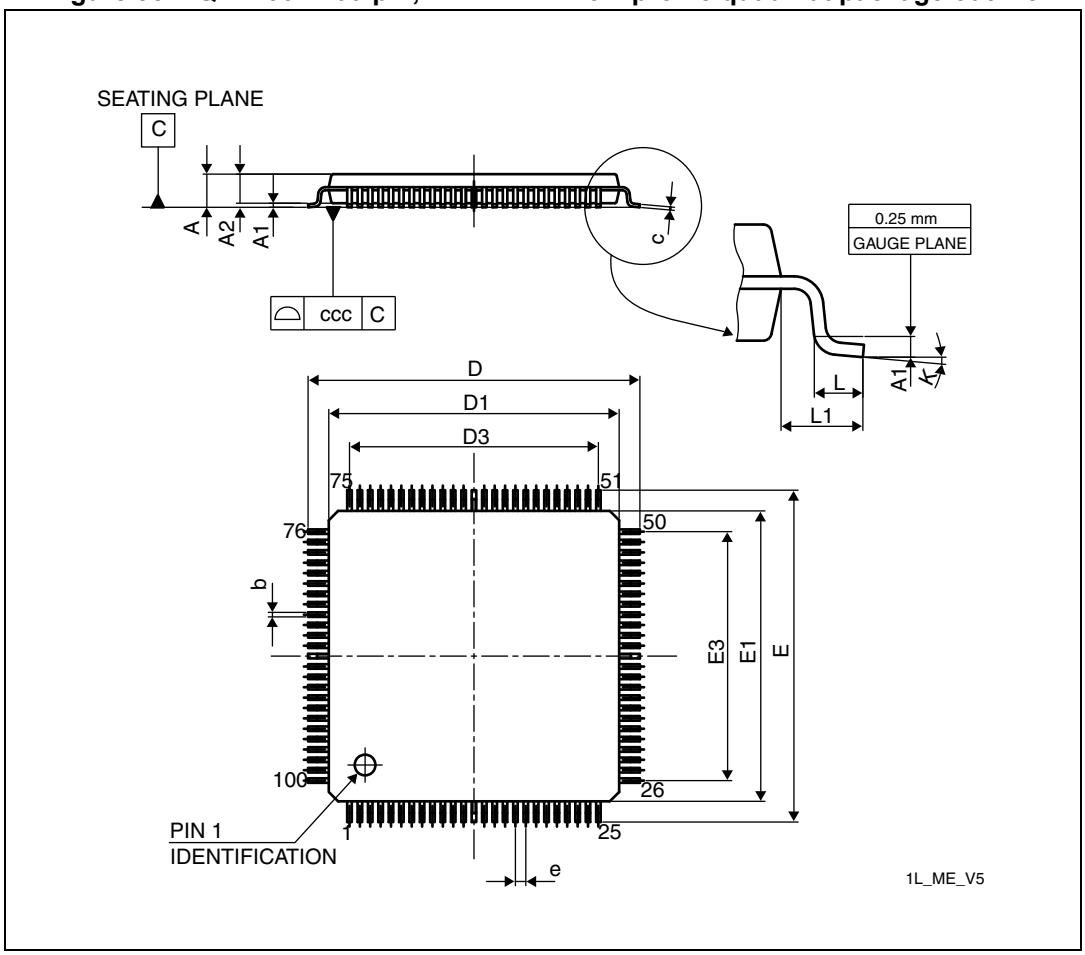



**Table 77. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.5 |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |

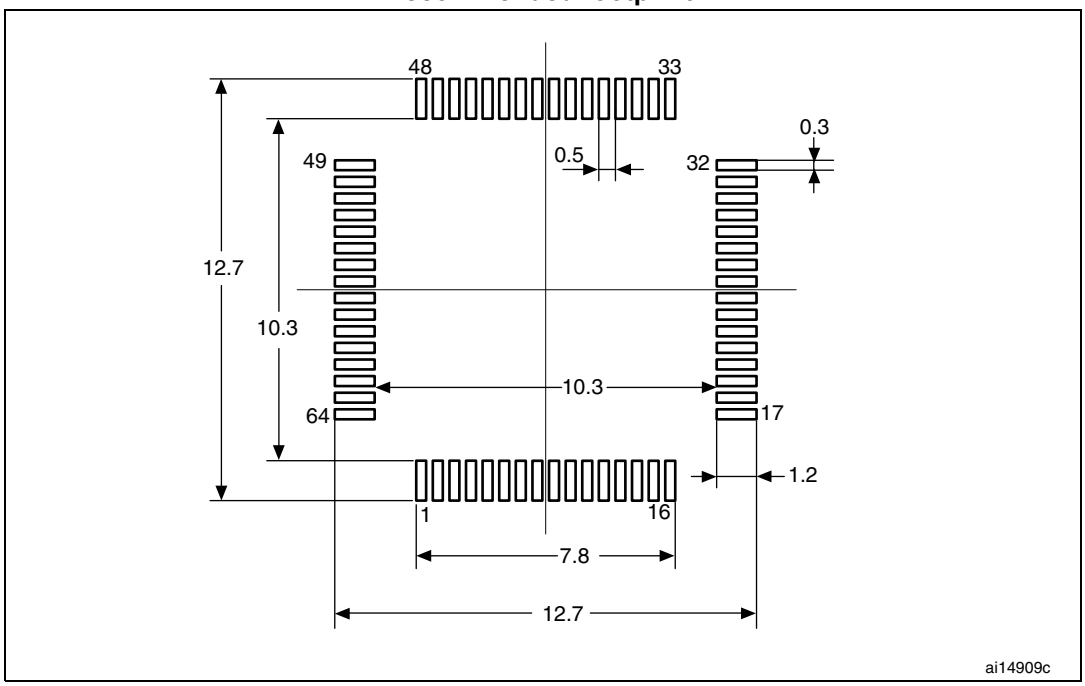
## 7.2 LQFP100 package information

**Figure 35. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline**




1. Drawing is not to scale.

**Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint**

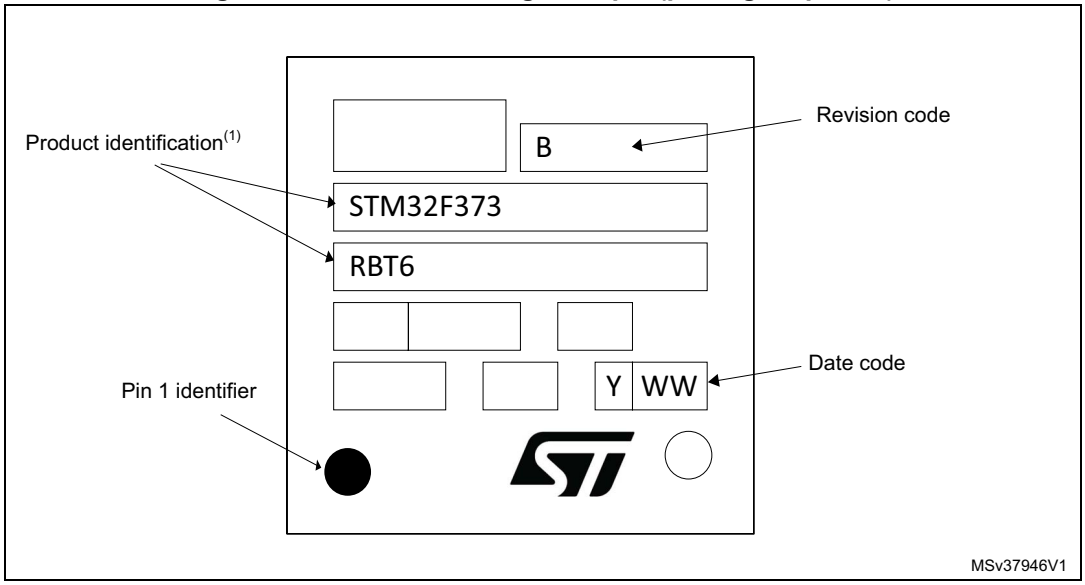



1. Dimensions are expressed in millimeters.

## Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 40. LQFP64 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 83. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 19-Sep-2013 | 4 | Replaced “Cortex-M4F” with “Cortex-M4” throughout the document.<br>Removed part number STM32F372xx.<br>Added “1.25 DMIPS/MHz (Dhrystone 2.1)” in *Features*.<br>Updated *Introduction*.<br>Added reference to the STMTouch touch sensing firmware library in *Section 3.16: Touch sensing controller (TSC)*.<br>Added “All I2S interfaces can operate in half-duplex mode only.” in *Section 3.21: Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)*.<br>Added row “I2S full-duplex mode” to *Table 9: STM32F373xx SPI/I2S implementation*.<br>Modified introduction of *I2C interface characteristics*.<br>Added alternate function RTC_REFIN and removed additional function RTC_REF_CLK_IN to pins PA1 and PB15.<br>Replaced alternate function JNTRST with NJTRST for pin PB4.<br>In *Table 12: Alternate functions for port PA*: replaced alternate function JTMS-SWDIO with SWDIO-JTMS for pin PA13, and JTCK-SWCLK with SWCLK-JTCK for pin PA14.<br>Added rows $V_{REF+}$ and $V_{REFSD+}$ to *Table 22: General operating conditions*.<br>Replaced "$f_{APB1} = f_{AHB/2}$" with "$f_{APB1} = f_{AHB}$" for “When the peripherals are enabled...” in *Typical current consumption*.<br>Added COMP in *Table 36: Peripheral current consumption*<br>Added conditions for $f_{HSE\_ext}$ in *Table 38: High-speed external user clock characteristics*.<br>Added Min and Max values for $ACC_{HSI}$ in *Table 42: HSI oscillator characteristics*.<br>Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in *Table 49: ESD absolute maximum ratings*.<br>Removed pins PB0 and PB1 in description of $I_{INJ}$ in *Table 51: I/O current injection susceptibility*.<br>Updated *Table 56: I2C characteristics*.<br>Replaced all occurrences of “gain/2” with “gain*2” in *Table 74: SDADC characteristics*.<br>Corrected typo in *Figure 19: I/O AC characteristics definition*.<br>Replaced *Figure 21: I2C bus AC waveforms and measurement circuit*..<br>Added $I_{DDA(ADC)}$ and footnote 1 in *Table 60: ADC characteristics* |