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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373vct6

3.3 Embedded Flash memory

All STM32F373xx devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Embedded SRAM

All STM32F373xx devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.12 12-bit analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter is based on a successive approximation register (SAR) architecture. It has up to 16 external channels (AIN15:0) and 3 internal channels (temperature sensor, voltage reference, V_{BAT} voltage measurement) performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers (TIMx) can be internally connected to the ADC start and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See *Table 65: Temperature sensor calibration values on page 105*.

3.12.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.12.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.19 Inter-integrated circuit interface (I^2C)

Two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes with 20 mA output drive. They support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I^2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeout verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the application to wake up the MCU from Stop mode on address match.

The I^2C interfaces can be served by the DMA controller

Refer to *Table 7* for the differences between I2C1 and I2C2.

Table 7. STM32F373xx I^2C implementation

I^2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X

Table 11. STM32F373xx pin definitions (continued)

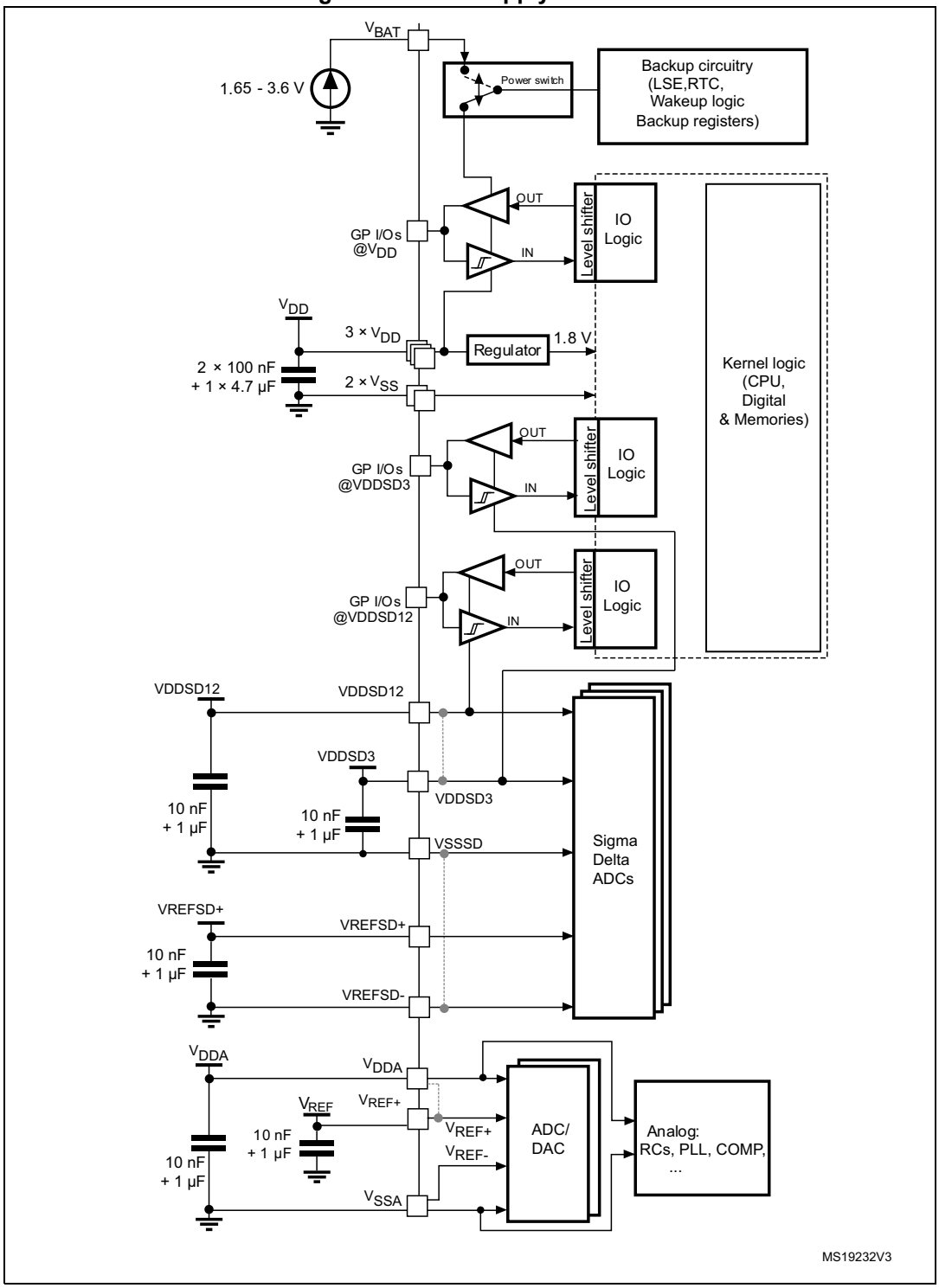
Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
8	D1	3	3	PC14 - OSC32_IN(1)	I/O	TC	-	-	OSC32_IN
9	E1	4	4	PC15 - OSC32_OUT(1)	I/O	TC	-	-	OSC32_OUT
10	F2	-	-	PF9	I/O	FT	(2)	TIM14_CH1	-
11	G2	-	-	PF10	I/O	FT	(2)	-	-
12	F1	5	5	PF0 - OSC_IN	I/O	FTf	-	I2C2_SDA	OSC_IN
13	G1	6	6	PF1 - OSC_OUT	I/O	FTf	-	I2C2_SCL	OSC_OUT
14	H2	7	7	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
15	H1	8	-	PC0	I/O	TTa	(2)	TIM5_CH1_ETR	ADC_IN10
16	J2	9	-	PC1	I/O	TTa	(2)	TIM5_CH2	ADCIN11
17	J3	10	-	PC2	I/O	TTa	(2)	SPI2_MISO/I2S2_MCK, TIM5_CH3	ADC_IN12
18	K2	11	-	PC3	I/O	TTa	(2)	SPI2_MOSI/I2S2_SD, TIM5_CH4	ADC_IN13
19	J1	-	-	PF2	I/O	FT	(2)	I2C2_SMBA	-
20	K1	12	8	VSSA/VREF-	S	-	-	Analog ground	
-	-	-	9	VDDA/VREF+	S	-	(2)	Analog power supply / Reference voltage for ADC, COMP, DAC	
21	M1	13	-	VDDA	S	-	(2)	Analog power supply	
22	L1	17	-	VREF+	S	-	(2)	Reference voltage for ADC, COMP, DAC	
23	L2	14	10	PA0	I/O	TTa	-	USART2_CTS, TIM2_CH1_ETR, TIM5_CH1_ETR, TIM19_CH1, TSC_G1_IO1, COMP1_OUT	RTC_ TAMPER2, WKUP1, ADC_IN0, COMP1_INM
24	M2	15	11	PA1	I/O	TTa	-	SPI3_SCK/I2S3_CK, USART2_RTS, TIM2_CH2, TIM15_CH1N, TIM5_CH2, TIM19_CH2, TSC_G1_IO2, RTC_REFIN	ADC_IN1, COMP1_INP

Table 12. Alternate functions for port PA

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA0	-	TIM2_CH1_ETR	TIM5_CH1_ETR	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT	-	-	TIM19_CH1	-	EVENTOUT
PA1	RTC_REFIN	TIM2_CH2	TIM5_CH2	TSC_G1_IO2	-	-	SPI3_SCK/I2S3_CK	USART2_RTS	-	TIM15_CH1N	-	TIM19_CH2	-	EVENTOUT
PA2	-	TIM2_CH3	TIM5_CH3	TSC_G1_IO3	-	-	SPI3_MISO/I2S3_MCK	USART2_TX	COMP2_OUT	TIM15_CH1	-	TIM19_CH3	-	EVENTOUT
PA3	-	TIM2_CH4	TIM5_CH4	TSC_G1_IO4	-	-	SPI3_MOSI/I2S3_SD	USART2_RX	-	TIM15_CH2	-	TIM19_CH4	-	EVENTOUT
PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	TIM12_CH1	-	-	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	TSC_G2_IO2	-	SPI1_SCK/I2S1_CK	-	CEC	-	TIM14_CH1	TIM12_CH2	-	-	EVENTOUT
PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	-	SPI1_MISO/I2S1_MCK	-	-	COMP1_OUT	TIM13_CH1	-	-	-	EVENTOUT
PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	-	SPI1_MOSI/I2S1_SD	-	-	COMP2_OUT	TIM14_CH1	-	-	-	EVENTOUT
PA8	MCO	-	TIM5_CH1_ETR	-	I2C2_SMBA	SPI2_SCK/I2S2_CK	-	USART1_CK	-	-	TIM4_ETR	-	-	EVENTOUT
PA9	-	-	TIM13_CH1	TSC_G4_IO1	I2C2_SCL	SPI2_MISO/I2S2_MCK	-	USART1_TX	-	TIM15_BKIN	TIM2_CH3	-	-	EVENTOUT
PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	SPI2_MOSI/I2S2_SD	-	USART1_RX	-	TIM14_CH1	TIM2_CH4	-	-	EVENTOUT
PA11	-	-	TIM5_CH2	-	-	SPI2_NSS/I2S2_WS	SPI1_NSS/I2S1_WS	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	-	-	EVENTOUT
PA12	-	TIM16_CH1	TIM5_CH3	-	-	-	SPI1_SCK/I2S1_CK	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2	-	-	EVENTOUT

6.1.6 Power supply scheme

Figure 9. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

The following relationship must be respected between V_{REFSD+} and V_{DDSD12}, V_{DDSD3}: V_{REFSD+} must be lower than V_{DDSD3}.
Depending on the SDADCx operation mode, there can be more constraints between V_{REFSD+}, V_{DDSD12} and V_{DDSD3} which are described in reference manual RM0313.

Table 20. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x and VDDSDx power lines (source)(1)	160	mA
ΣI_{VSS}	Total current out of sum of all VSS_x and VSSSD ground lines (sink)(1)	-160	
$I_{VDD(PIN)}$	Maximum current into each VDD_x or VDDSDx power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x or VSSSD ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. VDDSD12 is the external power supply for the PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to V_{SS}). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to V_{SS}). V_{DD} (VDD_x) is the external power supply for all remaining I/O pins (the I/O pin ground is internally connected to V_{SS}).
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 62*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{APB1} = f_{AHB}/2$, $f_{APB2} = f_{AHB}$
- When f_{HCLK} > 8 MHz PLL is ON and PLL inputs is equal to HSI/2 = 4 MHz (if internal clock is used) or HSE = 8 MHz (if HSE bypass mode is used)

The parameters given in *Table 28* to *Table 34* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V(1)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	HSE bypass, PLL on	72 MHz	63.1	70.7	71.5	73.4	29.2	31.1	31.7	34.2	mA
			64 MHz	56.3	63.3	64.1	64.9	26.1	27.8	28.4	30.4	
			48 MHz	42.5	48.5	48.0	50.1	19.9	22.6	21.9	23.1	
			32 MHz	28.8	31.4	32.2	34.3	13.1	16.1	14.9	16.2	
			24 MHz	21.9	24.4	24.4	25.8	10.1	10.9	11.9	12.4	
		HSE bypass, PLL off	8 MHz	7.3	8.0	9.3	9.3	3.7	4.1	4.4	5.0	
			1 MHz	1.1	1.5	1.8	2.3	0.8	1.1	1.4	1.9	
		HSI clock, PLL on	64 MHz	51.7	57.7	58.0	60.4	25.8	27.6	28.1	30.1	
			48 MHz	38.6	45.9	43.5	46.9	19.8	21.9	21.7	22.8	
			32 MHz	26.4	31.1	29.7	31.9	13.1	15.7	14.8	16.2	
			24 MHz	20.3	22.6	22.6	23.7	6.9	7.5	8.1	8.8	
		HSI clock, PLL off	8 MHz	7.0	7.6	8.8	8.8	3.7	4.1	4.4	5.0	

Table 31. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ@V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} and V_{DDSD12}	Regulator in run mode, all oscillators OFF	1.99	2.07	2.19	2.33	2.46	2.64	10.8	11.8	12.4	µA
			Regulator in low-power mode, all oscillators OFF	1.99	2.07	2.18	2.32	2.47	2.63	10.6	11.5	12.5	
	Supply current in Standby mode		LSI ON and IWDG ON	2.44	2.53	2.7	2.89	3.09	3.33	-	-	-	
			LSI OFF and IWDG OFF	1.87	1.94	2.06	2.19	2.35	2.51	4.1	4.5	4.8	
IDDAmon	Supply current for V_{DDA} and V_{DDSD12} monitoring	-		0.95	1.02	1.12	1.2	1.27	1.4	-	-	-	

1. Data based on characterization results and tested in production.
2. To obtain data with monitoring OFF is necessary to substract the IDDAmon current.

Table 32. Typical and maximum current consumption from V_{BAT} supply(1)

Symbol	Parameter	Conditions	Typ @ V_{BAT}							Max(2)			Unit
			= 1.65 V	= 1.8 V	= 2.0 V	= 2.4 V	= 2.7 V	= 3.3 V	= 3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.50	0.52	0.55	0.63	0.70	0.87	0.95	1.1	1.6	2.2	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.85	0.90	0.93	1.02	1.10	1.27	1.38	1.6	2.4	3.0	

1. Crystal used: Abracon ABS07-120-32.768kHz-T with 6 pF of CL for typical values.
2. Guaranteed by characterization results.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 37. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = V_{DDA}					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.1	3.9	3.8	3.7	3.6	4.5	µs
		Regulator in low power mode	7.9	6.7	6.1	5.7	5.4	8.6	
$t_{WUSTANDBY}$	Wakeup from Standby mode	LSI and IWDG off	62.6	53.7	49.2	45.7	42.7	100	
$t_{WUSLEEP}$	Wakeup from Sleep mode	After WFE instruction	6						CPU clock cycles

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

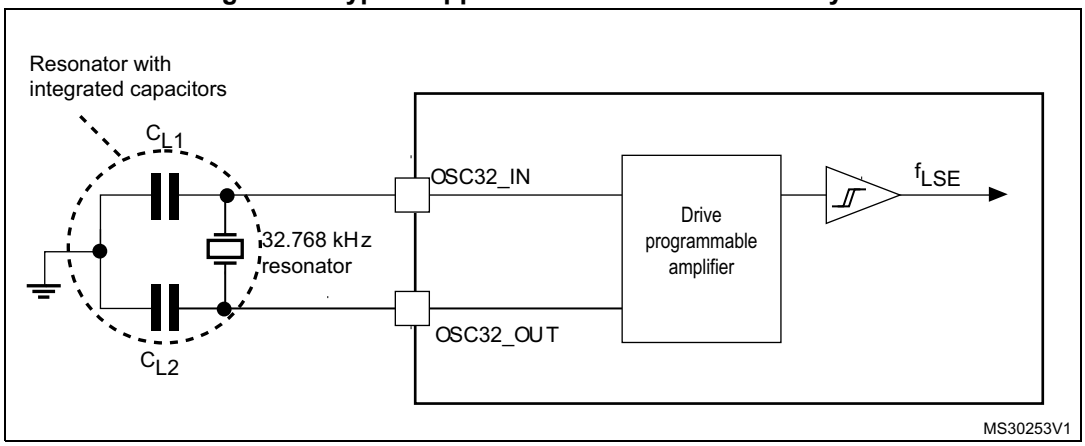
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 12*.

Table 38. High-speed external user clock characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	-	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	-	20	

1. Guaranteed by design.

Figure 15. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

The provided curves are characterization results, not tested in production.

High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = –40 to 105 °C	–3.8(3)	-	4.6(3)	%
		T_A = –10 to 85 °C	–2.9(3)	-	2.9(3)	%
		T_A = 0 to 70 °C	–2.3(3)	-	–2.2(3)	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI)}$	HSI oscillator startup time	-	1(3)	-	2(3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	100(3)	µA

1. V_{DDA} =3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 47*. They are based on the EMS levels and classes defined in application note AN1709.

Table 47. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 48. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} - 3.3 V, T_A - 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	9	dBµV
			30 to 130 MHz	26	
			130 MHz to 1 GHz	30	
			SAE EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 49. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1, LQFP100, LQFP64, LQFP48 and UFBGA100 packages	II	500	

1. Guaranteed by characterization results.

Table 51. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	-0	NA	mA
	Injected current on PC0 pin	-0	+5	
	Injected current on TC type I/O pins on VDDSD12 power domain: PB2, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB10 with induced leakage current on other pins from this group less than -50 µA	-5	+5	
	Injected current on TC type I/O pins on VDDSD3 power domain: PB14, PB15, PD8, PD9, PD10, PD12, PD13, PD14, PD15 with induced leakage current on other pins from this group less than -50 µA	-5	+5	
	Injected current on TTa type pins: PA4, PA5, PA6 with induced leakage current on adjacent pins less than -10 µA	-5	+5	
	Injected current on any other FT and FTf pins	-5	NA	
	Injected current on any other pins	-5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.18 DAC electrical specifications

Table 63. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.4	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}		2.4	-	3.6	V
V_{SSA}	Ground		-	0	-	0	V
R_{LOAD}(1)	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
R_O(1)	Output Impedance	DAC output buffer OFF		-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).		-	-	50	pF
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) and (0xEAB) at V_{REF+} = 2.4 V		0.2	-	-	V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON			-	-	V_{DDA} – 0.2	V
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	It gives the maximum output excursion of the DAC.		-	0.5	-	mV
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF			-	-	V_{REF+} – 1LSB	V
$I_{DDVREF+}$(3)	DAC DC current consumption in quiescent mode (Standby mode)	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs		-	-	220	µA
I_{DDA}(3)	DAC DC current consumption in quiescent mode(2)	With no load, middle code (0x800) on the inputs		-	-	380	µA
		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs		-	-	480	µA
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for the DAC in 10-bit configuration		-	-	± 0.5	LSB
		Given for the DAC in 12-bit configuration		-	-	± 2	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	Given for the DAC in 10-bit configuration		-	-	± 1	LSB
		Given for the DAC in 12-bit configuration		-	-	± 4	LSB

Table 64. Comparator characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

1. Guaranteed by design.
2. For more details and conditions see *Figure 30: Maximum VREFINT scaler startup time from power down*

Figure 30. Maximum V_{REFINT} scaler startup time from power down

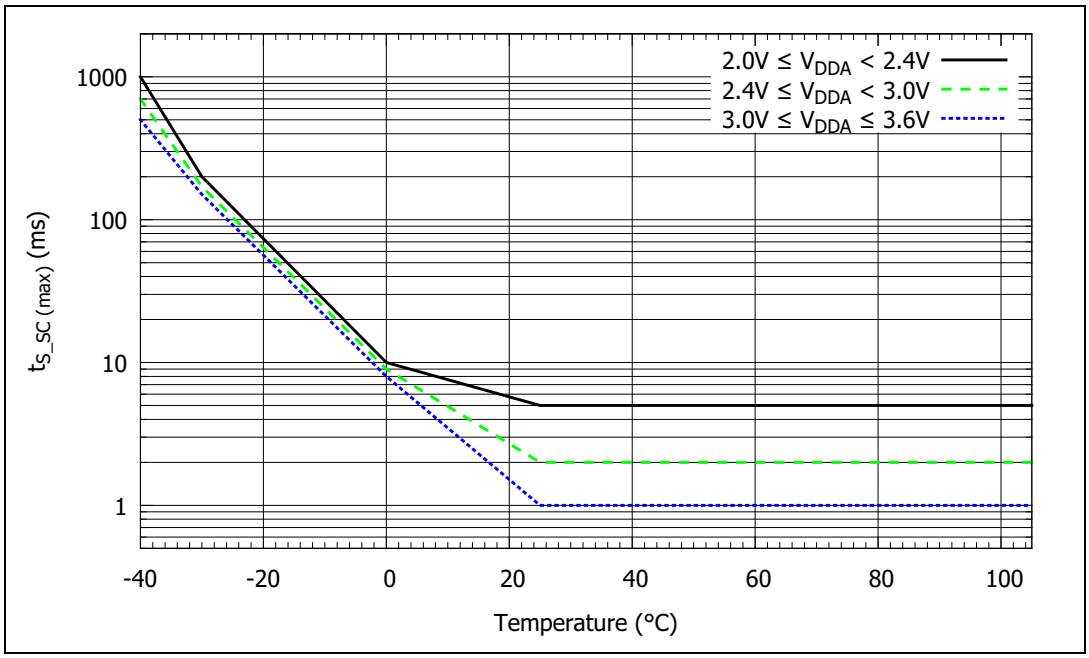


Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SNR(5)	Signal to noise ratio	Differential mode	gain = 1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(3)	84	85	-	dB	-
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	86	88	-		
						V_{REFSD+} = 3.3	88	92	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	76	78	-		
						V_{REFSD+} = 3.3	82	86	-		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(3)	76	80	-		
		Single ended mode	gain = 1	f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3	80	84	-		
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	77	81	-		
						V_{REFSD+} = 3.3	85	90	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	66	71	-		
						V_{REFSD+} = 3.3	74	78	-		

Table 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 33. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

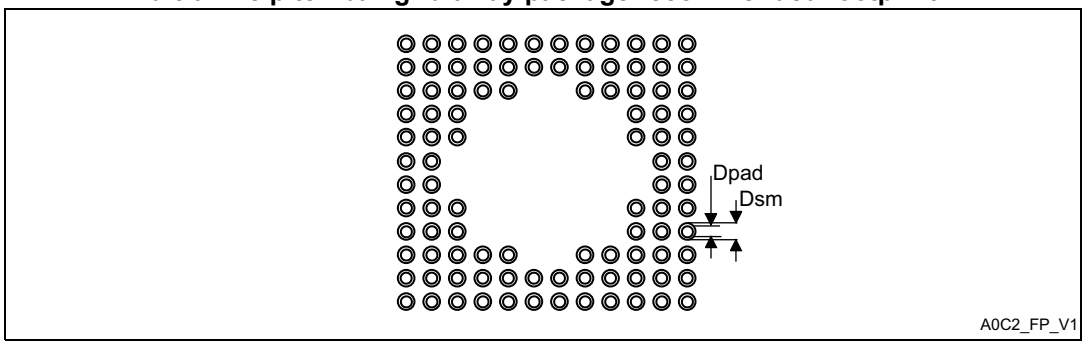


Table 77. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Table 83. Document revision history (continued)

Date	Revision	Changes
21-Dec-2012	3	Updated *Table 2: Device overview*, capacitive sensing channels peripheral added. Updated *Table 3: Capacitive sensing GPIOs available on STM32F373xx devices* Updated *Section 3.19: Inter-integrated circuit interface (I2C)* Updated the function names in *Table 11: STM32F373 pin definitions* Updated *Table 20: Current characteristics* Updated *Table 22: General operating conditions* Updated *Table 30: Typical and maximum VDD consumption in Stop and Standby modes* Updated *Table 32: Typical and maximum current consumption from VBAT supply* Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')* Updated *Table 33: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 34: Typical current consumption in Sleep mode, code running from Flash or RAM* Added *Table 35: Switching output I/O current consumption* Added *Table 36: Peripheral current consumption*, *Figure 16: HSI oscillator accuracy characterization results* Updated *Section 6.3.6: Wakeup time from low-power mode* Updated *Table 37: Low-power mode wakeup timings* Updated *Table 47: EMS characteristics* Updated *Table 51: I/O current injection susceptibility* Updated *Table 52: I/O static characteristics* Updated , *Figure 18: TC and TTa I/O input characteristics - TTL port*, *Figure 18: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port* and *Figure 20: Five volt tolerant (FT and FTf) I/O input characteristics - TTL port* Updated *Table 53: Output voltage characteristics* Updated *Table 54: I/O AC characteristics* Updated *Table 55: NRST pin characteristics* Updated *Table 63: DAC characteristics* Updated *Table 74: SDADC characteristics* Updated *Figure 32: LQFP100 –14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 35: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Figure 38: LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline* Updated *Table 72: LQPF100 – 14 x 14 mm low-profile quad flat package mechanical data*, *Table 73: LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data* and *Table 74: LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data* Added *Figure 16: HSI oscillator accuracy characterization results*

Table 83. Document revision history (continued)

Date	Revision	Changes
08-Jun-2016	7	Updated: – *Table 3: Capacitive sensing GPIOs available on STM32F373xx devices* – *Table 19: Voltage characteristics* – *Table 27: Embedded internal reference voltage* – *Table 41: LSE oscillator characteristics (fLSE = 32.768 kHz)* – *Table 49: ESD absolute maximum ratings* – *Table 60: ADC characteristics* – *Table 63: DAC characteristics* – *Table 65: Temperature sensor calibration values* – *Table 74: SDADC characteristics* – *Table 81: Package thermal characteristics* – *Figure 17: TC and TTa I/O input characteristics - CMOS port* – *Figure 18: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port* Removed: – *Figure 18: TC and TTa I/O input characteristics - TTL port* – *Figure 20: Five volt tolerant (FT and FTf) I/O input characteristics - TTL port*