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"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e54rd2a-40-c-nje

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Product Description

The SST89E54RD2A/RDA and SST89E58RD2A/RDA are members of the FlashFlex family of 8-bit microcontroller products designed and manufactured with SST patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for SST customers. The devices use the 8051 instruction set and are pin-for-pin compatible with standard 8051 microcontroller devices.

The devices come with 24/40 KByte of on-chip flash EEPROM program memory which is partitioned into 2 independent program memory blocks. The primary Block 0 occupies 16/32 KByte of internal program memory space and the secondary Block 1 occupies 8 KByte of internal program memory space.

The 8-KByte secondary block can be mapped to the lowest location of the 16/32 KByte address space; it can also be hidden from the program counter and used as an independent EEPROM-like data memory.

In addition to the 24/40 KByte of EEPROM program memory on-chip and 1024 x8 bits of on-chip RAM, the devices can address up to 64 KByte of external program memory and up to 64 KByte of external RAM.

The flash memory blocks can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and the firmware for SST devices. During power-on reset, the devices can be configured as either a slave to an external host for source code storage or a master to an external host for an in-application programming (IAP) operation. The devices are designed to be programmed in-system and in-application on the printed circuit board for maximum flexibility. The devices are pre-programmed with an example of the bootstrap loader in the memory, demonstrating the initial user program code loading or subsequent user code updating via the IAP operation. The sample bootstrap loader is available for the user's reference and convenience only; SST does not guarantee its functionality or usefulness. Chip-Erase or Block-Erase operations will erase the pre-programmed sample code.

Memory Organization

The device has separate address spaces for program and data memory.

Program Flash Memory

There are two internal flash memory blocks in the device. The primary flash memory block (Block 0) has 16/32 KByte. The secondary flash memory block (Block 1) has 8 KByte. Since the total program address space is limited to 64 KByte, the SFCF[1:0] bit are used to control program bank selection. Please refer to Figures 5 and 6 for the program memory configuration. Program bank selection is described in the next section.

The 16K/32K x8 primary SuperFlash block is organized as 128/256 sectors, each sector consists of 128 Bytes.

The 8K x8 secondary SuperFlash block is organized as 64 sectors, each sector consists also of 128 Bytes.

For both blocks, the 7 least significant program address bits select the byte within the sector. The remainder of the program address bits select the sector within the block.
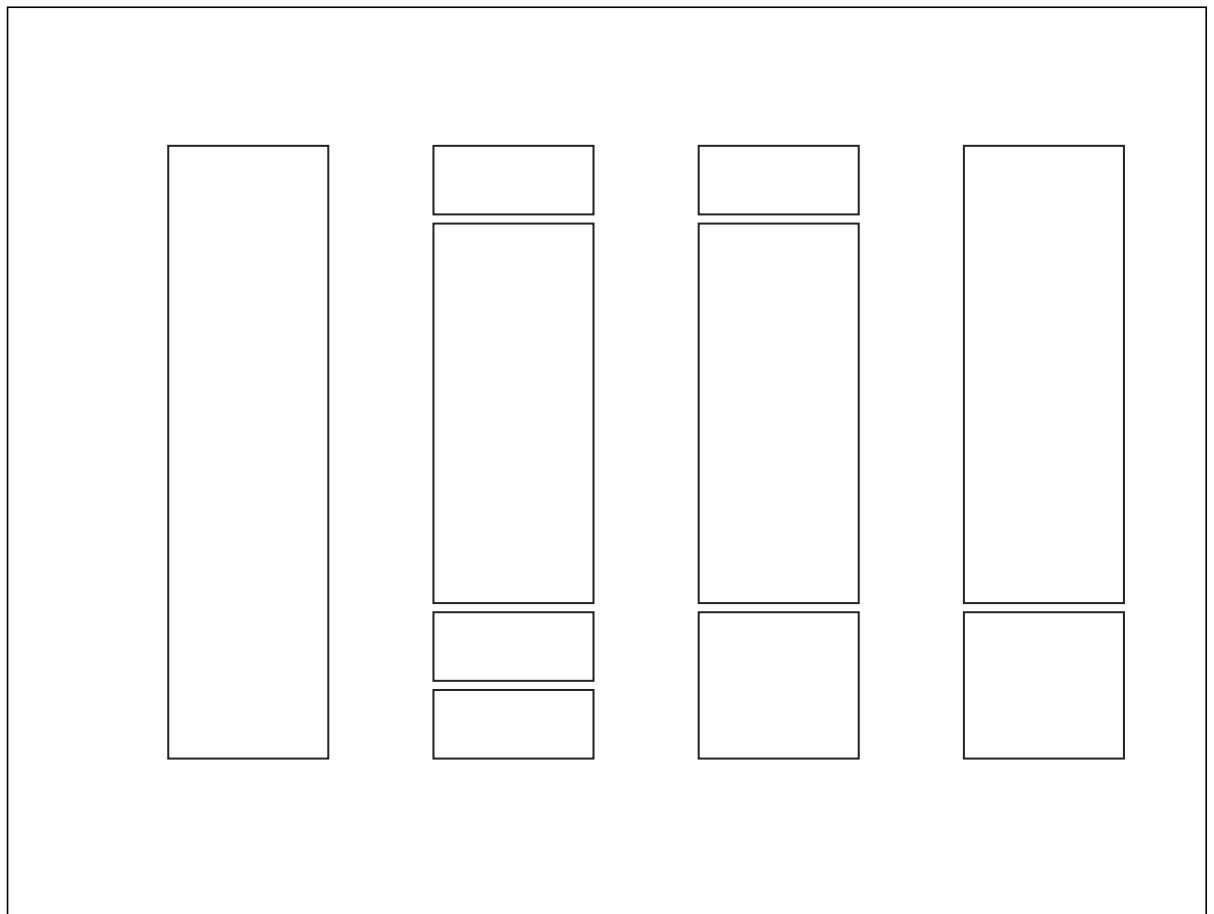

Figure 5: Program Memory Organization for 16 KByte SST89E54RDxA

Expanded Data RAM Addressing

The SST89E/V5xRDxA both have the capability of 1K of RAM. See Figure 7.

The device has four sections of internal data memory:

1. The lower 128 Bytes of RAM (00H to 7FH) are directly and indirectly addressable.

2. The higher 128 Bytes of RAM (80H to FFH) are indirectly addressable.

3. The special function registers (80H to FFH) are directly addressable only.

4. The expanded RAM of 768 Bytes (00H to 2FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit. (See "Auxiliary Register (AUXR)" in Section , "Special Function Registers")

Since the upper 128 bytes occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

When instructions access addresses in the upper 128 bytes (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

MOV @R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in "#data" is written to RAM location 90H rather than port 1.

Direct Access:

MOV 90H, #data; write data to P1

Data in "#data" is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 bytes of memory is physically located on the chip and logically occupies the first 768 bytes of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 (WR#), P3.7 (RD#), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

MOVX @DPTR, A; DPTR contains 0A0H

DPTR points to 0A0H and data in "A" is written to address 0A0H of the expanded RAM rather than external memory. Access to external memory higher than 2FFH using the MOVX instruction will access external memory (0300H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX

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@DPTR generates a 16-bit address. This allows external addressing up the 64K. Port 2 provides the high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary read and write signals (P3.6 - WR# and P3.7 - RD#) for external memory use. Table 4 shows external data memory RD#, WR# operation with EXTRAM bit.

The stack pointer (SP) can be located anywhere within the 256 bytes of internal RAM (lower 128 bytes and upper 128 bytes). The stack pointer may not be located in any part of the expanded RAM.

Table 4: External Data Memory RD#, WR# with EXTRAM bit

AUXR	MOVX @DPTR, A or MOVX A, @DPTR		MOVX @Ri, A or MOVX A, @Ri
	ADDR < 0300H	ADDR >= 0300H	ADDR = Any
EXTRAM = 0	RD# / WR# not asserted	RD# / WR# asserted	RD# / WR# not asserted[1]
EXTRAM = 1	RD# / WR# asserted	RD# / WR# asserted	RD# / WR# asserted

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1. Access limited to ERAM address within 0 to 0FFH; cannot access 100H to 02FFH.

2FFH

Expanded RAM

000H

0300H

0000H

EXTRAM = 0

EXTRAM = 1
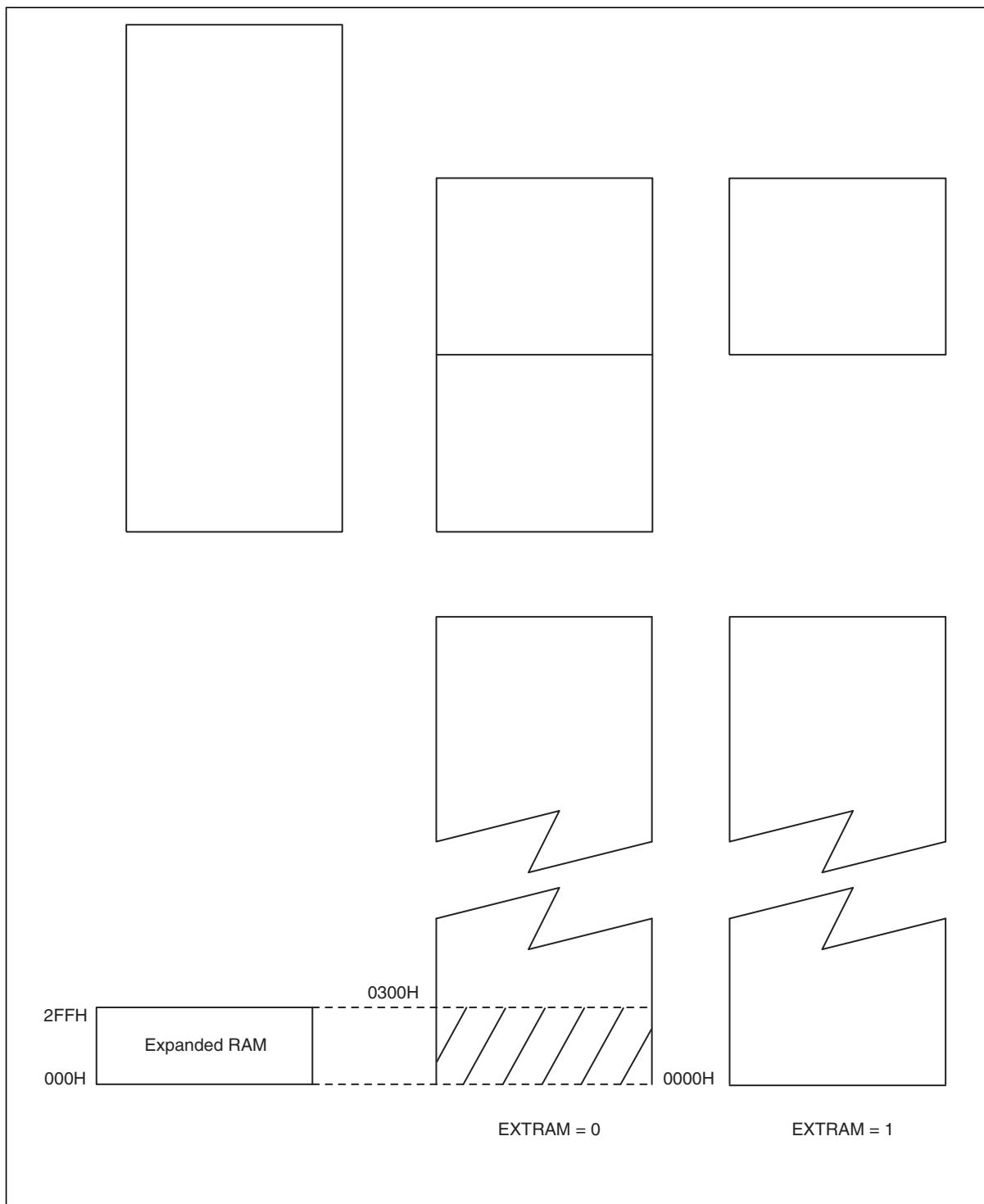
Figure 7: Internal and External Data Memory Structure

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PCA Compare/Capture Module Mode Register[1] (CCAPMn)

Location	7	6	5	4	3	2	1	0	Reset Value
DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	00xxx000b
DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	00xxx000b
DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	00xxx000b
DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	00xxx000b
DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	00xxx000b

1. Not bit addressable

Symbol	Function
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
ECOMn	Enable Comparator 0: Disables the comparator function 1: Enables the comparator function
CAPPn	Capture Positive 0: Disables positive edge capture on CEX[4:0] 1: Enables positive edge capture on CEX[4:0]
CAPNn	Capture Negative 0: Disables negative edge capture on CEX[4:0] 1: Enables negative edge capture on CEX[4:0]
MATn	Match: Set ECOM[4:0] and MAT[4:0] to implement the software timer mode 0: Disables software timer mode 1: A match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle 0: Disables toggle function 1: A match of the PCA counter with this module's compare/capture register causes the the CEXn pin to toggle.
PWMn	Pulse Width Modulation mode 0: Disables PWM mode 1: Enables CEXn pin to be used as a pulse width modulated output
ECCFn	Enable CCF Interrupt 0: Disables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request. 1: Enables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request.

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SPI Data Register (SPDR)

Location	7	6	5	4	3	2	1	0	Reset Value
86H				SPDR[7:0]					00H

Power Control Register (PCON)

Location	7	6	5	4	3	2	1	0	Reset Value
87H	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	00010000b

Symbol	Function
SMOD1	Double Baud rate bit. If SMOD1 = 1, Timer 1 is used to generate the baud rate, and the serial port is used in modes 1, 2, and 3.
SMOD0	FE/SM0 Selection bit. 0: SCON[7] = SM0 1: SCON[7] = FE,
BOF	Brown-out detection status bit, this bit will not be affected by any other reset. BOF should be cleared by software. Power-on reset will also clear the BOF bit. 0: No brown-out. 1: Brown-out occurred
POF	Power-on reset status bit, this bit will not be affected by any other reset. POF should be cleared by software. 0: No Power-on reset. 1: Power-on reset occurred
GF1	General-purpose flag bit.
GF0	General-purpose flag bit.
PD	Power-down bit, this bit is cleared by hardware after exiting from power-down mode. 0: Power-down mode is not activated. 1: Activates Power-down mode.
IDL	Idle mode bit, this bit is cleared by hardware after exiting from idle mode. 0: Idle mode is not activated. 1: Activates idle mode.

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Byte-Program

The Byte-Program command programs data into a single byte. The address is determined by the contents of SFAH and SFAL. The data byte is in SFDT.
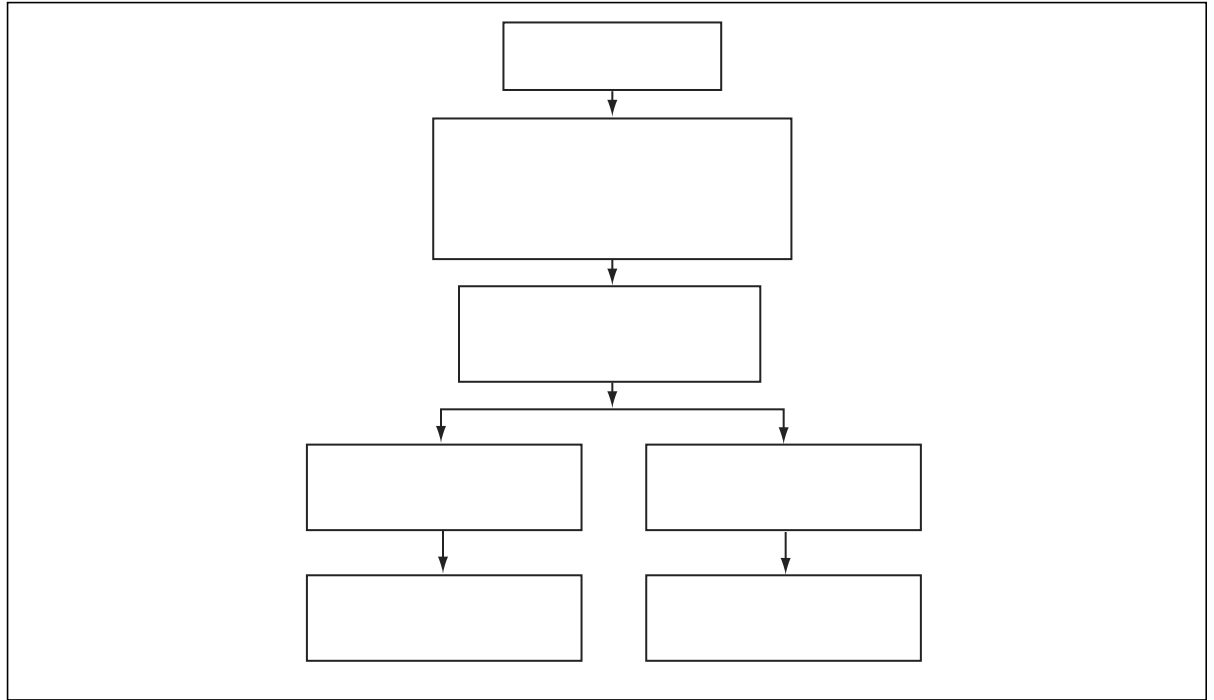

Figure 12: Byte-Program

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Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 9 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 14: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

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1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 15: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

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1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

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Using the Broadcast Address to Select Slaves

Using the broadcast address, the master can communicate with all the slaves at once. It is formed by performing a logical OR of SADDR and SADEN with '0's in the result treated as "don't cares".

Slave 1

```
 1111 0001  =  SADDR
+1111 1010  =  SADEN
 1111 1X11  =  Broadcast
```

"Don't cares" allow for a wider range in defining the broadcast address, but in most cases, the broadcast address will be FFH.

On reset, SADDR and SADEN are "0". This produces an given address of all "don't cares" as well as a broadcast address of all "don't cares." This effectively disables Automatic Addressing mode and allows the microcontroller to function as a standard 8051, which does not make use of this feature.

Serial Peripheral Interface

SPI Features

- Master or slave operation
- 10 MHz bit frequency (max)
- LSB first or MSB first data transfer
- Four programmable bit rates
- End of transmission (SPIF)
- Write collision flag protection (WCOL)
- Wake up from idle mode (slave mode only)

SPI Description

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the SST89E/V5xRDxA and peripheral devices or between several SST89E/V5xRDxA devices.

Figure 20 shows the correspondence between master and slave SPI devices. The SCK pin is the clock output and input for the master and slave modes, respectively. The SPI clock generator will start following a write to the master devices SPI data register. The written data is then shifted out of the MOSI pin on the master device into the MOSI pin of the slave device. Following a complete transmission of one byte of data, the SPI clock generator is stopped and the SPIF flag is set. An SPI interrupt request will be generated if the SPI Interrupt Enable bit (SPIE) and the Serial Port Interrupt Enable bit (ES) are both set.

An external master drives the Slave Select input pin, SS#/P1[4], low to select the SPI module as a slave. If SS#/P1[4] has not been driven low, then the slave SPI unit is not active and the MOSI/P1[5] port can also be used as an input port pin.

CPHA and CPOL control the phase and polarity of the SPI clock. Figures 21 and 22 show the four possible combinations of these two bits.

Watchdog Timer

The device offers a programmable Watchdog Timer (WDT) for fail safe protection against software deadlock and automatic recovery.

To protect the system against software deadlock, the user software must refresh the WDT within a user-defined time period. If the software fails to do this periodical refresh, an internal hardware reset will be initiated if enabled (WDRE= 1). The software can be designed such that the WDT times out if the program does not work properly.

The WDT in the device uses the system clock (XTAL1) as its time base. So strictly speaking, it is a watchdog counter rather than a watchdog timer. The WDT register will increment every 344,064 crystal clocks. The upper 8-bits of the time base register (WDTD) are used as the reload register of the WDT.

The WDTS flag bit is set by WDT overflow and is not changed by WDT reset. User software can clear WDTS by writing "1" to it.

Figure 23 provides a block diagram of the WDT. Two SFRs (WDTC and WDTD) control watchdog timer operation. During idle mode, WDT operation is temporarily suspended, and resumes upon an interrupt exit from idle.

The time-out period of the WDT is calculated as follows:

Period = (255 - WDTD) * 344064 * $1/f_{CLK\,(XTAL1)}$

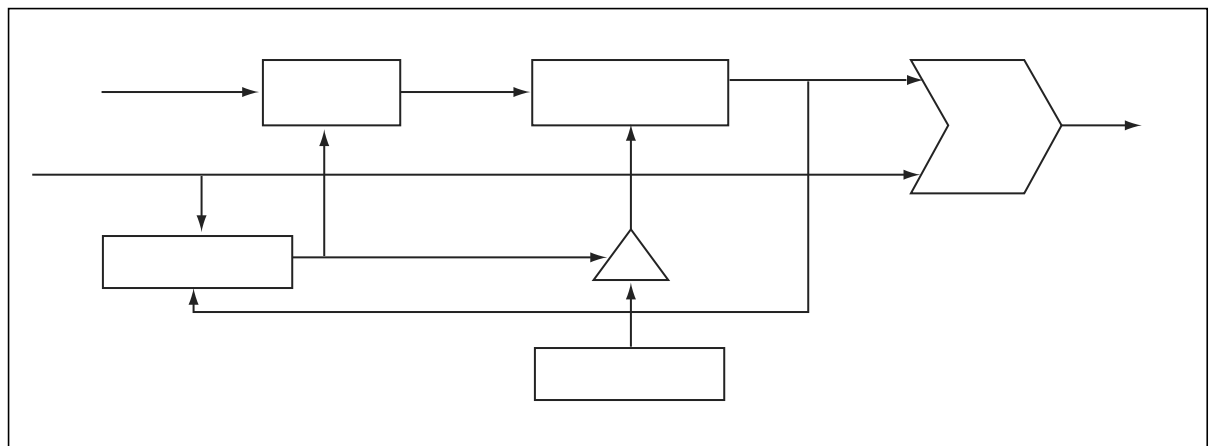where WDTD is the value loaded into the WDTD register and f_{OSC} is the oscillator frequency.

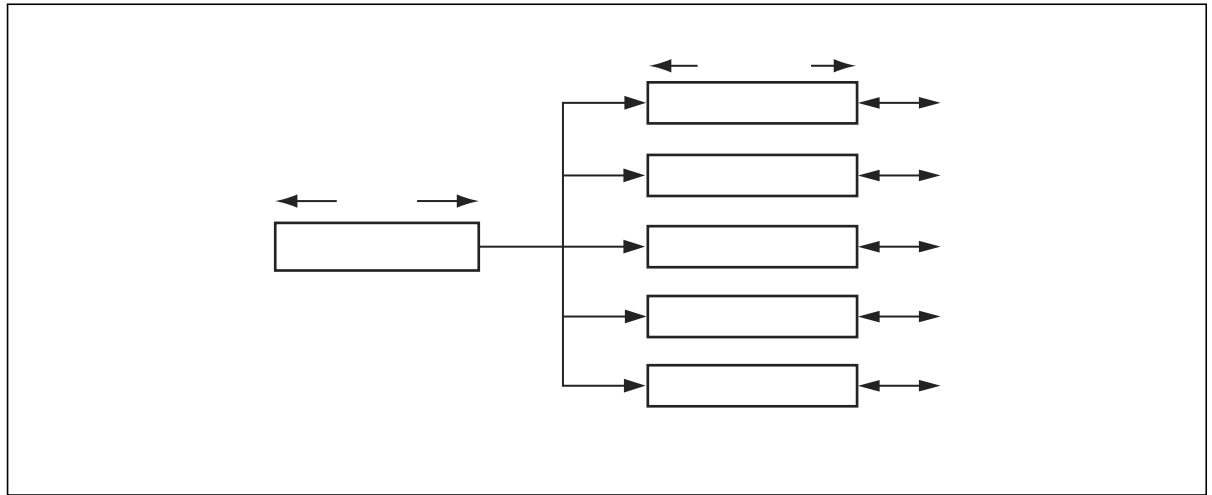**Figure 23:** Block Diagram of Programmable Watchdog Timer

Figure 24: PCA Timer/Counter and Compare/Capture Modules

The table below summarizes various clock inputs at two common frequencies.

Table 18: PCA Timer/Counter Inputs

	Clock Increments	
PCA Timer/Counter Mode	**12 MHz**	**16 MHz**
Mode 0: $f_{OSC}/12$	1 μsec	0.75 μsec
Mode 1:	330 nsec	250 nsec
Mode 2: Timer 0 Overflows[1]		
Timer 0 programmed in:		
8-bit mode	256 μsec	192 μsec
16-bit mode	65 msec	49 μsec
8-bit auto-reload	1 to 255 μsec	0.75 to 191 μsec
Mode 3: External Input MAX	0.66 μsec	0.50 μsec

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1. In Mode 2, the overflow interrupt for Timer 0 does not need to be enabled.

The four possible CMOD timer modes with and without the overflow interrupt enabled are shown below. This list assumes that PCA will be left running during idle mode.

Table 19: CMOD Values

	CMOD Value	
PCA Count Pulse Selected	**Without Interrupt Enabled**	**With Interrupt Enabled**
Internal clock, $f_{OSC}/12$	00H	01H
Internal clock, $f_{OSC}/4$	02H	03H
Timer 0 overflow	04H	05H
External clock at P1.2	06H	07H

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The CCON register is associated with all PCA timer functions. It contains run control bits and flags for the PCA timer (CF) and all modules. To run the PCA the CR bit (CCON.6) must be set by software. Clearing the bit, will turn off PCA. When the PCA counter overflows, the CF (CCON.7) will be set, and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Each module has its own timer interrupt or capture interrupt flag (CCF0 for module 0, CCF4 for module 4, etc.). They are set when either a match or capture occurs. These flags can only be cleared by software. (See "PCA Timer/Counter Control Register (CCON)" on page 26.)

Compare/Capture Modules

Each PCA module has an associated SFR with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. Refer to "PCA Compare/Capture Module Mode Register (CCAPMn)" on page 28 for details. The registers each contain 7 bits which are used to control the mode each module will operate in. The ECCF bit (CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on module) will enable the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set, causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. When there is a match between the PCA counter and the module's capture/compare register, the MATn (CCAPMn.3) and the CCFn bit in the CCON register to be set.

Bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine whether the capture input will be active on a positive edge or negative edge. The CAPN bit enables the negative edge that a capture input will be active on, and the CAPP bit enables the positive edge. When both bits are set, both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set, enables the comparator function. Table 21 shows the CCAPMn settings for the various PCA functions.

There are two additional register associated with each of the PCA modules: CCAPnH and CCAPnL. They are registers that hold the 16-bit count value when a capture occurs or a compare occurs. When a module is used in PWM mode, these registers are used to control the duty cycle of the output. See Figure 24.

Table 20: PCA High and Low Register Compare/Capture Modules

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB	RESET Value
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]	00H
CCAP0L		EAH	CCAP0L[7:0]	00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]	00H
CCAP1L		EBH	CCAP1L[7:0]	00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]	00H
CCAP2L		ECH	CCAP2L[7:0]	00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]	00H
CCAP3L		EDH	CCAP3L[7:0]	00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]	00H
CCAP4L		EEH	CCAP4L[7:0]	00H

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Security Lock Status

The three bits that indicate the device security lock status are located in SFST[7:5]. As shown in Figure 30 and Table 24, the three security lock bits control the lock status of the primary and secondary blocks of memory. There are four distinct levels of security lock status. In the first level, none of the security lock bits are programmed and both blocks are unlocked. In the second level, although both blocks are now locked and cannot be programmed, they are available for read operation via Byte-Verify. In the third level, three different options are available: Block 1 hard lock / Block 0 SoftLock, SoftLock on both blocks, and hard lock on both blocks. Locking both blocks is the same as Level 2, Block 1 except read operation isn't available. The fourth level of security is the most secure level. It doesn't allow read/program of internal memory or boot from external memory. For details on how to program the security lock bits refer to the external host mode and in-application programming sections.
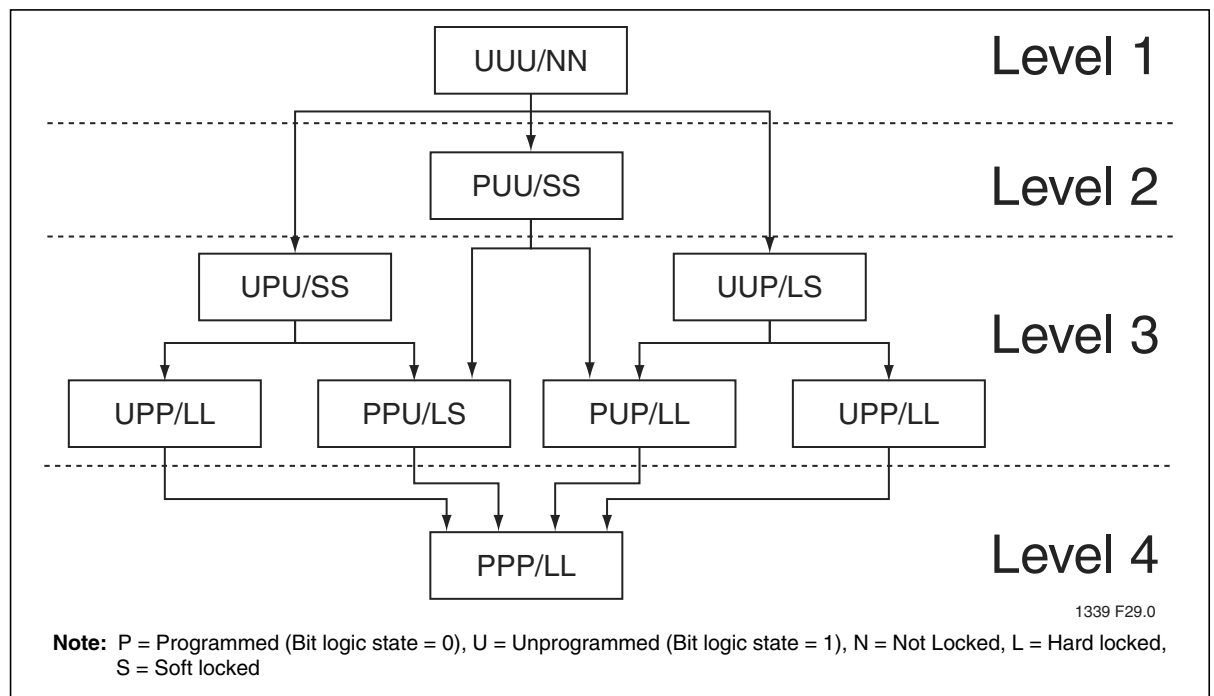

Note: P = Programmed (Bit logic state = 0), U = Unprogrammed (Bit logic state = 1), N = Not Locked, L = Hard locked, S = Soft locked

1339 F29.0

Figure 30: Security Lock Levels

Power-Saving Modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are idle and power-down, see Table 27.

Idle Mode

Idle mode is entered setting the IDL bit in the PCON register. In idle mode, the program counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits idle mode through either a system interrupt or a hardware reset. Exiting idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits idle mode. After exit the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the idle mode. A hardware reset starts the device similar to a power-on reset.

Power-down Mode

The power-down mode is entered by setting the PD bit in the PCON register. In the power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during power-down, the minimum V_{DD} level is 2.0V.

The device exits power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding the external interrupt pin low restarts the oscillator, the signal must hold low at least 1024 clock cycles before bringing back high to complete the exit. Upon interrupt signal being restored to logic $V_{IH,}$ the first instruction of the interrupt service routine will execute. A hardware reset starts the device similar to power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 29 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 13 for the IAP mode enabling commands (When set, the EDC# bit in SFST register will indicate 6 clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.
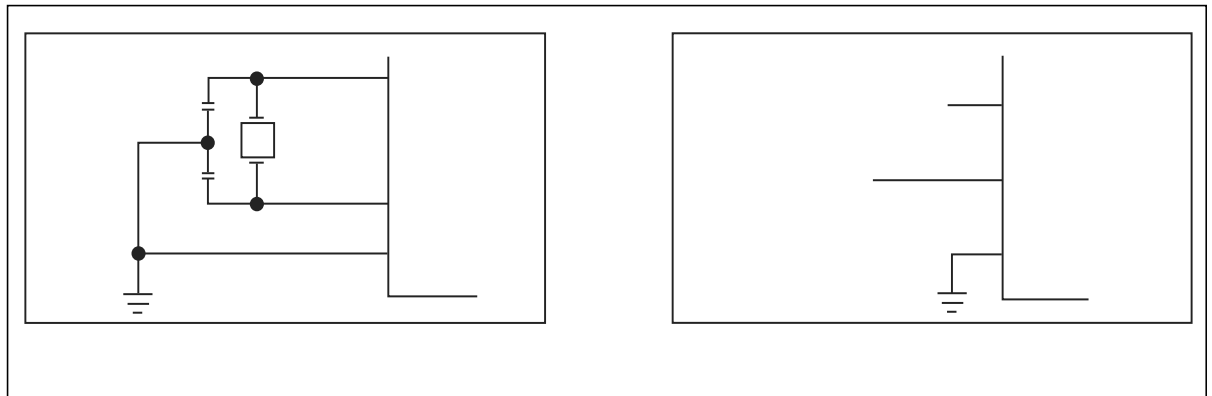

Figure 33: Oscillator Characteristics

Table 29: Clock Doubling Features

Device	Standard Mode (x1)		Clock Double Mode (x2)	
	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)
SST89E5xRD2A/RDA	12	40	6	20

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Electrical Specification

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias . . . . -55°C to +125°C

Storage Temperature. . . . . -65°C to +150°C

Voltage on EA# Pin to V_{SS}. . . . . -0.5V to +14.0V

D.C. Voltage on Any Pin to Ground Potential . . . .-0.5V to V_{DD}+0.5V

Transient Voltage (<20ns) on Any Other Pin to V_{SS} . . . .-1.0V to V_{DD}+1.0V

Maximum I_{OL} per I/O Pins P1.5, P1.6, P1.7 . . . . .20mA

Maximum I_{OL} per I/O for All Other Pins 15mA

Package Power Dissipation Capability ($T_A = 25°C$). 1.5W

Through Hole Lead Soldering Temperature (10 Seconds) . . . . 300°C

Surface Mount Solder Reflow Temperature[1]. . . . . 260°C for 10 seconds

Output Short Circuit Current[2] . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.
   (Based on package heat transfer limitations, not device power consumption.

Note: This specification contains preliminary information on new products in production.
Specifications are subject to change without notice.

Table 30: Operating Range

Symbol	Description	Min.	Max	Unit
T_A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
V_{DD}	Supply Voltage			
	SST89E5xRD2A/RDA	4.5	5.5	V
f_{OSC}	Oscillator Frequency			
	SST89E5xRD2A/RDA	0	40	MHz
	Oscillator Frequency for IAP			
	SST89E5xRD2A/RDA	0.25	40	MHz

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Table 31: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port:26mA
   Maximum I_{OL} total for all outputs:71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Load capacitance for Port 0, ALE and PSEN#= 100pF, load capacitance for all other outputs = 80pF.
4. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.
5. Pins of Ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
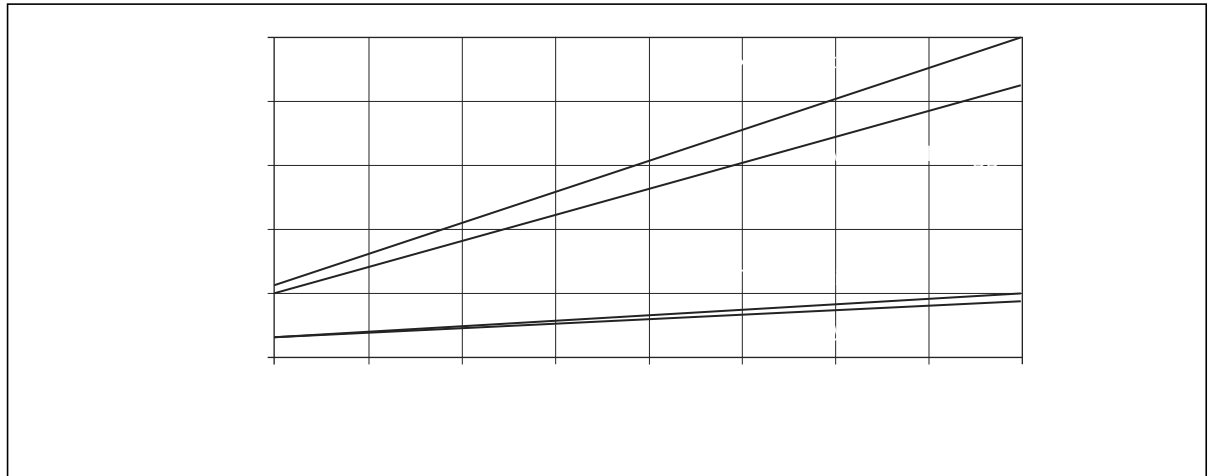6. Pin capacitance is characterized but not tested. EA# is 25pF (max).

Figure 34:I_{DD} vs. Frequency for 5V SST89E5xRD2A/RDA

Not Recommended for New Designs

AC Electrical Characteristics

AC Characteristics:

(Over Operating Conditions: Load Capacitance for Port 0, ALE#, and PSEN# = 100pF;
Load Capacitance for All Other Outputs = 80pF)

Table 36: AC Electrical Characteristics (1 of 2)
T_A = -40°C to +85°C, V_{DD} = 4.5-5.5V@40MHz, V_{SS} = 0V

Symbol	Parameter	Oscillator 40 MHz (x1 Mode) 20 MHz (x2 Mode) Min	Max	Variable Min	Max	Units
$1/T_{CLCL}$	x1 Mode Oscillator Frequency	0	40	0	40	MHz
$1/2T_{CLCL}$	x2 Mode Oscillator Frequency	0	20	0	20	MHz
T_{LHLL}	ALE Pulse Width	35		$2T_{CLCL}$ - 15		ns
T_{AVLL}	Address Valid to ALE Low			T_{CLCL} - 25 (3V)		ns
		10		T_{CLCL} - 15 (5V)		ns
T_{LLAX}	Address Hold After ALE Low			T_{CLCL} - 25 (3V)		ns
		10		T_{CLCL} - 15 (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In				$4T_{CLCL}$ - 65 (3V)	ns
			55		$4T_{CLCL}$ - 45 (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low			T_{CLCL} - 25 (3V)		ns
		10		T_{CLCL} - 15 (5V)		ns
T_{PLPH}	PSEN# Pulse Width	60		$3T_{CLCL}$ - 25 (3V) $3T_{CLCL}$ - 15 (5V)		ns
T_{PLIV}	PSEN# Low to Valid Instr In				$3T_{CLCL}$ - 55 (3V)	ns
			25		$3T_{CLCL}$ - 50 (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#			0		ns
T_{PXIZ}	Input Instr Float After PSEN#				T_{CLCL} - 5 (3V)	ns
			10		T_{CLCL} - 15 (5V)	ns
T_{PXAV}	PSEN# to Address valid	17		T_{CLCL} - 8		ns
T_{AVIV}	Address to Valid Instr In				$5T_{CLCL}$ - 80 (3V)	ns
			65		$5T_{CLCL}$ - 60 (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10	ns
T_{RLRH}	RD# Pulse Width	120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{WLWH}	Write Pulse Width (WE#)	120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{RLDV}	RD# Low to Valid Data In				$5T_{CLCL}$ - 90 (3V)	ns
			75		$5T_{CLCL}$ - 50 (5V)	ns
T_{RHDX}	Data Hold After RD#	0		0		ns
T_{RHDZ}	Data Float After RD#				$2T_{CLCL}$ - 25 (3V)	ns
			38		$2T_{CLCL}$ - 12 (5V)	ns
T_{LLDV}	ALE Low to Valid Data In				$8T_{CLCL}$ - 90 (3V)	ns
			150		$8T_{CLCL}$ - 50 (5V)	ns
T_{AVDV}	Address to Valid Data In				$9T_{CLCL}$ - 90 (3V)	ns
			150		$9T_{CLCL}$ - 75 (5V)	ns

Not Recommended for New Designs

Revision	Description	Date
00	• Initial Release	Dec 2006
01	• Changed FlashFlex51 to FlashFlex globally	Jan 2007
02	• Removed all 3V parts (89V58RD2A/RDA and 89V54RD2A/RDA) globally • Removed WQFN/ QIF package information globally • Remove all I-grade part information globally	Feb 2008
A	• Applied new document format • Released document under letter revision system • Updated Spec number from S71339 to DS25114	Dec 2011

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