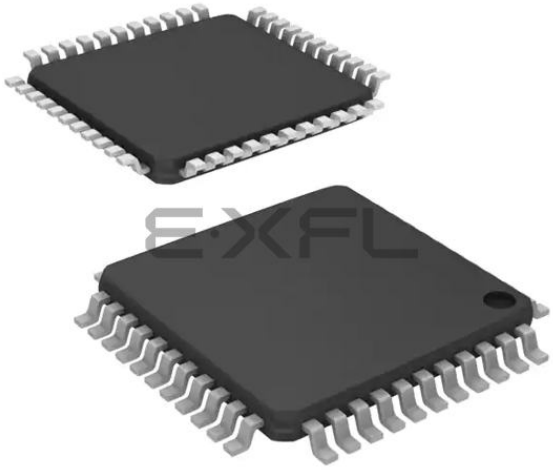

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e54rd2a-40-c-tqje-t

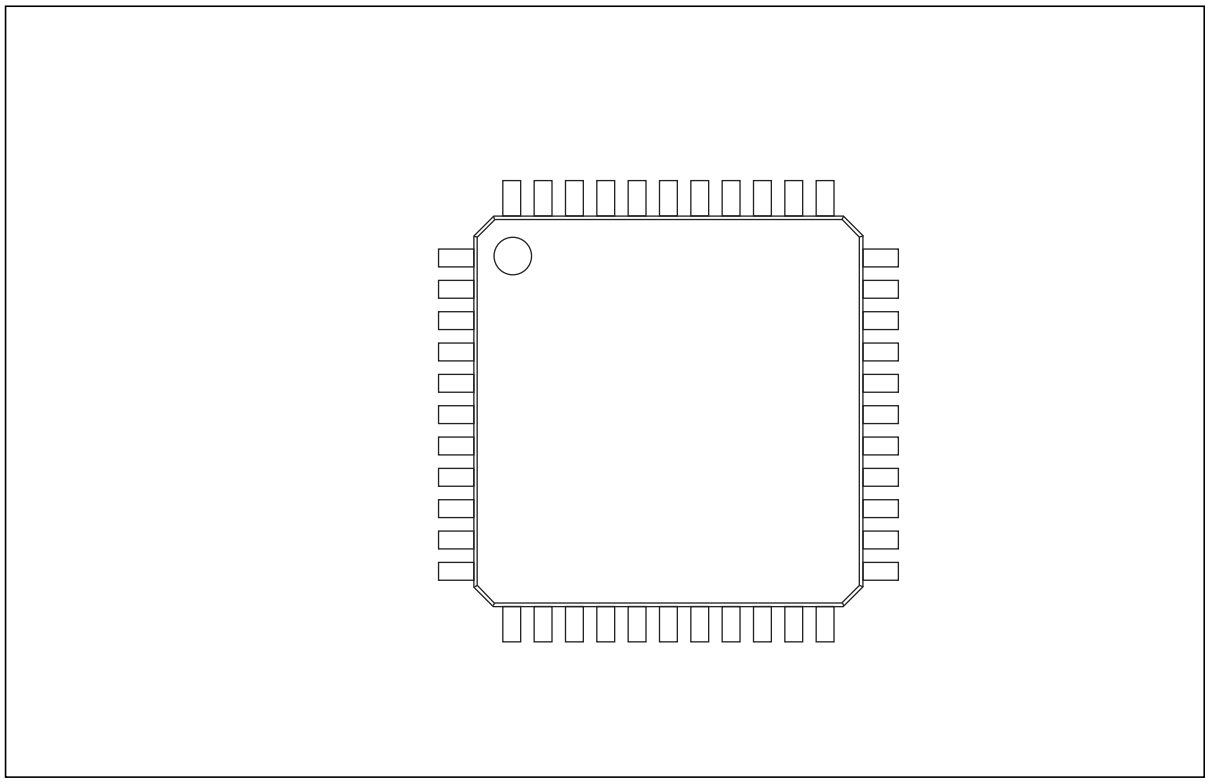

Figure 3: Pin Assignments for 44-lead TQFP

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Table 1: Pin Descriptions (Continued) (3 of 3)

Symbol	Type[1]	Name and Functions
XTAL1	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	**Crystal 2:** Output from the inverting oscillator amplifier
V_{DD}	I	**Power Supply**
V_{SS}	I	**Ground**

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1. I = Input; O = Output
2. ALE loading issue: When ALE pin experiences higher loading (>30pf) during the reset, the MCU may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3-50 KΩ to V_{DD}, e.g. for ALE pin.
3. For 6 clock mode, ALE is emitted at 1/3 of crystal frequency.
4. Port 4 is not present on the PDIP package.

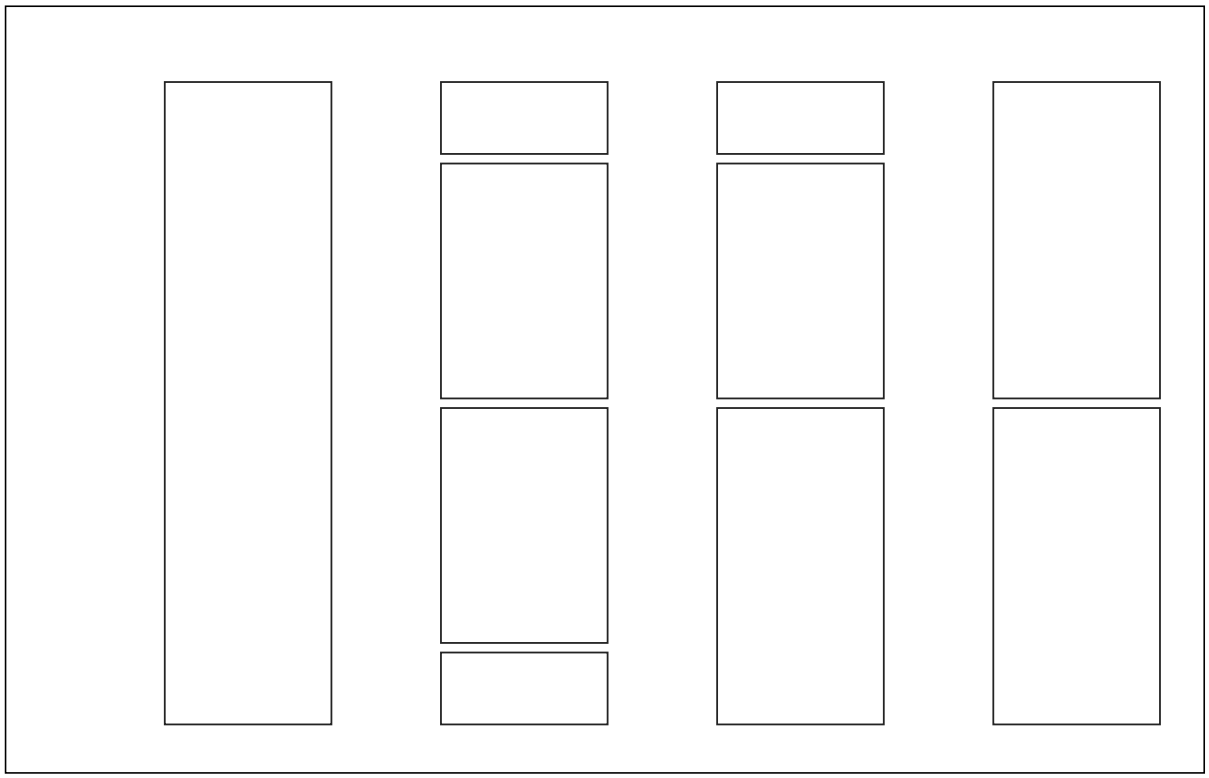

Figure 6: Program Memory Organization for 32 KByte SST89E58RDxA

Program Memory Block Switching

The program memory block switching feature of the device allows either Block 1 or the lowest 8 KByte of Block 0 to be used for the lowest 8 KByte of the program address space. SFCF[1:0] controls program memory block switching.

Table 2: SFCF Values for Program Memory Block Switching

SFCF[1:0]	Program Memory Block Switching
10, 11	Block 1 is not visible to the PC; Block 1 is reachable only via in-application programming from E000H - FFFFH.
01	Both Block 0 and Block 1 are visible to the PC. Block 0 is occupied from 0000H - 7FFFH. Block 1 is occupied from E000H - FFFFH.
00	Block 1 is overlaid onto the low 8K of the program address space; occupying address locations 0000H - 1FFFH. When the PC falls within 0000H - 1FFFH, the instruction will be fetched from Block 1 instead of Block 0. Outside of 0000H - 1FFFH, Block 0 is used. Locations 0000H - 1FFFH of Block 0 are reachable through in-application programming.

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Reset Configuration of Program Memory Block Switching

Program memory block switching is initialized after reset according to the state of the Start-up Configuration bit SC0 and/or SC1. The SC0 and SC1 bits are programmed via an external host mode command or an IAP Mode command. See Table 13.

Once out of reset, the SFCF[0] bit can be changed dynamically by the program for desired effects. Changing SFCF[0] will not change the SC0 bit.

Caution must be taken when dynamically changing the SFCF[0] bit. Since this will cause different physical memory to be mapped to the logical program address space. The user must avoid executing block switching instructions within the address range 0000H to 1FFFH.

Table 3: SFCF Values Under Different Reset Conditions

SC1[1]	SC0[1]	State of SFCF[1:0] after:		
		Power-on or External Reset	WDT Reset or Brown-out Reset	Software Reset
U (1)	U (1)	00 (default)	x0	10
U (1)	P (0)	01	x1	11
P (0)	U (1)	10	10	10
P (0)	P (0)	11	11	11

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1. P = Programmed (Bit logic state = 0),
   U = Unprogrammed (Bit logic state = 1)

Data RAM Memory

The data RAM has 1024 bytes of internal memory. The RAM can be addressed up to 64KB for external data memory.

Expanded Data RAM Addressing

The SST89E/V5xRDxA both have the capability of 1K of RAM. See Figure 7.

The device has four sections of internal data memory:

1. The lower 128 Bytes of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 Bytes of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 768 Bytes (00H to 2FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit. (See “Auxiliary Register (AUXR)” in Section , “Special Function Registers”)

Since the upper 128 bytes occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

When instructions access addresses in the upper 128 bytes (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

MOV@R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in “#data” is written to RAM location 90H rather than port 1.

Direct Access:

MOV90H, #data; write data to P1

Data in “#data” is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 bytes of memory is physically located on the chip and logically occupies the first 768 bytes of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 (WR#), P3.7 (RD#), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

MOVX@DPTR, A; DPTR contains 0A0H

DPTR points to 0A0H and data in “A” is written to address 0A0H of the expanded RAM rather than external memory. Access to external memory higher than 2FFH using the MOVX instruction will access external memory (0300H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX

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Table 11: PCA SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
CH	PCA Timer/Counter	F9H	CH[7:0]								00H
CL		E9H	CL[7:0]								00H
CCON[1]	PCA Timer/Counter Control Register	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000b
CMOD	PCA Timer/Counter Mode Register	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000b
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]								00H
CCAP0L		EAH	CCAP0L[7:0]								00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]								00H
CCAP1L		EBH	CCAP1L[7:0]								00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]								00H
CCAP2L		ECH	CCAP2L[7:0]								00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]								00H
CCAP3L		EDH	CCAP3L[7:0]								00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]								00H
CCAP4L		EEH	CCAP4L[7:0]								00H
CCAPM0	PCA Compare/Capture Module Mode Registers	DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	x0000000b
CCAPM1		DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	x0000000b
CCAPM2		DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	x0000000b
CCAPM3		DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	x0000000b
CCAPM4		DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	x0000000b

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1. Bit Addressable SFRs

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PCA Timer/Counter Mode Register[1] (CMOD)

Location	7	6	5	4	3	2	1	0	Reset Value
D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000b

1. Not bit addressable

Symbol	Function
CIDL	Counter Idle Control: 0: Programs the PCA Counter to continue functioning during idle mode 1: Programs the PCA Counter to be gated off during idle
WDTE	Watchdog Timer Enable: 0: Disables Watchdog Timer function on PCA module 4 1: Enables Watchdog Timer function on PCA module 4
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
CPS1	PCA Count Pulse Select bit 1
CPS0	PCA Count Pulse Select bit 2

CPS1	CPS0	Selected PCA Input[1]	
0	0	0	Internal clock, f_{OSC}/6 in 6 clock mode (f_{OSC}/12 in 12 clock mode)
0	1	1	Internal clock, f_{OSC}/2 in 6 clock mode (f_{OSC}/4 in 12 clock mode)
1	0	2	Timer 0 overflow
1	1	3	External clock at ECI/P1.2 pin
			(max. rate = f_{OSC}/4 in 6 clock mode, f_{OSC}/8 in 12 clock mode)

1. f_{OSC} = oscillator frequency

ECF	PCA Enable Counter Overflow interrupt: 0: Disables the CF bit in CCON 1: Enables CF bit in CCON to generate an interrupt

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Serial I/O

Full-Duplex, Enhanced UART

The device serial I/O port is a full-duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The transmit and receive registers are both located in the Serial Data Buffer (SBUF) special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive register.

The UART has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) SFR is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set.

Framing Error Detection

Framing Error Detection is a feature, which allows the receiving controller to check for valid stop bits in modes 1, 2, or 3. Missing stops bits can be caused by noise in serial lines or from simultaneous transmission by two CPUs.

Framing Error Detection is selected by going to the PCON register and changing SMOD0 = 1 (see Figure 17). If a stop bit is missing, the Framing Error bit (FE) will be set. Software may examine the FE bit after each reception to check for data errors. After the FE bit has been set, it can only be cleared by software. Valid stop bits do not clear FE. When FE is enabled, RI rises on the stop bit, instead of the last data bit (see Figure 18 and Figure 19).

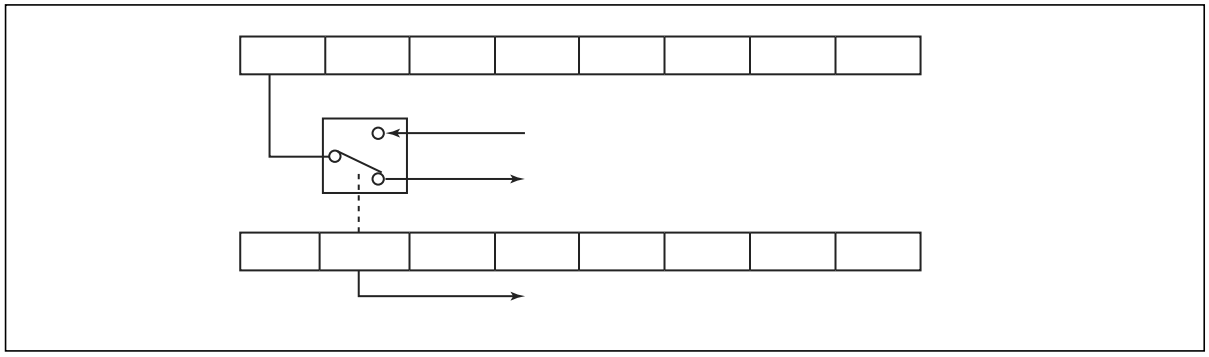

Figure 17: Framing Error Block Diagram

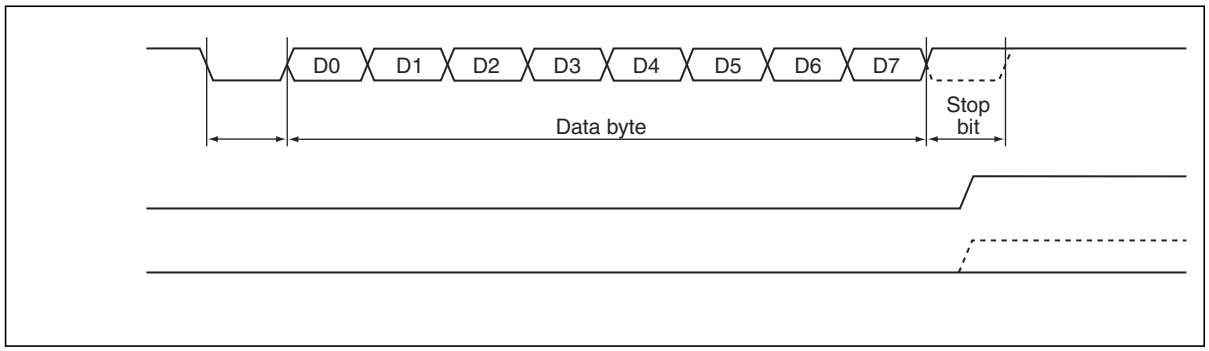

Figure 18: UART Timings in Mode 1

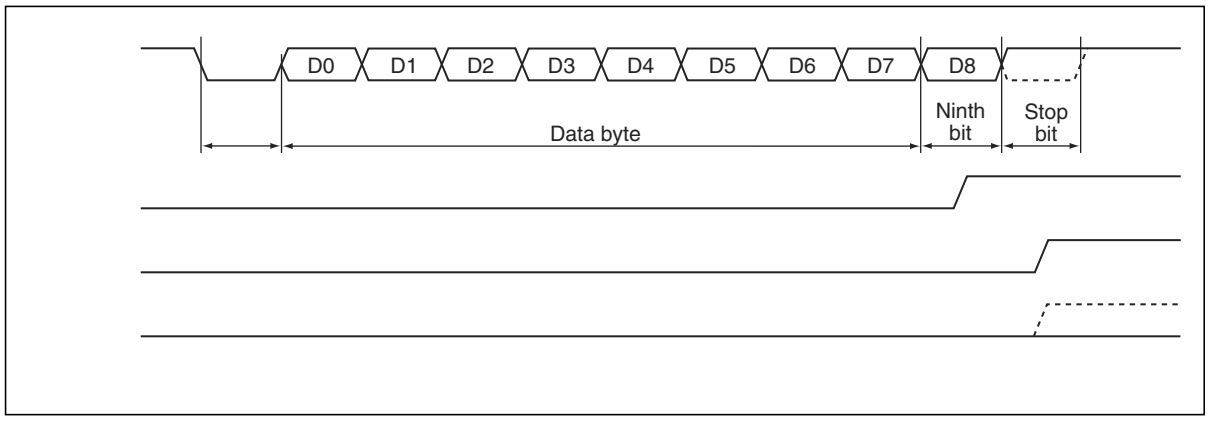

Figure 19: UART Timings in Modes 2 and 3

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Programmable Counter Array

The Programmable Counter Array (PCA) present on the SST89E/V5xRD2A/RDA is a special 16-bit timer that has five 16-bit capture/compare modules. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. The 5th module can be programmed as a Watchdog Timer in addition to the other four modes. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1[4] (CEX1), module 2 to P1[5] (CEX2), module 3 to P1[6] (CEX3), and module 4 to P1[7] (CEX4). PCA configuration is shown in Figure 24.

PCA Overview

PCA provides more timing capabilities with less CPU intervention than the standard timer/counter. Its advantages include reduced software overhead and improved accuracy.

The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/capture modules. Figure 24 shows a block diagram of the PCA. External events associated with modules are shared with corresponding Port 1 pins. Modules not using the port pins can still be used for standard I/O.

Each of the five modules can be programmed in any of the following modes:

- Rising and/or falling edge capture
- Software timer
- High speed output
- Watchdog Timer (Module 4 only)
- Pulse Width Modulator (PWM)

PCA Timer/Counter

The PCA timer is a free-running 16-bit timer consisting of registers CH and CL (the high and low bytes of the count values). The PCA timer is common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, Timer 0 overflow, or the input on the ECI pin (P1.2). The timer/counter source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see “PCA Timer/Counter Mode Register (CMOD)” on page 27):

Table 17: PCA Timer/Counter Source

CPS1	CPS0	12 Clock Mode	6 Clock Mode
0	0	f_{OSC} /12	f_{OSC} /6
0	1	f_{OSC} /4	f_{OSC} /2
1	0	Timer 0 overflow	Timer 0 overflow
1	1	External clock at ECI pin (maximum rate = f_{OSC} /8)	External clock at ECI pin (maximum rate = f_{OSC} /4)

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Table 24: Security Lock Options

Level	Security Lock Bits[1,2]				Security Status of:		Security Type
	SFST[7:5]	SB1	SB2[1]	SB3[1]	Block 1	Block 0	
1	000	U	U	U	Unlock	Unlock	No Security Features are Enabled.
2	100	P	U	U	SoftLock	SoftLock	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA# is sampled and latched on Reset, and further programming of the flash is disabled.
3	011 101	U P	P U	P P	Hard Lock	Hard Lock	Level 2 plus Verify disabled, both blocks locked.
	010	U	P	U	SoftLock	SoftLock	Level 2 plus Verify disabled. Code in Block 1 may program Block 0 and vice versa.
	110 001	P U	P U	U P	Hard Lock	SoftLock	Level 2 plus Verify disabled. Code in Block 1 may program Block 0.
4	111	P	P	P	Hard Lock	Hard Lock	Same as Level 3 hard lock/hard lock, but MCU will start code execution from the internal memory regardless of EA#.

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1. P = Programmed (Bit logic state = 0), U = Unprogrammed (Bit logic state = 1).
2. SFST[7:5] = Security Lock Status Bits (SB1_i, SB2_i, SB3_i)

Read Operation Under Lock Condition

The status of security bits SB1, SB2, and SB3 can be read when the read command is disabled by security lock. There are three ways to read the status.

1. External host mode: Read-back = 00H (locked)
2. IAP command: Read-back = previous SFDT data
3. MOVC: Read-back = FFH (blank)

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Table 25: Security Lock Access Table

Level	SFST[7:5]	Source Address[1]	Target Address[2]	Byte-Verify Allowed		MOVC Allowed
				External Host[3]	IAP	5xRDx
4	111b (hard lock on both blocks)	Block 0/1	Block 0/1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
3	011b/101b (hard lock on both blocks)	Block 0/1	Block 0/1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
	001b/110b (Block 0 = SoftLock, Block 1 = hard lock)	Block 0	Block 0	N	N	Y
			Block 1	N	N	N
			External	N/A	N/A	Y
		Block 1	Block 0	N	Y	Y
			Block 1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
	010b (SoftLock on both blocks)	Block 0	Block 0	N	N	Y
			Block 1	N	Y	Y
			External	N/A	N/A	Y
		Block 1	Block 0	N	Y	Y
			Block 1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
2	100b (SoftLock on both blocks)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	Y
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	Y	N	N
			External	N/A	N/A	Y
1	000b (unlock)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	Y
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	Y	Y	Y
			External	N/A	N/A	Y

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1. Location of MOVC or IAP instruction
2. Target address is the location of the byte being read
3. External host Byte-Verify access does not depend on a source address.

Reset

A system reset initializes the MCU and begins program execution at program memory location 0000H. The reset input for the device is the RST pin. In order to reset the device, a logic level high must be applied to the RST pin for at least two machine cycles (24 clocks), after the oscillator becomes stable. ALE, PSEN# are weakly pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform a proper reset. This level must not be affected by external element. A system reset will not affect the 1 KByte of on-chip RAM while the device is running, however, the contents of the on-chip RAM during power up are indeterminate. Following reset, all Special Function Registers (SFR) return to their reset values outlined in Tables 6 to 10.

Power-on Reset

At initial power up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins high. **Powering up the device without a valid reset could cause the MCU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash.**

When power is applied to the device, the RST pin must be held high long enough for the oscillator to start up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2KΩ resistor as shown in Figure 31. Note that if an RC circuit is being used, provisions should be made to ensure the V_{DD} rise time does not exceed 1 millisecond and the oscillator start-up time does not exceed 10 milliseconds.

For a low frequency oscillator with slow start-up time the reset signal must be extended in order to account for the slow start-up time. This method maintains the necessary relationship between V_{DD} and RST to avoid programming at an indeterminate location, which may cause corruption in the code of the flash. The power-on detection is designed to work as power up initially, before the voltage reaches the brown-out detection level. The POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain active until cleared by software. Please see Section , “Power Control Register (PCON)” on page 30 for detailed information.

For more information on system level design techniques, please review the **FlashFlex MCU: Oscillator Circuit Design Considerations** application note.

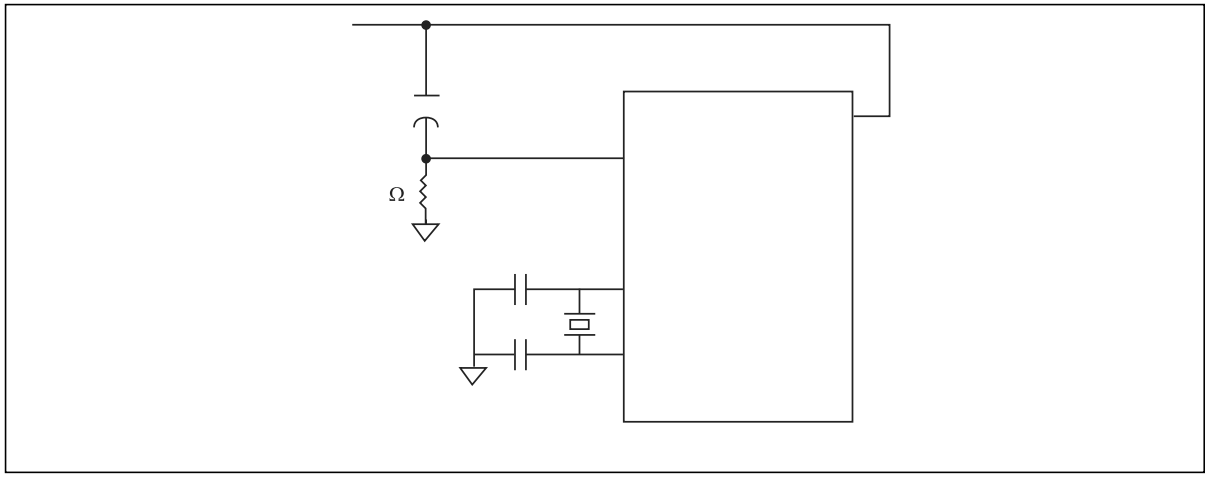

Figure 31: Power-on Reset Circuit

Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 29 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 13 for the IAP mode enabling commands (When set, the EDC# bit in SFST register will indicate 6 clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

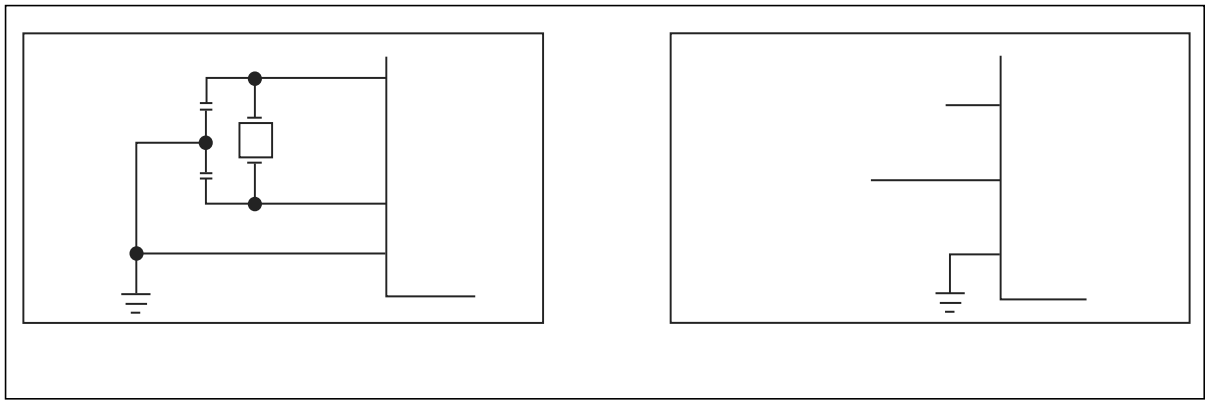

Figure 33: Oscillator Characteristics

Table 29: Clock Doubling Features

Device	Standard Mode (x1)		Clock Double Mode (x2)	
	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)
SST89E5xRD2A/RDA	12	40	6	20

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Table 35: DC Electrical Characteristics for SST89E5xRD2A/RDA
T_A = -40°C to +85°C; V_{DD} = 4.5-5.5V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	4.5 < V_{DD} < 5.5	-0.5	0.2V_{DD} - 0.1	V
V_{IH}	Input High Voltage	4.5 < V_{DD} < 5.5	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	4.5 < V_{DD} < 5.5	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 4.5V			
		I_{OL} = 16mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 4.5V			
		I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 4.5V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 4.5V			
		I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 4.5V			
		I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
V_{BOD}	Brown-out Detection Voltage		3.85	4.15	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}- 0.3		±10	µA
R_{RST}	RST Pull-down Resistor		40	225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current IAP Mode @ 40 MHz			88	mA
	Active Mode @ 40 MHz			50	mA
	Idle Mode @ 40 MHz			42	mA
	Power-down Mode	T_A = 0°C to +70°C		80	µA
		T_A = -40°C to +85°C		90	µA

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AC Electrical Characteristics

AC Characteristics:

(Over Operating Conditions: Load Capacitance for Port 0, ALE#, and PSEN# = 100pF; Load Capacitance for All Other Outputs = 80pF)

Table 36: AC Electrical Characteristics (1 of 2)
T_A = -40°C to +85°C, V_{DD} = 4.5-5.5V@40MHz, V_{SS} = 0V

		Oscillator				
		40 MHz (x1 Mode) 20 MHz (x2 Mode)		Variable		
Symbol	Parameter	Min	Max	Min	Max	Units
$1/T_{CLCL}$	x1 Mode Oscillator Frequency	0	40	0	40	MHz
$1/2T_{CLCL}$	x2 Mode Oscillator Frequency	0	20	0	20	MHz
T_{LHLL}	ALE Pulse Width	35		$2T_{CLCL}$ - 15		ns
T_{AVLL}	Address Valid to ALE Low			T_{CLCL} - 25 (3V)		ns
		10		T_{CLCL} - 15 (5V)		ns
T_{LLAX}	Address Hold After ALE Low			T_{CLCL} - 25 (3V)		ns
		10		T_{CLCL} - 15 (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In				$4T_{CLCL}$ - 65 (3V)	ns
			55		$4T_{CLCL}$ - 45 (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low			T_{CLCL} - 25 (3V)		ns
		10		T_{CLCL} - 15 (5V)		ns
T_{PLPH}	PSEN# Pulse Width	60		$3T_{CLCL}$ - 25 (3V) $3T_{CLCL}$ - 15 (5V)		ns
T_{PLIV}	PSEN# Low to Valid Instr In				$3T_{CLCL}$ - 55 (3V)	ns
			25		$3T_{CLCL}$ - 50 (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#			0		ns
T_{PXIZ}	Input Instr Float After PSEN#				T_{CLCL} - 5 (3V)	ns
			10		T_{CLCL} - 15 (5V)	ns
T_{PXAV}	PSEN# to Address valid	17		T_{CLCL} - 8		ns
T_{AVIV}	Address to Valid Instr In				$5T_{CLCL}$ - 80 (3V)	ns
			65		$5T_{CLCL}$ - 60 (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10	ns
T_{RLRH}	RD# Pulse Width	120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{WLWH}	Write Pulse Width (WE#)	120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{RLDV}	RD# Low to Valid Data In				$5T_{CLCL}$ - 90 (3V)	ns
			75		$5T_{CLCL}$ - 50 (5V)	ns
T_{RHDX}	Data Hold After RD#	0		0		ns
T_{RHDZ}	Data Float After RD#				$2T_{CLCL}$ - 25 (3V)	ns
			38		$2T_{CLCL}$ - 12 (5V)	ns
T_{LLDV}	ALE Low to Valid Data In				$8T_{CLCL}$ - 90 (3V)	ns
			150		$8T_{CLCL}$ - 50 (5V)	ns
T_{AVDV}	Address to Valid Data In				$9T_{CLCL}$ - 90 (3V)	ns
			150		$9T_{CLCL}$ - 75 (5V)	ns

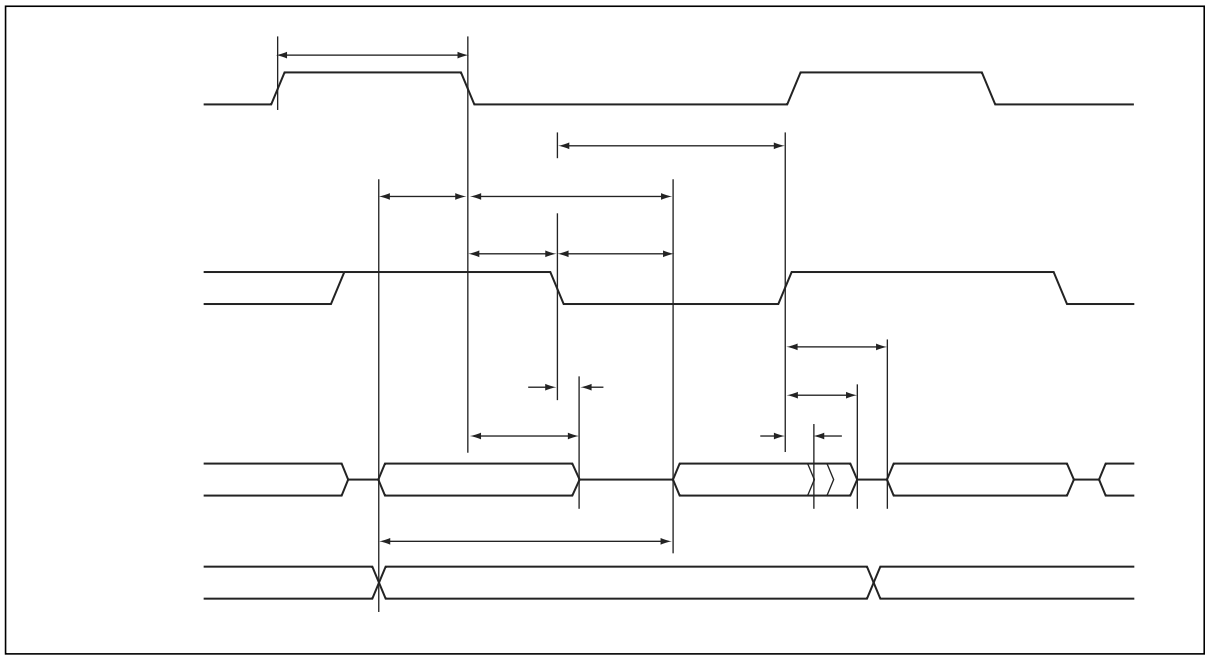

Figure 35: External Program Memory Read Cycle

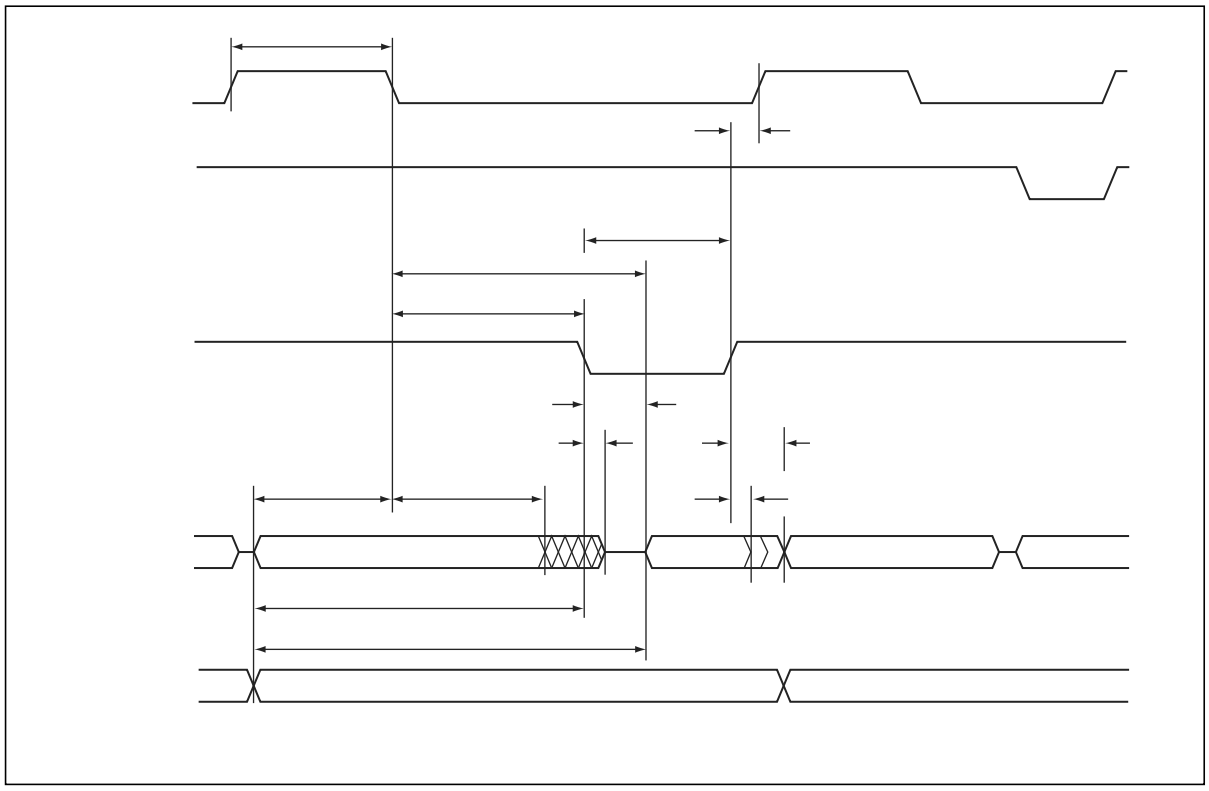

Figure 36: External Data Memory Read Cycle

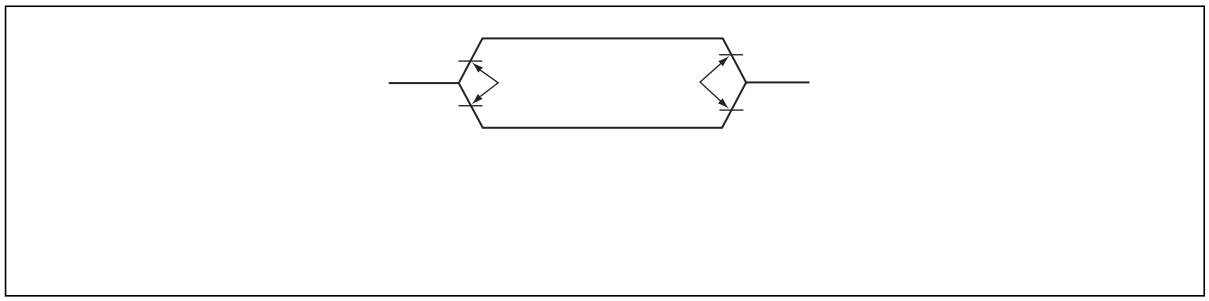

Figure 41: Float Waveform

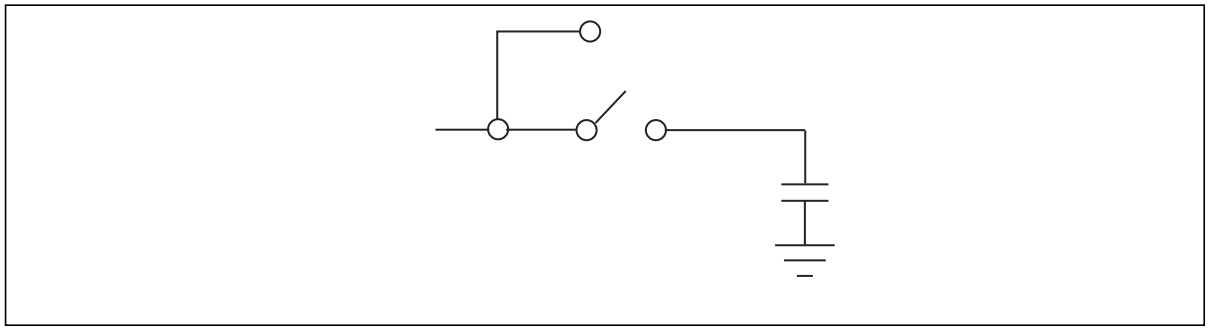

Figure 42: A Test Load Example

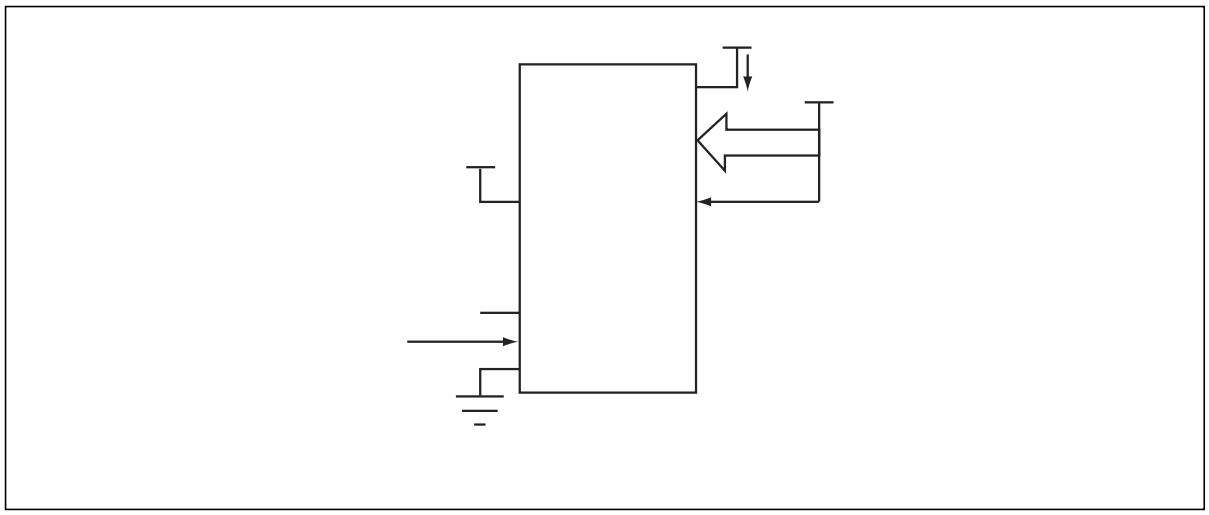

Figure 43: I_{DD} Test Condition, Active Mode

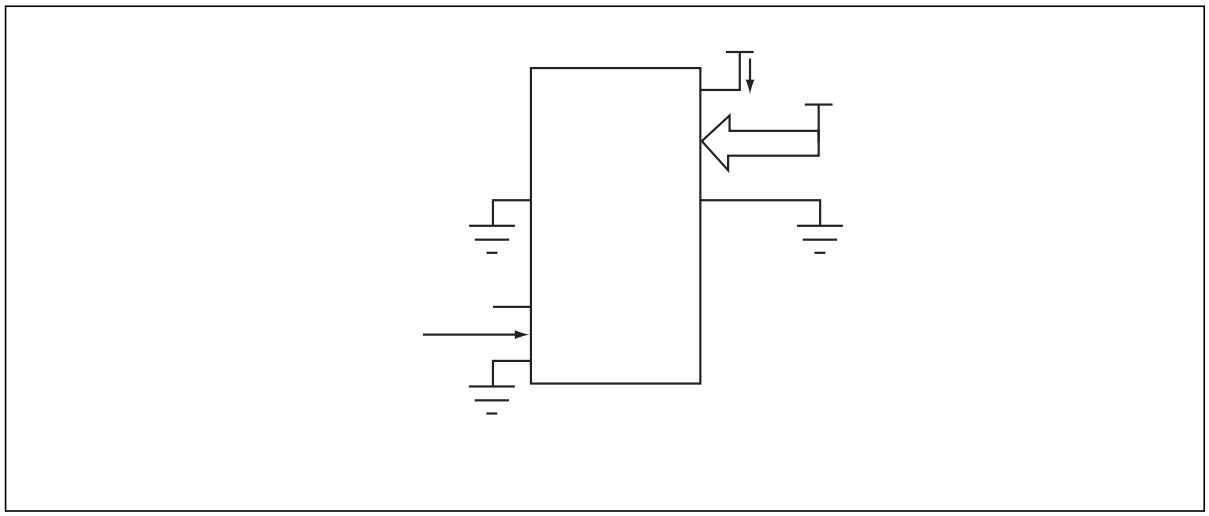

Figure 44: I_{DD} Test Condition, Idle Mode

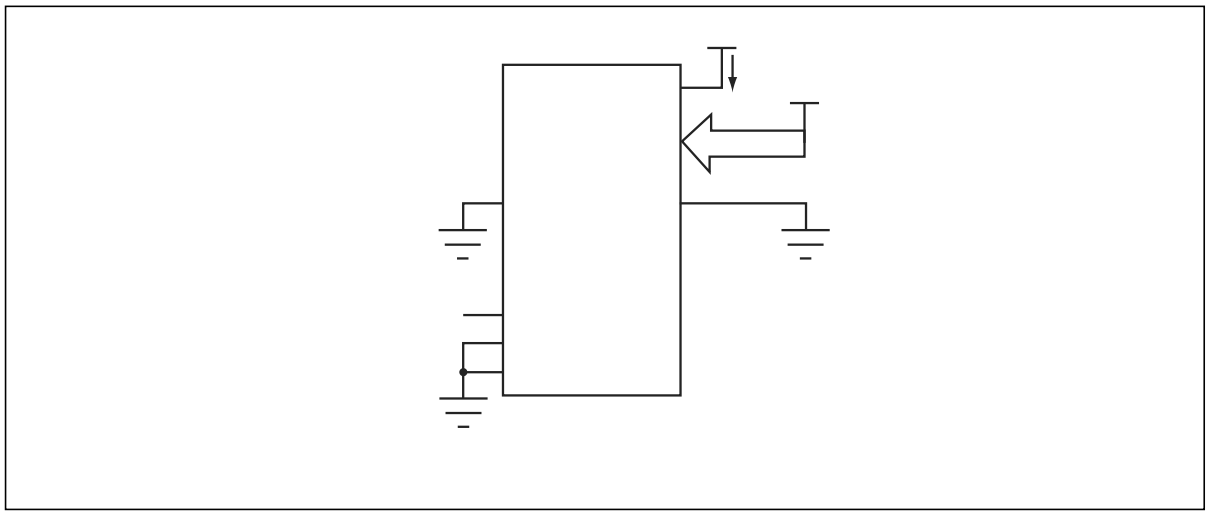

Figure 45: I_{DD} Test Condition, Power-down Mode

Table 38: Flash Memory Programming/Verification Parameters[1]

Parameter[2]	Max	Units
Chip-Erase Time	150	ms
Block-Erase Time	100	ms
Sector-Erase Time	30	ms
Byte-Program Time[3]	50	µs
Re-map or Security bit Program Time	80	µs

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1. For IAP operations, the program execution overhead must be added to the above timing parameters.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. Each byte must be erased before programming.

Not Recommended for New Designs

Valid Combinations

Valid combinations for SST89E54RD2A

SST89E54RD2A-40-C-NJE SST89E54RD2A-40-C-TQJE

Valid combinations for SST89E58RD2A

SST89E58RD2A-40-C-NJE SST89E58RD2A-40-C-TQJE

Valid combinations for SST89E54RDA

SST89E54RDA-40-C-PIE

Valid combinations for SST89E58RDA

SST89E58RDA-40-C-PIE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.