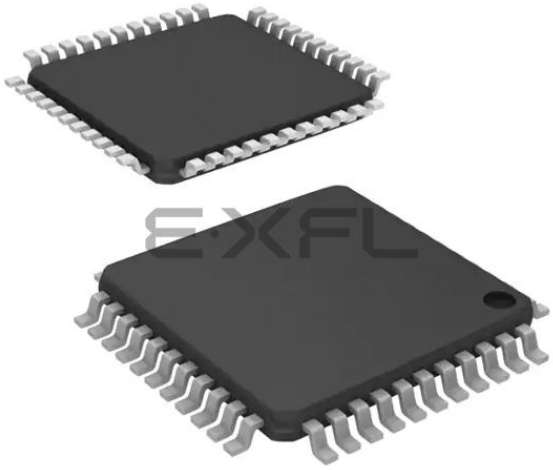

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	40KB (40K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e58rd2-40-c-tqje

Not Recommended for New Designs

Product Description

The SST89E54RD2A/RDA and SST89E58RD2A/RDA are members of the FlashFlex family of 8-bit microcontroller products designed and manufactured with SST patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for SST customers. The devices use the 8051 instruction set and are pin-for-pin compatible with standard 8051 microcontroller devices.

The devices come with 24/40 KByte of on-chip flash EEPROM program memory which is partitioned into 2 independent program memory blocks. The primary Block 0 occupies 16/32 KByte of internal program memory space and the secondary Block 1 occupies 8 KByte of internal program memory space.

The 8-KByte secondary block can be mapped to the lowest location of the 16/32 KByte address space; it can also be hidden from the program counter and used as an independent EEPROM-like data memory.

In addition to the 24/40 KByte of EEPROM program memory on-chip and 1024 x8 bits of on-chip RAM, the devices can address up to 64 KByte of external program memory and up to 64 KByte of external RAM.

The flash memory blocks can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and the firmware for SST devices. During power-on reset, the devices can be configured as either a slave to an external host for source code storage or a master to an external host for an in-application programming (IAP) operation. The devices are designed to be programmed in-system and in-application on the printed circuit board for maximum flexibility. The devices are pre-programmed with an example of the bootstrap loader in the memory, demonstrating the initial user program code loading or subsequent user code updating via the IAP operation. The sample bootstrap loader is available for the user's reference and convenience only; SST does not guarantee its functionality or usefulness. Chip-Erase or Block-Erase operations will erase the pre-programmed sample code.

Expanded Data RAM Addressing

The SST89E/V5xRDxA both have the capability of 1K of RAM. See Figure 7.

The device has four sections of internal data memory:

1. The lower 128 Bytes of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 Bytes of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 768 Bytes (00H to 2FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit. (See “Auxiliary Register (AUXR)” in Section , “Special Function Registers”)

Since the upper 128 bytes occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

When instructions access addresses in the upper 128 bytes (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

MOV@R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in “#data” is written to RAM location 90H rather than port 1.

Direct Access:

MOV90H, #data; write data to P1

Data in “#data” is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 bytes of memory is physically located on the chip and logically occupies the first 768 bytes of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 (WR#), P3.7 (RD#), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

MOVX@DPTR, A; DPTR contains 0A0H

DPTR points to 0A0H and data in “A” is written to address 0A0H of the expanded RAM rather than external memory. Access to external memory higher than 2FFH using the MOVX instruction will access external memory (0300H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX

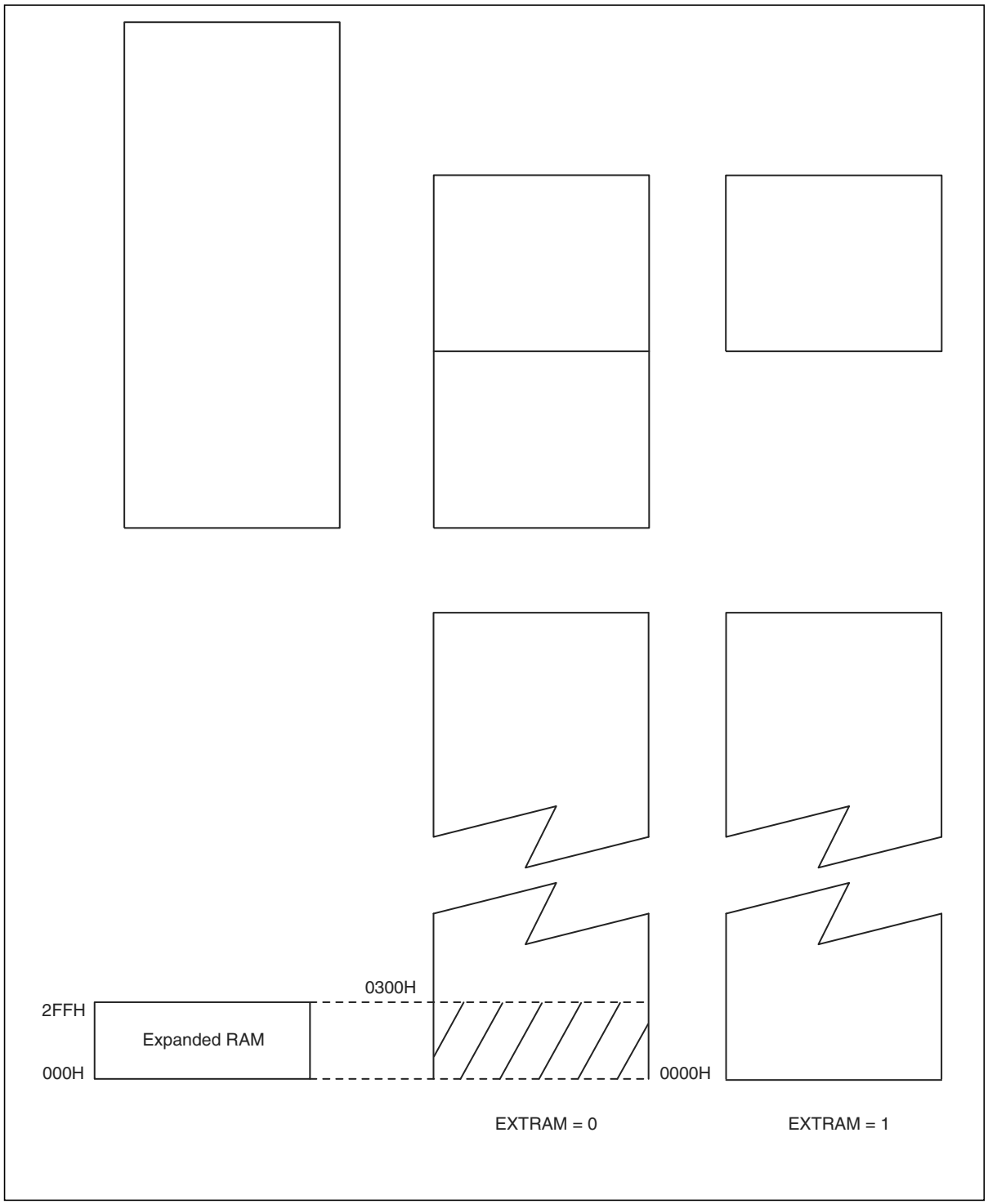

Figure 7: Internal and External Data Memory Structure

Not Recommended for New Designs

SuperFlash Address Registers (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
B4H	SuperFlash High Order Byte Address Register								00H

Symbol	Function
SFAH	Mailbox register for interfacing with flash memory block. (High order address register).

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
B5H	SuperFlash Data Register								00H

Symbol	Function
SFDT	Mailbox register for interfacing with flash memory block. (Data register).

SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BUSY	-	-	xxxxx0xxb

Symbol	Function
SB1_i	Security Bit 1 status (inverse of SB1 bit)
SB2_i	Security Bit 2 status (inverse of SB2 bit)
SB3_i	Security Bit 3 status (inverse of SB3 bit) Please refer to Table 25 for security lock options.
EDC_i	Double Clock Status 0: 12 clocks per machine cycle 1: 6 clocks per machine cycle
FLASH_BUSY	Flash operation completion polling bit. 0: Device has fully completed the last IAP command. 1: Device is busy with flash operation.

Not Recommended for New Designs

Interrupt Enable (IE)

Location	7	6	5	4	3	2	1	0	Reset Value
A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H

Symbol	Function
EA	Global Interrupt Enable. 0 = Disable 1 = Enable
EC	PCA Interrupt Enable.
ET2	Timer 2 Interrupt Enable.
ES	Serial Interrupt Enable.
ET1	Timer 1 Interrupt Enable.
EX1	External 1 Interrupt Enable.
ET0	Timer 0 Interrupt Enable.
EX0	External 0 Interrupt Enable.

Interrupt Enable A (IEA)

Location	7	6	5	4	3	2	1	0	Reset Value
E8H	-	-	-	-	EBO	-	-	-	xxxx0xxxb

Symbol	Function
EBO	Brown-out Interrupt Enable. 1 = Enable the interrupt 0 = Disable the interrupt

Interrupt Priority (IP)

Location	7	6	5	4	3	2	1	0	Reset Value
B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000b

Symbol	Function
PPC	PCA interrupt priority bit
PT2	Timer 2 interrupt priority bit
PS	Serial Port interrupt priority bit
PT1	Timer 1 interrupt priority bit
PX1	External interrupt 1 priority bit
PT0	Timer 0 interrupt priority bit
PX0	External interrupt 0 priority bit

Not Recommended for New Designs

PCA Timer/Counter Mode Register[1] (CMOD)

Location	7	6	5	4	3	2	1	0	Reset Value
D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000b

1. Not bit addressable

Symbol	Function
CIDL	Counter Idle Control: 0: Programs the PCA Counter to continue functioning during idle mode 1: Programs the PCA Counter to be gated off during idle
WDTE	Watchdog Timer Enable: 0: Disables Watchdog Timer function on PCA module 4 1: Enables Watchdog Timer function on PCA module 4
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
CPS1	PCA Count Pulse Select bit 1
CPS0	PCA Count Pulse Select bit 2

CPS1	CPS0	Selected PCA Input[1]	
0	0	0	Internal clock, f_{OSC}/6 in 6 clock mode (f_{OSC}/12 in 12 clock mode)
0	1	1	Internal clock, f_{OSC}/2 in 6 clock mode (f_{OSC}/4 in 12 clock mode)
1	0	2	Timer 0 overflow
1	1	3	External clock at ECI/P1.2 pin
			(max. rate = f_{OSC}/4 in 6 clock mode, f_{OSC}/8 in 12 clock mode)

1. f_{OSC} = oscillator frequency

ECF	PCA Enable Counter Overflow interrupt: 0: Disables the CF bit in CCON 1: Enables CF bit in CCON to generate an interrupt

Not Recommended for New Designs

SPI Control Register (SPCR)

Location	7	6	5	4	3	2	1	0	Reset Value
D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	00H

Symbol	Function
SPIE	If both SPIE and ES are set to one, SPI interrupts are enabled.
SPE	SPI enable bit. 0: Disables SPI. 1: Enables SPI and connects SS#, MOSI, MISO, and SCK to pins P1.4, P1.5, P1.6, P1.7.
DORD	Data Transmission Order. 0: MSB first in data transmission. 1: LSB first in data transmission.
MSTR	Master/Slave select. 0: Selects Slave mode. 1: Selects Master mode.
CPOL	Clock Polarity 0: SCK is low when idle (Active High). 1: SCK is high when idle (Active Low).
CPHA	Clock Phase control bit. The CPHA bit with the CPOL bit control the clock and data relationship between master and slave. See Figures 21 and 22. 0: Shift triggered on the leading edge of the clock. 1: Shift triggered on the trailing edge of the clock.
SPR1, SPR0	SPI Clock Rate Select bits. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, f_{OSC}, is as follows:

SPR1	SPR0	SCK = f_{OSC} divided by
0	0	4
0	1	16
1	0	64
1	1	128

SPI Status Register (SPSR)

Location	7	6	5	4	3	2	1	0	Reset Value
AAH	SPIF	WCOL	-	-	-	-	-	-	00xxxxxxb

Symbol	Function
SPIF	SPI Interrupt Flag. Upon completion of data transfer, this bit is set to 1. If SPIE =1 and ES =1, an interrupt is then generated. This bit is cleared by software.
WCOL	Write Collision Flag. Set if the SPI data register is written to during data transfer. This bit is cleared by software.

Not Recommended for New Designs

Serial Port Control Register (SCON)

Location	7	6	5	4	3	2	1	0	Reset Value
98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00000000b

Symbol	Function
FE	Set SMOD0 = 1 to access FE bit. 0: No framing error 1: Framing Error. Set by receiver when an invalid stop bit is detected. This bit needs to be cleared by software.
SM0	SMOD0 = 0 to access SM0 bit. Serial Port Mode Bit 0
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate[1]
0	0	0	Shift Register	f_{OSC}/6 (6 clock mode) or f_{OSC}/12 (12 clock mode)
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	f_{OSC}/32 or f_{OSC}/16 (6 clock mode) or f_{OSC}/64 or f_{OSC}/32 (12 clock mode)
1	1	3	9-bit UART	Variable

1. f_{OSC} = oscillator frequency

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a given or broadcast address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be 0.
REN	Enables serial reception. 0: to disable reception. 1: to enable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission, Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Not Recommended for New Designs

Timer/Counter 2 Control Register (T2CON)

Location	7	6	5	4	3	2	1	0	Reset Value
C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflow to be used for the transmit clock.
EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2#	Timer or counter select (Timer 2) 0: Internal timer (OSC/6 in 6 clock mode, OSC/12 in 12 clock mode) 1: External event counter (falling edge triggered)
CP/RL2#	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Timer/Counter 2 Mode Control (T2MOD)

Location	7	6	5	4	3	2	1	0	Reset Value
C9H	X	-	-	-	-	-	T2OE	DCEN	xxxxxx00b

Symbol	Function
X	Don't Care
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

Byte-Program

The Byte-Program command programs data into a single byte. The address is determined by the contents of SFAH and SFAL. The data byte is in SFDT.

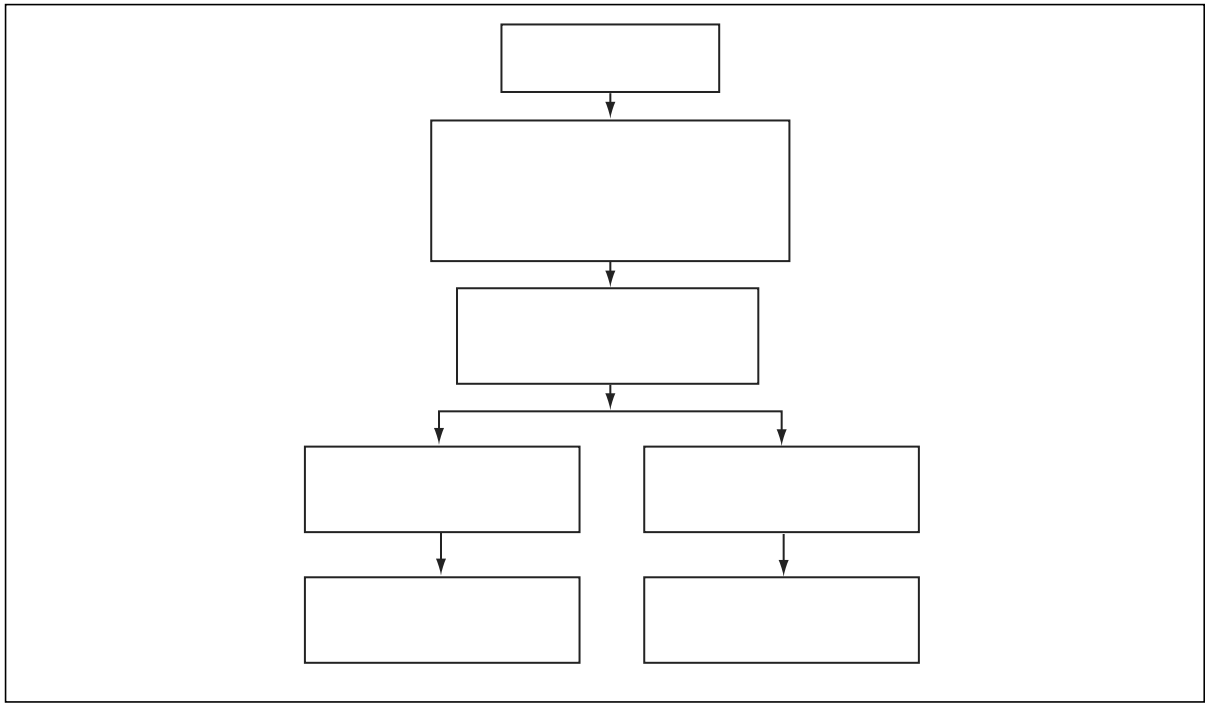

Figure 12: Byte-Program

Not Recommended for New Designs

Interrupt Termination

If interrupt termination is selected, (SFCM[7] is set), then an interrupt (INT1) will be generated to indicate flash operation completion. Under this condition, the INT1 becomes an internal interrupt source. The INT1# pin can now be used as a general purpose port pin and it cannot be the source of External Interrupt 1 during in-application programming.

In order to use an interrupt to signal flash operation termination. EX1 and EA bits of IE register must be set. The IT1 bit of TCON register must also be set for edge trigger detection.

Table 13: IAP Commands

Operation	SFCM [6:0][1]	SFDT [7:0]	SFAH [7:0]	SFAL [7:0]
Chip-Erase[2]	01H	55H	X[3]	X
Block-Erase	0DH	55H	AH[4]	X
Sector-Erase	0BH	X	AH	AL[5]
Byte-Program	0EH	DI[6]	AH	AL
Byte-Verify (Read)[7]	0CH	DO[6]	AH	AL
Prog-SB1[8]	0FH	AAH	X	X
Prog-SB2[8]	03H	AAH	X	X
Prog-SB3[8]	05H	AAH	X	X
Prog-SC0[8]	09H	AAH	5AH	X
Prog-SC1[8]	09H	AAH	AAH	X
Enable-Clock-Double[8]	08H	AAH	55H	X

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1. Interrupt/Polling enable for flash operation completion
   SFCM[7] =1: Interrupt enable for flash operation completion
   0: polling enable for flash operation completion
2. Chip-Erase only functions in IAP mode when EA#=0 (external memory execution) and device is not in level 4 locking.
3. X can be V_{IL} or V_{IH}, but no other value.
4. AH = Address high order byte
5. AL = Address low order byte
6. DI = Data Input, DO = Data Output, all other values are in hex.
7. SFAH[7:5] = 111b selects Block 1, SFAH[7] = 0b selects Block 0
8. Instruction must be located in Block 1 or external code memory.

Note: DISIAPL pin in PLCC or TQFP will also disable IAP commands if it is externally pulled low when reset.

Not Recommended for New Designs

Capture Mode

Capture mode is used to capture the PCA timer/counter value into a module's capture registers (CCAPnH and CCAPnL). The capture will occur on a positive edge, negative edge, or both on the corresponding module's pin. To use one of the PCA modules in the capture mode, either one or both the CCAPM bits CAPN and CAPP for that module must be set. When a valid transition occurs on the CEX pin corresponding to the module used, the PCA hardware loads the 16-bit value of the PCA counter register (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set, then an interrupt will be generated. In the interrupt service routine, the 16-bit capture value must be saved in RAM before the next event capture occurs. If a subsequent capture occurred, the original capture values would be lost. After flag event flag has been set by hardware, the user must clear the flag in software. (See Figure 25)

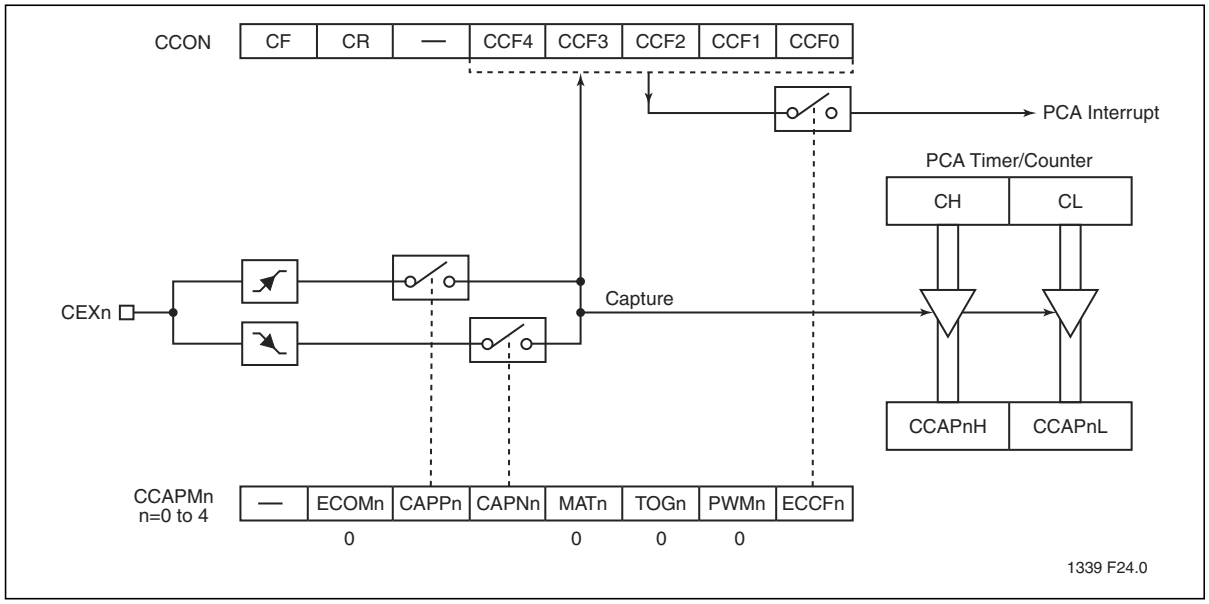

Figure 25: PCA Capture Mode

Not Recommended for New Designs

Table 24: Security Lock Options

Level	Security Lock Bits[1,2]				Security Status of:		Security Type
	SFST[7:5]	SB1	SB2[1]	SB3[1]	Block 1	Block 0	
1	000	U	U	U	Unlock	Unlock	No Security Features are Enabled.
2	100	P	U	U	SoftLock	SoftLock	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA# is sampled and latched on Reset, and further programming of the flash is disabled.
3	011 101	U P	P U	P P	Hard Lock	Hard Lock	Level 2 plus Verify disabled, both blocks locked.
	010	U	P	U	SoftLock	SoftLock	Level 2 plus Verify disabled. Code in Block 1 may program Block 0 and vice versa.
	110 001	P U	P U	U P	Hard Lock	SoftLock	Level 2 plus Verify disabled. Code in Block 1 may program Block 0.
4	111	P	P	P	Hard Lock	Hard Lock	Same as Level 3 hard lock/hard lock, but MCU will start code execution from the internal memory regardless of EA#.

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1. P = Programmed (Bit logic state = 0), U = Unprogrammed (Bit logic state = 1).
2. SFST[7:5] = Security Lock Status Bits (SB1_i, SB2_i, SB3_i)

Read Operation Under Lock Condition

The status of security bits SB1, SB2, and SB3 can be read when the read command is disabled by security lock. There are three ways to read the status.

1. External host mode: Read-back = 00H (locked)
2. IAP command: Read-back = previous SFDT data
3. MOVC: Read-back = FFH (blank)

Not Recommended for New Designs

Table 25: Security Lock Access Table

Level	SFST[7:5]	Source Address[1]	Target Address[2]	Byte-Verify Allowed		MOVC Allowed
				External Host[3]	IAP	5xRDx
4	111b (hard lock on both blocks)	Block 0/1	Block 0/1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
3	011b/101b (hard lock on both blocks)	Block 0/1	Block 0/1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
	001b/110b (Block 0 = SoftLock, Block 1 = hard lock)	Block 0	Block 0	N	N	Y
			Block 1	N	N	N
			External	N/A	N/A	Y
		Block 1	Block 0	N	Y	Y
			Block 1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
	010b (SoftLock on both blocks)	Block 0	Block 0	N	N	Y
			Block 1	N	Y	Y
			External	N/A	N/A	Y
		Block 1	Block 0	N	Y	Y
			Block 1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
2	100b (SoftLock on both blocks)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	Y
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	Y	N	N
			External	N/A	N/A	Y
1	000b (unlock)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	Y
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	Y	Y	Y
			External	N/A	N/A	Y

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1. Location of MOVC or IAP instruction
2. Target address is the location of the byte being read
3. External host Byte-Verify access does not depend on a source address.

System Clock and Clock Options

Clock Input Options and Recommended Capacitor Values for Oscillator

Shown in Figure 33 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 28, shows the typical values for C1 and C2 vs. crystal type for various frequencies

Table 28: Recommended Values for C1 and C2 by Crystal Type

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

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More specific information about on-chip oscillator design can be found in the ***FlashFlex Oscillator Circuit Design Considerations*** application note.

Not Recommended for New Designs

Electrical Specification

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature. . . . . -65°C to +150°C
Voltage on EA# Pin to V_{SS}. . . . . -0.5V to +14.0V
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20ns) on Any Other Pin to V_{SS} . . . . . -1.0V to V_{DD}+1.0V
Maximum I_{OL} per I/O Pins P1.5, P1.6, P1.7 . . . . . 20mA
Maximum I_{OL} per I/O for All Other Pins 15mA
Package Power Dissipation Capability (T_A = 25°C). 1.5W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Solder Reflow Temperature[1]. . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.
(Based on package heat transfer limitations, not device power consumption.

Note: This specification contains preliminary information on new products in production.
Specifications are subject to change without notice.

Table 30: Operating Range

Symbol	Description	Min.	Max	Unit
T_A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
V_{DD}	Supply Voltage			
	SST89E5xRD2A/RDA	4.5	5.5	V
f_{OSC}	Oscillator Frequency			
	SST89E5xRD2A/RDA	0	40	MHz
	Oscillator Frequency for IAP			
	SST89E5xRD2A/RDA	0.25	40	MHz

T0-0.0 25114

Table 31: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T0-0.0 25114

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 32: AC Conditions of Test[1]

Input Rise/Fall Time	Output Load
10ns	C_L = 100 pF

T32.1 25114

1. See Figures 40 and 42

Table 33: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T0-0.2 25114

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

Table 34: Pin Impedance (VDD=3.3V, TA=25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF
L_{PIN}[2]	Pin Inductance		20 nH

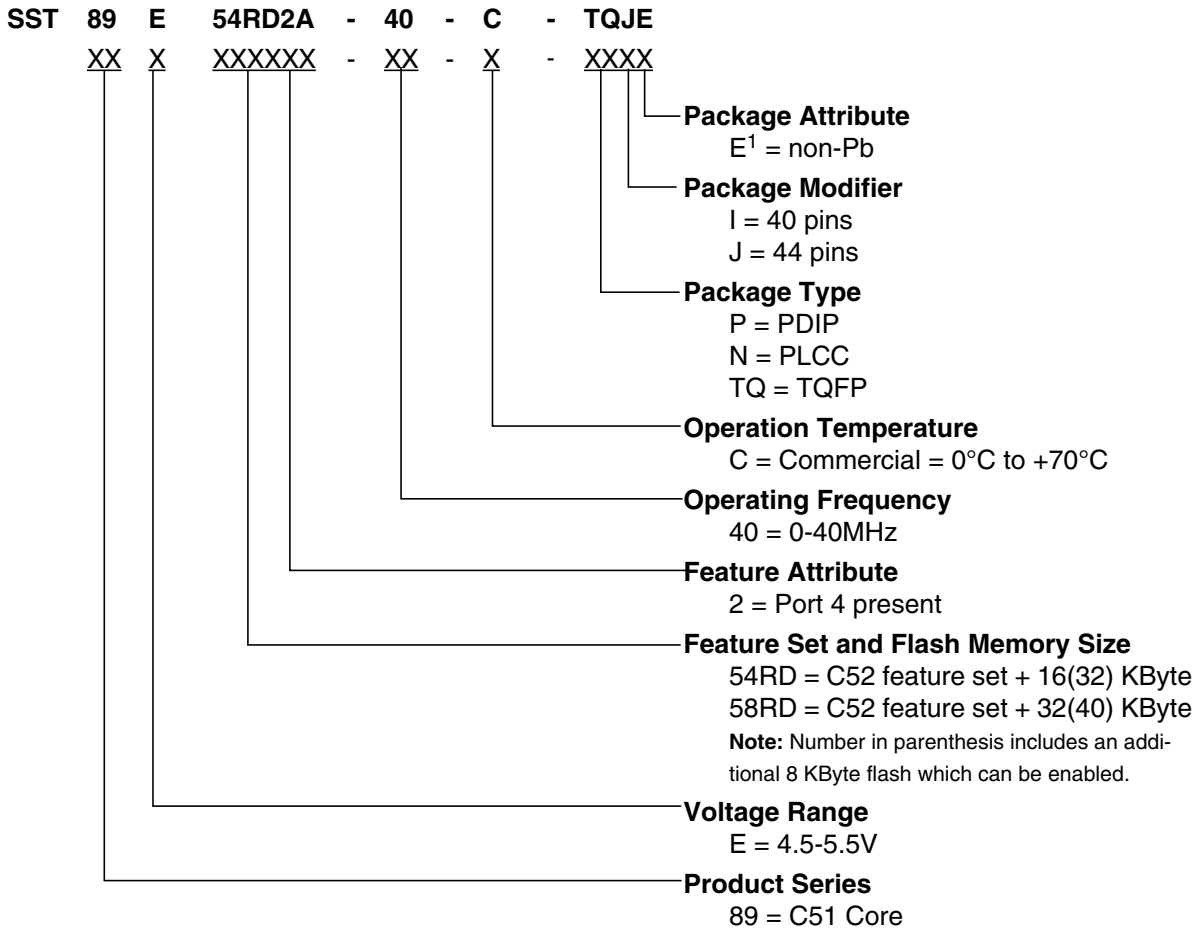
T0-0.4 25114

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI spec.

DC Electrical Characteristics

Not Recommended for New Designs

Product Ordering Information



1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

Packaging Diagrams

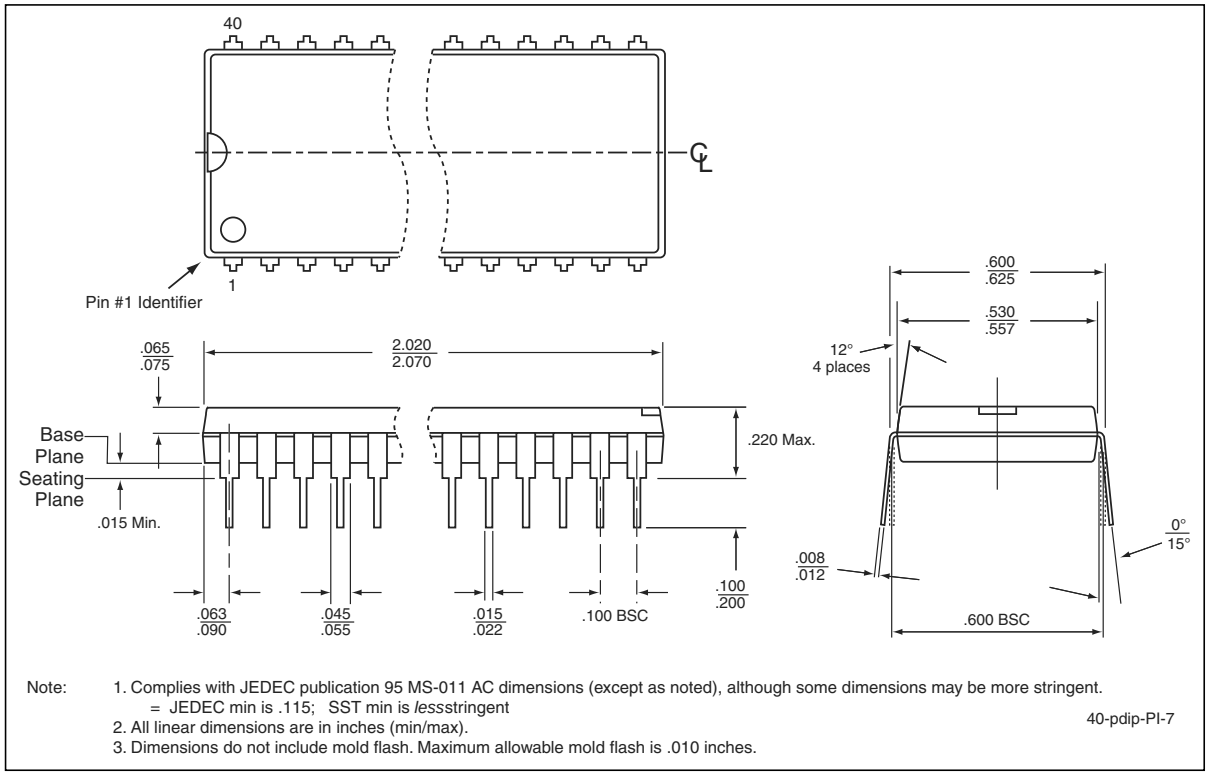


Figure 46: 40-Pin Plastic Dual In-line Pins (PDIP)
SST Package Code: PI

Not Recommended for New Designs

Revision	Description	Date
00	• Initial Release	Dec 2006
01	• Changed FlashFlex51 to FlashFlex globally	Jan 2007
02	• Removed all 3V parts (89V58RD2A/RDA and 89V54RD2A/RDA) globally • Removed WQFN/ QIF package information globally • Remove all I-grade part information globally	Feb 2008
A	• Applied new document format • Released document under letter revision system • Updated Spec number from S71339 to DS25114	Dec 2011

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