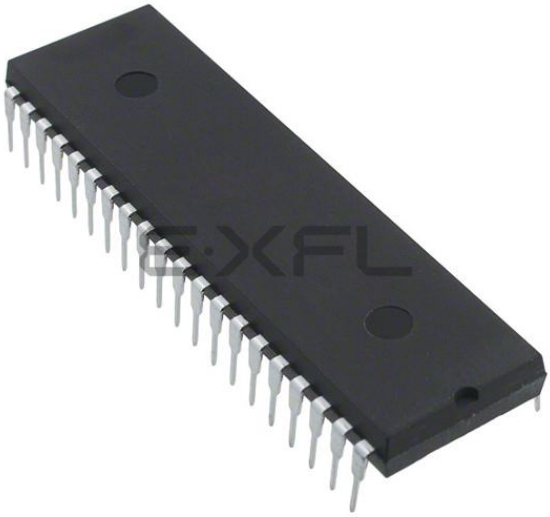
Microchip Technology - SST89E58RDA-40-C-PIE Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	32
Program Memory Size	40KB (40K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e58rda-40-c-pie

Functional Blocks

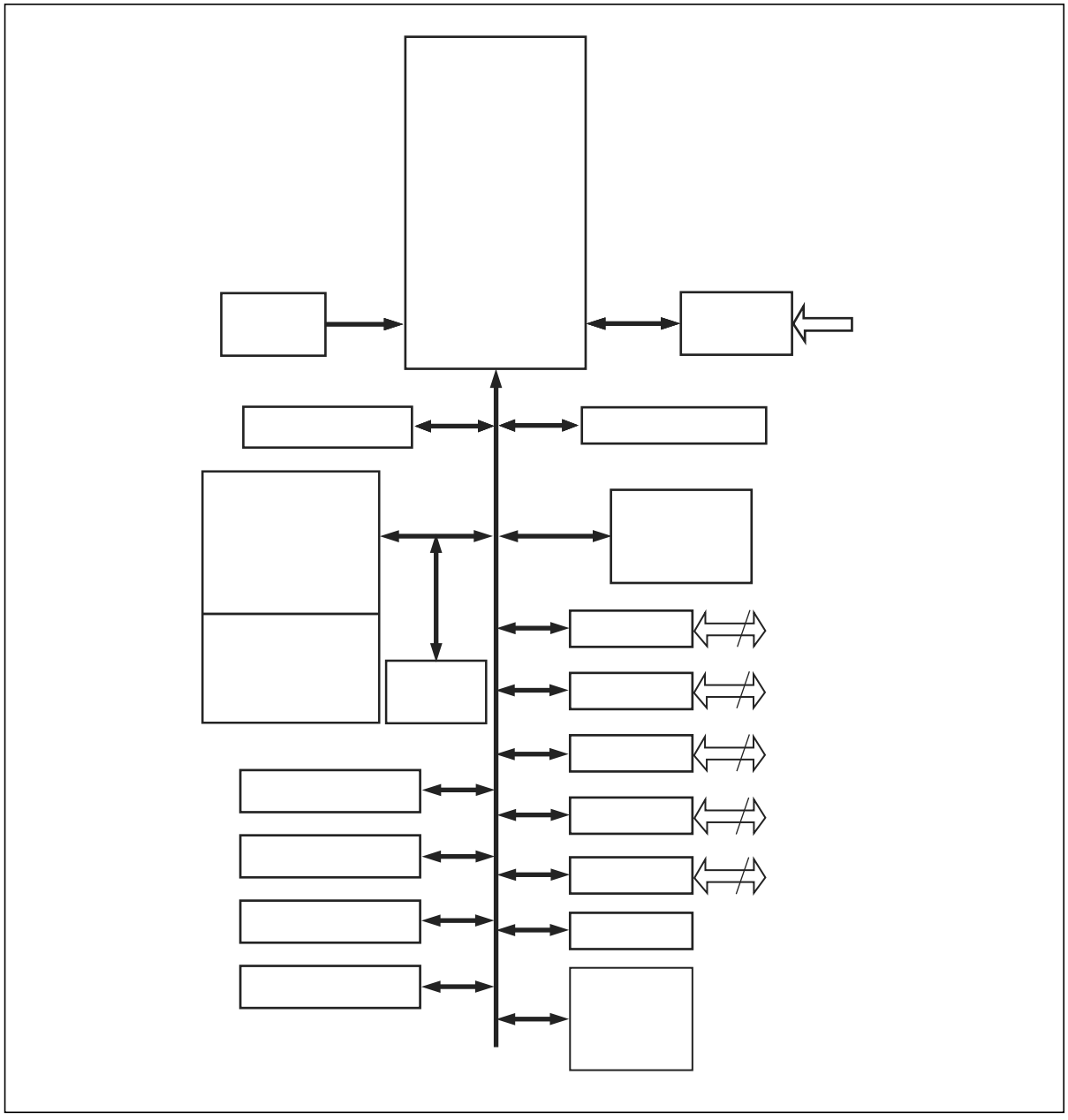

Figure 1: Functional Block Diagram

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Table 1: Pin Descriptions (Continued) (3 of 3)

Symbol	Type[1]	Name and Functions
XTAL1	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	**Crystal 2:** Output from the inverting oscillator amplifier
V_{DD}	I	**Power Supply**
V_{SS}	I	**Ground**

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1. I = Input; O = Output
2. ALE loading issue: When ALE pin experiences higher loading (>30pf) during the reset, the MCU may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3-50 KΩ to V_{DD}, e.g. for ALE pin.
3. For 6 clock mode, ALE is emitted at 1/3 of crystal frequency.
4. Port 4 is not present on the PDIP package.

Memory Organization

The device has separate address spaces for program and data memory.

Program Flash Memory

There are two internal flash memory blocks in the device. The primary flash memory block (Block 0) has 16/32 KByte. The secondary flash memory block (Block 1) has 8 KByte. Since the total program address space is limited to 64 KByte, the SFCF[1:0] bit are used to control program bank selection. Please refer to Figures 5 and 6 for the program memory configuration. Program bank selection is described in the next section.

The 16K/32K x8 primary SuperFlash block is organized as 128/256 sectors, each sector consists of 128 Bytes.

The 8K x8 secondary SuperFlash block is organized as 64 sectors, each sector consists also of 128 Bytes.

For both blocks, the 7 least significant program address bits select the byte within the sector. The remainder of the program address bits select the sector within the block.

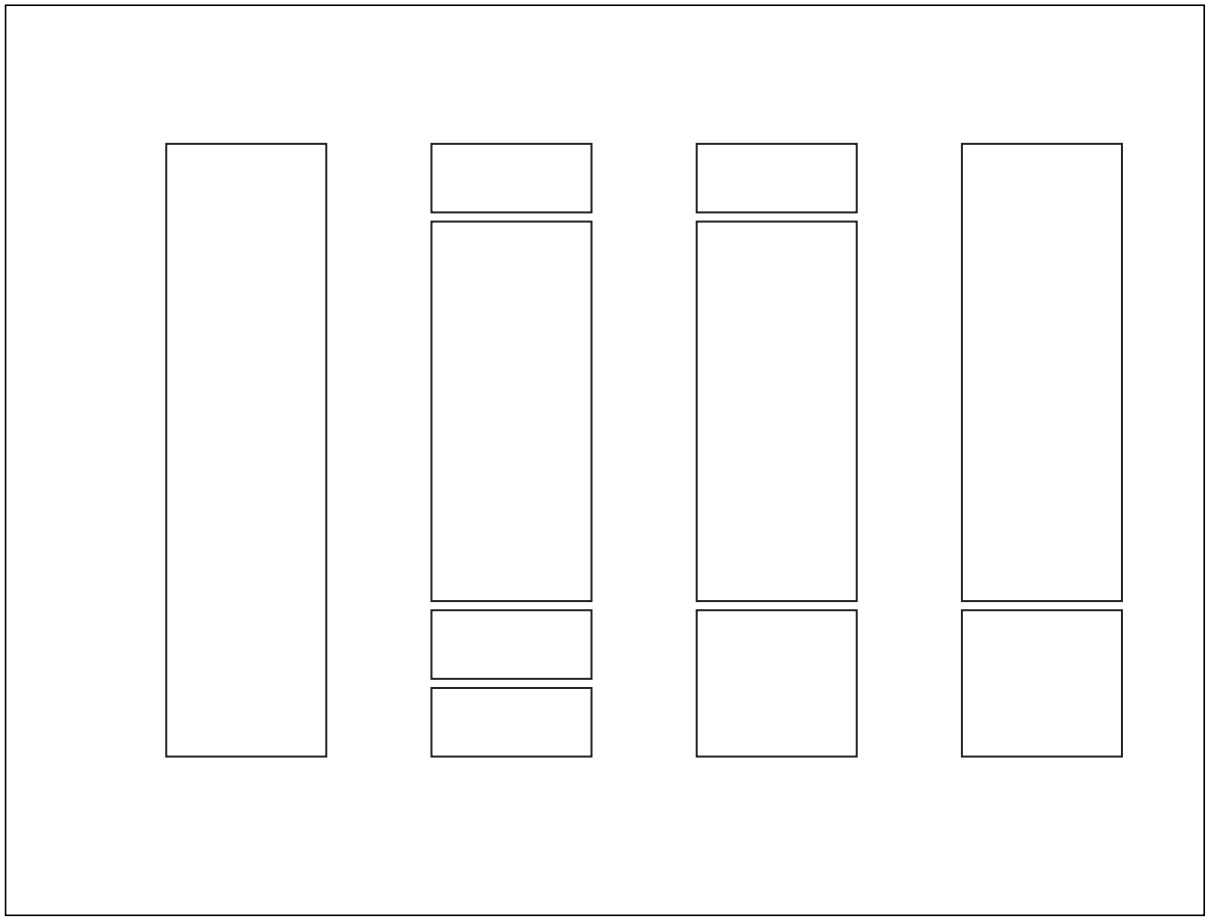

Figure 5: Program Memory Organization for 16 KByte SST89E54RDxA

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Watchdog Timer Data/Reload Register (WDTD)

Location	7	6	5	4	3	2	1	0	Reset Value
85H	Watchdog Timer Data/Reload								00H

Symbol	Function
WDTD	Initial/Reload value in Watchdog Timer. New value won't be effective until WDT is set.

PCA Timer/Counter Control Register[1] (CCON)

Location	7	6	5	4	3	2	1	0	Reset Value
D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000b

1. Bit addressable

Symbol	Function
CF	PCA Counter Overflow Flag Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software, but can only cleared by software.
CR	PCA Counter Run control bit Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

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Timer/Counter 2 Control Register (T2CON)

Location	7	6	5	4	3	2	1	0	Reset Value
C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflow to be used for the transmit clock.
EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2#	Timer or counter select (Timer 2) 0: Internal timer (OSC/6 in 6 clock mode, OSC/12 in 12 clock mode) 1: External event counter (falling edge triggered)
CP/RL2#	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Timer/Counter 2 Mode Control (T2MOD)

Location	7	6	5	4	3	2	1	0	Reset Value
C9H	X	-	-	-	-	-	T2OE	DCEN	xxxxxx00b

Symbol	Function
X	Don't Care
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

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Block-Erase

The Block-Erase command erases all bytes in one of the two memory blocks (Block 0 or Block 1). The selection of the memory block to be erased is determined by the (SFAH[7]) of the SuperFlash Address Register. For SST89E5xRD2A/RDA, if SFAH[7] = 0b, the primary flash memory Block 0 is selected. If SFAH[7:4] = EH, the secondary flash memory Block 1 is selected. The Block-Erase command sequence for SST89E5xRD2A/RDA is as follows:

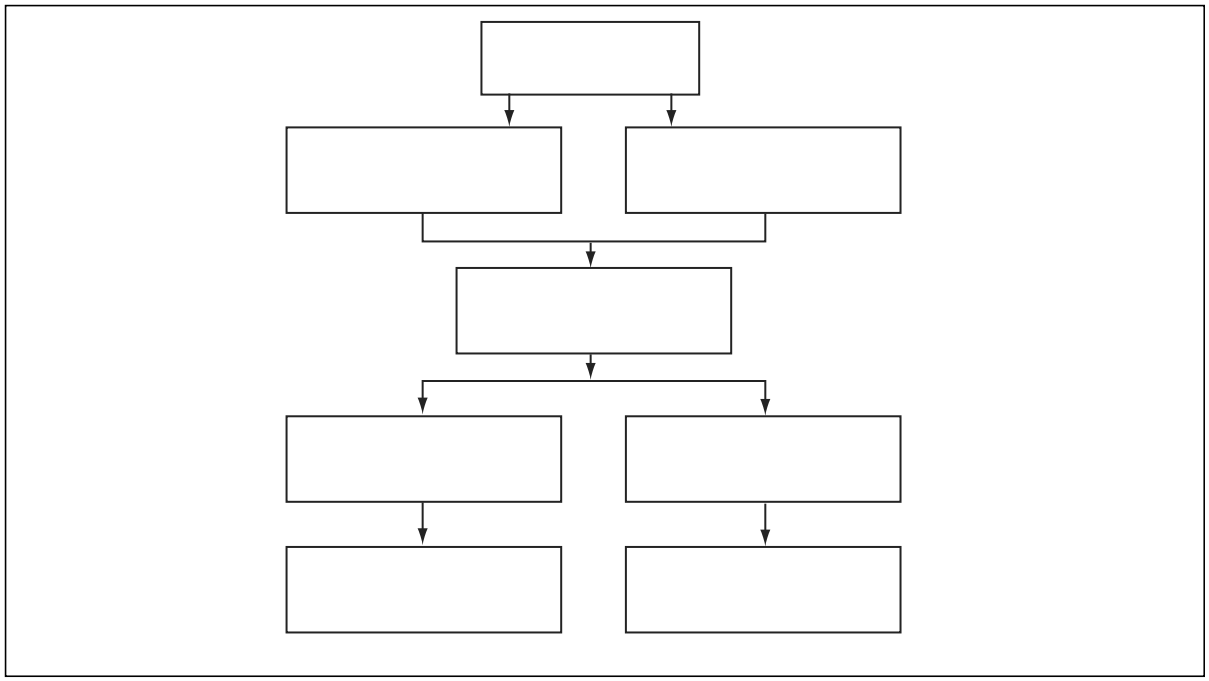

Figure 10: Block-Erase

Prog-SB3, Prog-SB2, Prog-SB1

Prog-SB3, Prog-SB2, Prog-SB1 commands are used to program the security bits (see Table 24). Completion of any of these commands, the security options will be updated immediately.

Security bits previously in un-programmed state can be programmed by these commands. Prog-SB3, Prog-SB2 and Prog-SB1 commands should only reside in Block 1 or external code memory.

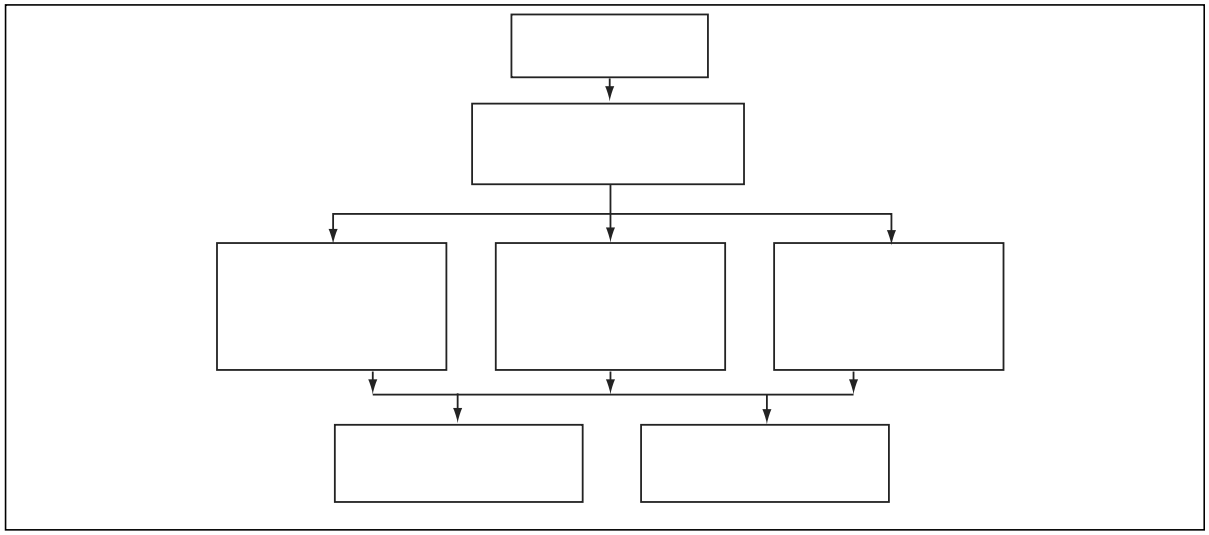

Figure 14: Prog-SB3, Prog-SB2, Prog-SB1

Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 9 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 14: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

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1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 15: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

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1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

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The CCON register is associated with all PCA timer functions. It contains run control bits and flags for the PCA timer (CF) and all modules. To run the PCA the CR bit (CCON.6) must be set by software. Clearing the bit, will turn off PCA. When the PCA counter overflows, the CF (CCON.7) will be set, and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Each module has its own timer interrupt or capture interrupt flag (CCF0 for module 0, CCF4 for module 4, etc.). They are set when either a match or capture occurs. These flags can only be cleared by software. (See "PCA Timer/Counter Control Register (CCON)" on page 26.)

Compare/Capture Modules

Each PCA module has an associated SFR with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. Refer to "PCA Compare/Capture Module Mode Register (CCAPMn)" on page 28 for details. The registers each contain 7 bits which are used to control the mode each module will operate in. The ECCF bit (CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on module) will enable the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set, causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. When there is a match between the PCA counter and the module's capture/compare register, the MATn (CCAPMn.3) and the CCFn bit in the CCON register to be set.

Bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine whether the capture input will be active on a positive edge or negative edge. The CAPN bit enables the negative edge that a capture input will be active on, and the CAPP bit enables the positive edge. When both bits are set, both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set, enables the comparator function. Table 21 shows the CCAPMn settings for the various PCA functions.

There are two additional register associated with each of the PCA modules: CCAPnH and CCAPnL. They are registers that hold the 16-bit count value when a capture occurs or a compare occurs. When a module is used in PWM mode, these registers are used to control the duty cycle of the output. See Figure 24.

Table 20: PCA High and Low Register Compare/Capture Modules

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB	RESET Value
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]	00H
CCAP0L		EAH	CCAP0L[7:0]	00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]	00H
CCAP1L		EBH	CCAP1L[7:0]	00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]	00H
CCAP2L		ECH	CCAP2L[7:0]	00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]	00H
CCAP3L		EDH	CCAP3L[7:0]	00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]	00H
CCAP4L		EEH	CCAP4L[7:0]	00H

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Pulse Width Modulator

The Pulse Width Modulator (PWM) mode is used to generate 8-bit PWMs by comparing the low byte of the PCA timer (CL) with the low byte of the compare register (CCAPnL). When CL < CCAPnL the output is low. When CL ≥ CCAPnL the output is high. To activate this mode, the user must set the PWM and ECOM bits in the module's CCAPMn SFR. (See Figure 28 and Table 23)

In PWM mode, the frequency of the output depends on the source for the PCA timer. Since there is only one set of CH and CL registers, all modules share the PCA timer and frequency. Duty cycle of the output is controlled by the value loaded into the high byte (CCAPnH). Since writes to the CCAPnH register are asynchronous, a new value written to the high byte will not be shifted into CCAPnL for comparison until the next period of the output (when CL rolls over from 255 to 00).

To calculate values for CCAPnH for any duty cycle, use the following equation:

CCAPnH = 256(1 - Duty Cycle)

where CCAPnH is an 8-bit integer and Duty Cycle is a fraction.

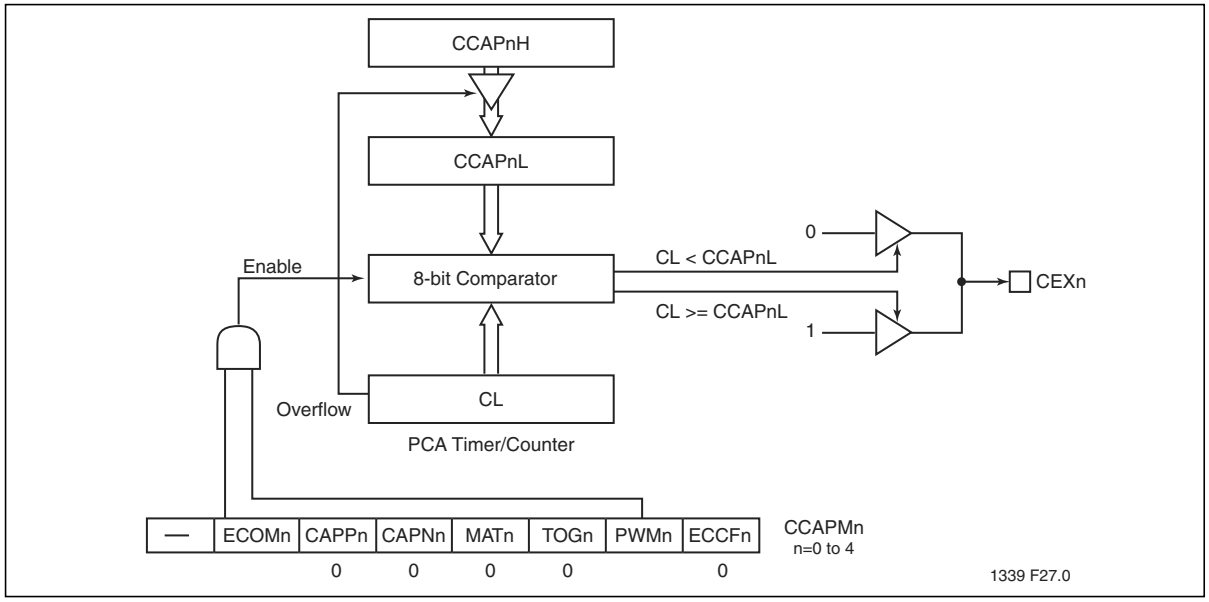

Figure 28: PCA Pulse Width Modulator Mode

Table 23: Pulse Width Modulator Frequencies

	PWM Frequency	
PCA Timer Mode	**12 MHz**	**16 MHz**
1/12 Oscillator Frequency	3.9 KHz	5.2 KHz
1/4 Oscillator Frequency	11.8 KHz	15.6 KHz
Timer 0 Overflow:		
8-bit	15.5 Hz	20.3 Hz
16-bit	0.06 Hz	0.08 Hz
8-bit Auto-Reload	3.9 KHz to 15.3 Hz	5.2 KHz to 20.3 Hz
External Input (Max)	5.9 KHz	7.8 KHz

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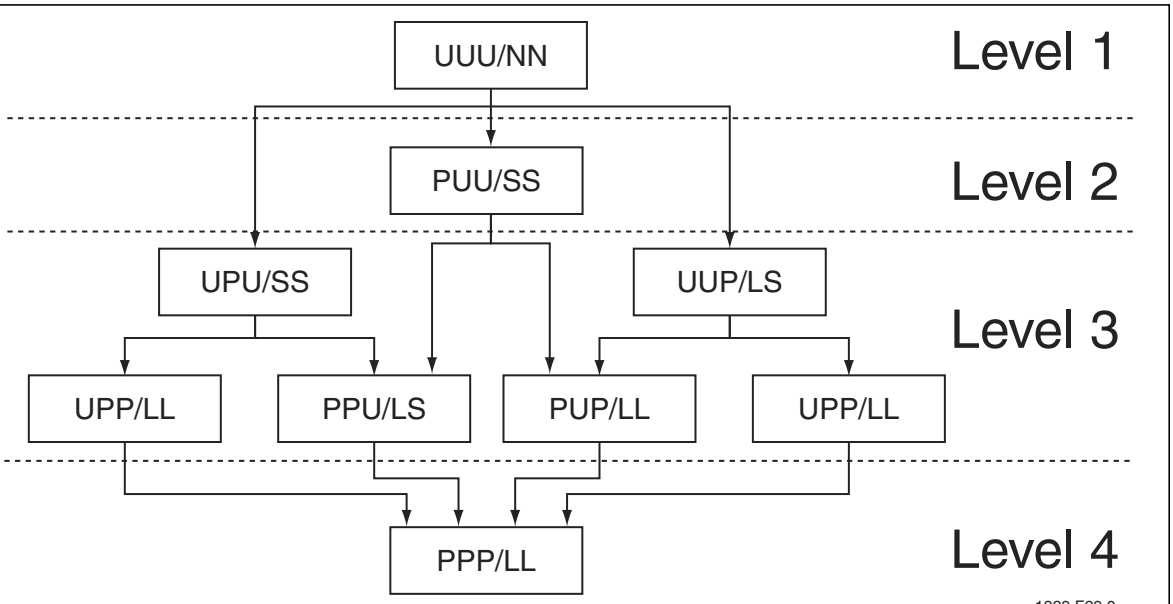
Security Lock Status

The three bits that indicate the device security lock status are located in SFST[7:5]. As shown in Figure 30 and Table 24, the three security lock bits control the lock status of the primary and secondary blocks of memory. There are four distinct levels of security lock status. In the first level, none of the security lock bits are programmed and both blocks are unlocked. In the second level, although both blocks are now locked and cannot be programmed, they are available for read operation via Byte-Verify. In the third level, three different options are available: Block 1 hard lock / Block 0 SoftLock, SoftLock on both blocks, and hard lock on both blocks. Locking both blocks is the same as Level 2, Block 1 except read operation isn't available. The fourth level of security is the most secure level. It doesn't allow read/program of internal memory or boot from external memory. For details on how to program the security lock bits refer to the external host mode and in-application programming sections.



Note: P = Programmed (Bit logic state = 0), U = Unprogrammed (Bit logic state = 1), N = Not Locked, L = Hard locked, S = Soft locked

Figure 30: Security Lock Levels

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Table 24: Security Lock Options

Level	Security Lock Bits[1,2]				Security Status of:		Security Type
	SFST[7:5]	SB1	SB2[1]	SB3[1]	Block 1	Block 0	
1	000	U	U	U	Unlock	Unlock	No Security Features are Enabled.
2	100	P	U	U	SoftLock	SoftLock	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA# is sampled and latched on Reset, and further programming of the flash is disabled.
3	011 101	U P	P U	P P	Hard Lock	Hard Lock	Level 2 plus Verify disabled, both blocks locked.
	010	U	P	U	SoftLock	SoftLock	Level 2 plus Verify disabled. Code in Block 1 may program Block 0 and vice versa.
	110 001	P U	P U	U P	Hard Lock	SoftLock	Level 2 plus Verify disabled. Code in Block 1 may program Block 0.
4	111	P	P	P	Hard Lock	Hard Lock	Same as Level 3 hard lock/hard lock, but MCU will start code execution from the internal memory regardless of EA#.

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1. P = Programmed (Bit logic state = 0), U = Unprogrammed (Bit logic state = 1).
2. SFST[7:5] = Security Lock Status Bits (SB1_i, SB2_i, SB3_i)

Read Operation Under Lock Condition

The status of security bits SB1, SB2, and SB3 can be read when the read command is disabled by security lock. There are three ways to read the status.

1. External host mode: Read-back = 00H (locked)
2. IAP command: Read-back = previous SFDT data
3. MOVC: Read-back = FFH (blank)

Reset

A system reset initializes the MCU and begins program execution at program memory location 0000H. The reset input for the device is the RST pin. In order to reset the device, a logic level high must be applied to the RST pin for at least two machine cycles (24 clocks), after the oscillator becomes stable. ALE, PSEN# are weakly pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform a proper reset. This level must not be affected by external element. A system reset will not affect the 1 KByte of on-chip RAM while the device is running, however, the contents of the on-chip RAM during power up are indeterminate. Following reset, all Special Function Registers (SFR) return to their reset values outlined in Tables 6 to 10.

Power-on Reset

At initial power up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins high. **Powering up the device without a valid reset could cause the MCU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash.**

When power is applied to the device, the RST pin must be held high long enough for the oscillator to start up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2KΩ resistor as shown in Figure 31. Note that if an RC circuit is being used, provisions should be made to ensure the V_{DD} rise time does not exceed 1 millisecond and the oscillator start-up time does not exceed 10 milliseconds.

For a low frequency oscillator with slow start-up time the reset signal must be extended in order to account for the slow start-up time. This method maintains the necessary relationship between V_{DD} and RST to avoid programming at an indeterminate location, which may cause corruption in the code of the flash. The power-on detection is designed to work as power up initially, before the voltage reaches the brown-out detection level. The POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain active until cleared by software. Please see Section , “Power Control Register (PCON)” on page 30 for detailed information.

For more information on system level design techniques, please review the **FlashFlex MCU: Oscillator Circuit Design Considerations** application note.

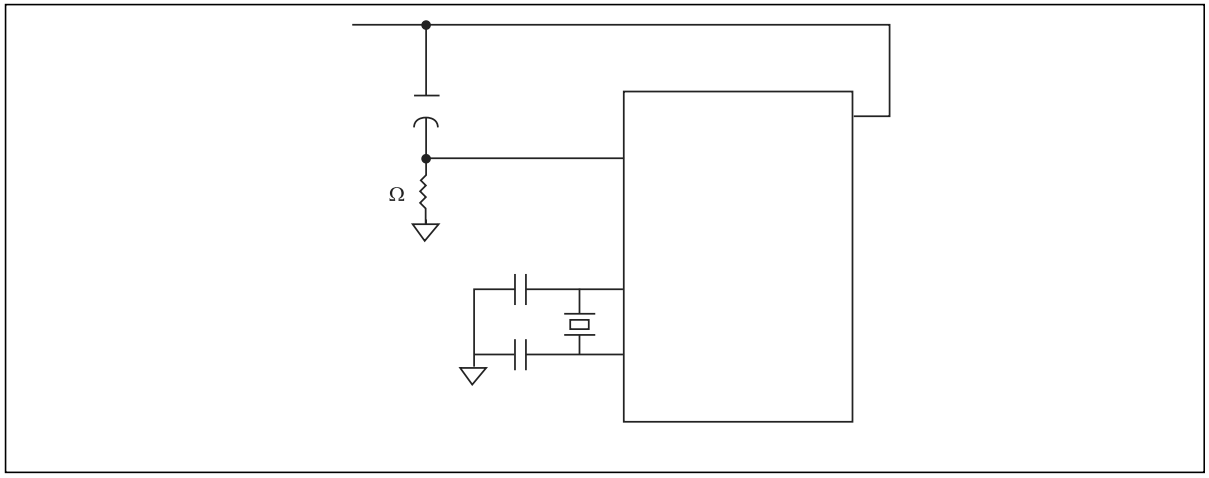

Figure 31: Power-on Reset Circuit

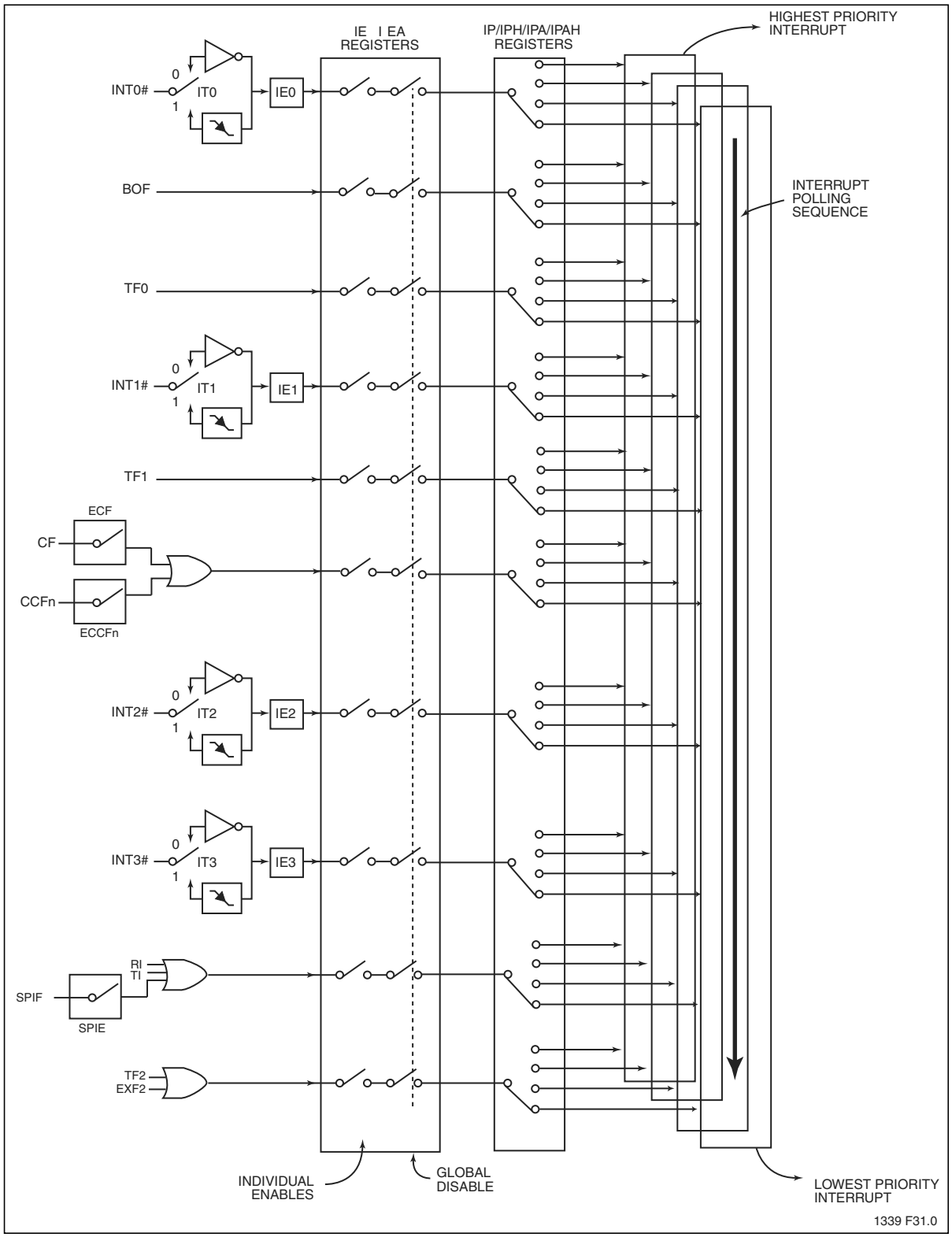

Figure 32: Interrupt Structure

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Table 27: Power Saving Modes

Mode	Initiated by	State of MCU	Exited by
Idle Mode	Software (Set IDL bit in PCON) MOV PCON, #01H;	CLK is running. Interrupts, serial port and timers/counters are active. Program Counter is stopped. ALE and PSEN# signals at a HIGH level during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked idle mode. A user could consider placing two or three NOP instructions after the instruction that invokes idle mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.
Power-down Mode	Software (Set PD bit in PCON) MOV PCON, #02H;	CLK is stopped. On-chip SRAM and SFR data is maintained. ALE and PSEN# signals at a LOW level during power -down. External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked power-down mode. A user could consider placing two or three NOP instructions after the instruction that invokes power-down mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.

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Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 29 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 13 for the IAP mode enabling commands (When set, the EDC# bit in SFST register will indicate 6 clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

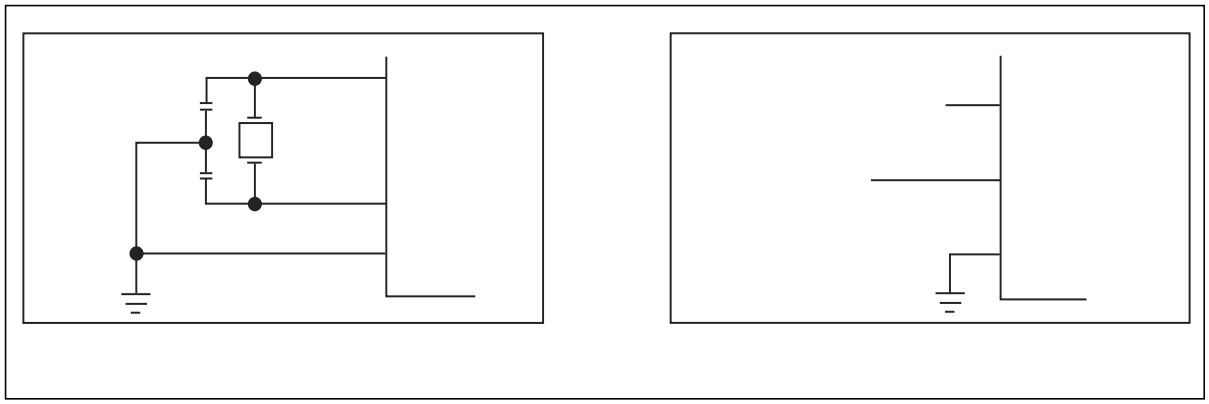

Figure 33: Oscillator Characteristics

Table 29: Clock Doubling Features

Device	Standard Mode (x1)		Clock Double Mode (x2)	
	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)
SST89E5xRD2A/RDA	12	40	6	20

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Table 35: DC Electrical Characteristics for SST89E5xRD2A/RDA
T_A = -40°C to +85°C; V_{DD} = 4.5-5.5V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	4.5 < V_{DD} < 5.5	-0.5	0.2V_{DD} - 0.1	V
V_{IH}	Input High Voltage	4.5 < V_{DD} < 5.5	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	4.5 < V_{DD} < 5.5	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 4.5V			
		I_{OL} = 16mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 4.5V			
		I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 4.5V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 4.5V			
		I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 4.5V			
		I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
V_{BOD}	Brown-out Detection Voltage		3.85	4.15	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}- 0.3		±10	µA
R_{RST}	RST Pull-down Resistor		40	225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current IAP Mode @ 40 MHz			88	mA
	Active Mode @ 40 MHz			50	mA
	Idle Mode @ 40 MHz			42	mA
	Power-down Mode	T_A = 0°C to +70°C		80	µA
		T_A = -40°C to +85°C		90	µA

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AC Electrical Characteristics

AC Characteristics:

(Over Operating Conditions: Load Capacitance for Port 0, ALE#, and PSEN# = 100pF; Load Capacitance for All Other Outputs = 80pF)

Table 36: AC Electrical Characteristics (1 of 2)
T_A = -40°C to +85°C, V_{DD} = 4.5-5.5V@40MHz, V_{SS} = 0V

		Oscillator				
		40 MHz (x1 Mode) 20 MHz (x2 Mode)		Variable		
Symbol	Parameter	Min	Max	Min	Max	Units
$1/T_{CLCL}$	x1 Mode Oscillator Frequency	0	40	0	40	MHz
$1/2T_{CLCL}$	x2 Mode Oscillator Frequency	0	20	0	20	MHz
T_{LHLL}	ALE Pulse Width	35		$2T_{CLCL}$ - 15		ns
T_{AVLL}	Address Valid to ALE Low			T_{CLCL} - 25 (3V)		ns
		10		T_{CLCL} - 15 (5V)		ns
T_{LLAX}	Address Hold After ALE Low			T_{CLCL} - 25 (3V)		ns
		10		T_{CLCL} - 15 (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In				$4T_{CLCL}$ - 65 (3V)	ns
			55		$4T_{CLCL}$ - 45 (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low			T_{CLCL} - 25 (3V)		ns
		10		T_{CLCL} - 15 (5V)		ns
T_{PLPH}	PSEN# Pulse Width	60		$3T_{CLCL}$ - 25 (3V) $3T_{CLCL}$ - 15 (5V)		ns
T_{PLIV}	PSEN# Low to Valid Instr In				$3T_{CLCL}$ - 55 (3V)	ns
			25		$3T_{CLCL}$ - 50 (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#			0		ns
T_{PXIZ}	Input Instr Float After PSEN#				T_{CLCL} - 5 (3V)	ns
			10		T_{CLCL} - 15 (5V)	ns
T_{PXAV}	PSEN# to Address valid	17		T_{CLCL} - 8		ns
T_{AVIV}	Address to Valid Instr In				$5T_{CLCL}$ - 80 (3V)	ns
			65		$5T_{CLCL}$ - 60 (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10	ns
T_{RLRH}	RD# Pulse Width	120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{WLWH}	Write Pulse Width (WE#)	120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{RLDV}	RD# Low to Valid Data In				$5T_{CLCL}$ - 90 (3V)	ns
			75		$5T_{CLCL}$ - 50 (5V)	ns
T_{RHDX}	Data Hold After RD#	0		0		ns
T_{RHDZ}	Data Float After RD#				$2T_{CLCL}$ - 25 (3V)	ns
			38		$2T_{CLCL}$ - 12 (5V)	ns
T_{LLDV}	ALE Low to Valid Data In				$8T_{CLCL}$ - 90 (3V)	ns
			150		$8T_{CLCL}$ - 50 (5V)	ns
T_{AVDV}	Address to Valid Data In				$9T_{CLCL}$ - 90 (3V)	ns
			150		$9T_{CLCL}$ - 75 (5V)	ns

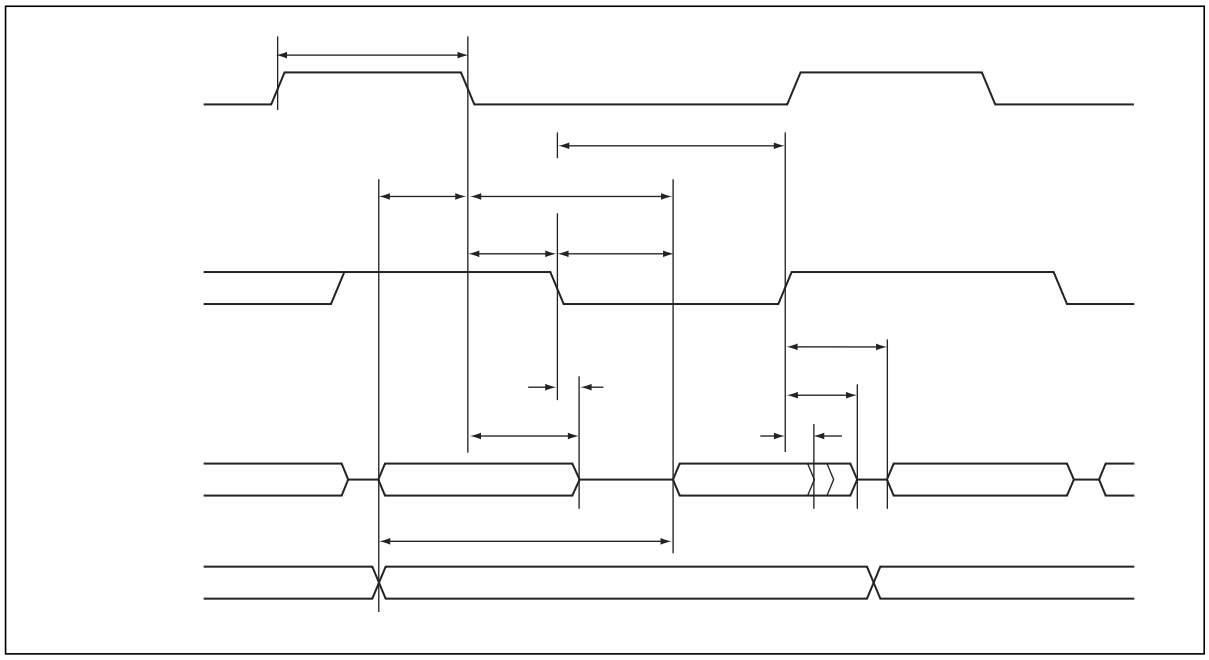

Figure 35: External Program Memory Read Cycle

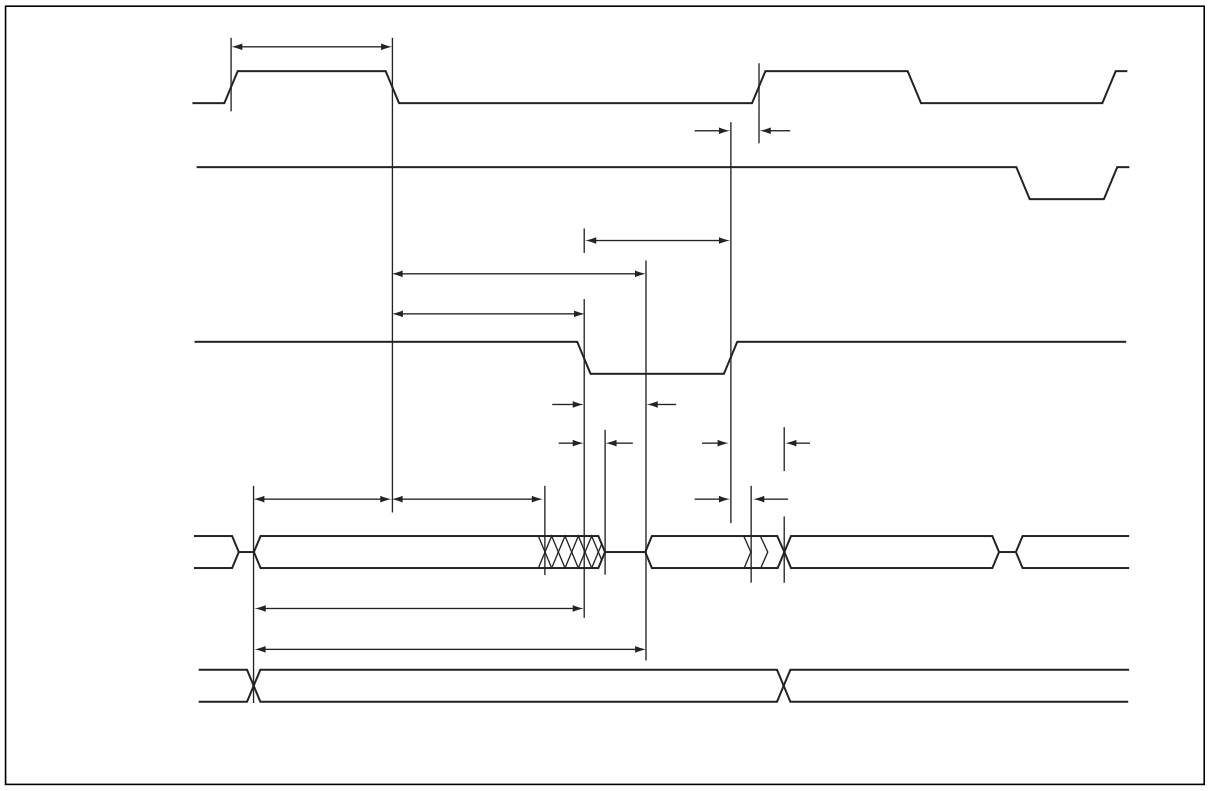

Figure 36: External Data Memory Read Cycle

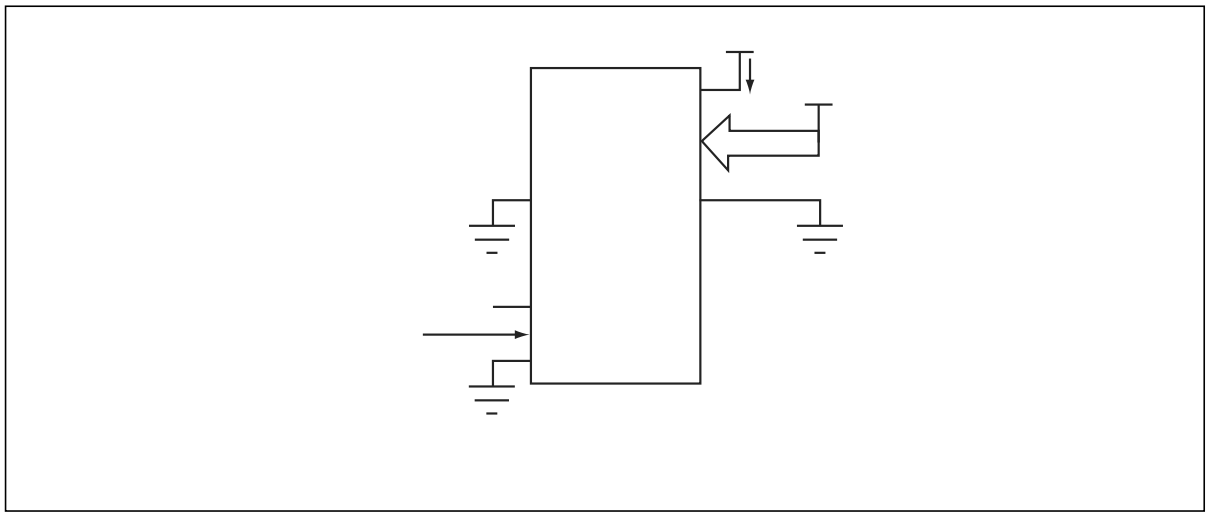

Figure 44: I_{DD} Test Condition, Idle Mode

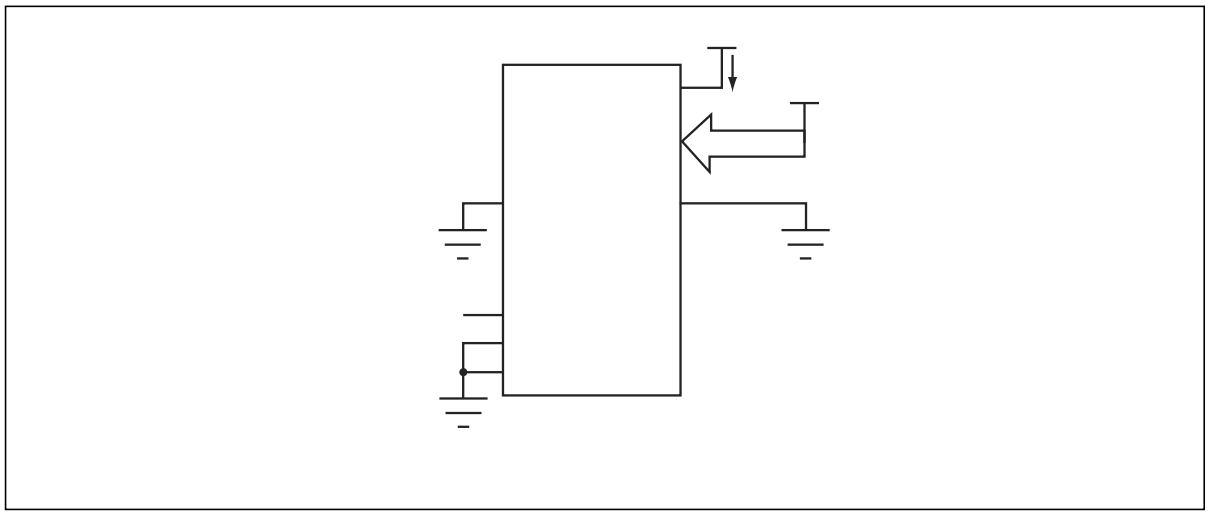

Figure 45: I_{DD} Test Condition, Power-down Mode

Table 38: Flash Memory Programming/Verification Parameters[1]

Parameter[2]	Max	Units
Chip-Erase Time	150	ms
Block-Erase Time	100	ms
Sector-Erase Time	30	ms
Byte-Program Time[3]	50	µs
Re-map or Security bit Program Time	80	µs

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1. For IAP operations, the program execution overhead must be added to the above timing parameters.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. Each byte must be erased before programming.