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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	39
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051c4t6tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3 Functional overview

Figure 1 shows the general block diagram of the STM32F051xx devices.

3.1 ARM[®]-Cortex[®]-M0 core

The ARM[®] Cortex[®]-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F051xx devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
 - 16 to 64 Kbytes of embedded Flash memory for programs and data
 - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.



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3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 **Power management**

3.5.1 **Power supply schemes**

- $V_{DD} = V_{DDIO1} = 2.0$ to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC are used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 13: Power supply scheme*.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.



Functional overview



Figure 2. Clock tree

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

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3.14 Timers and watchdogs

The STM32F051xx devices include up to six general-purpose timers, one basic timer and an advanced control timer.

Table 7 compares the features of the different timers.

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
General purpose	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6	16-bit	Up	integer from 1 to 65536	Yes	-	-

 Table 7. Timer feature comparison

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.



The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I²C)

Up to two I²C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) and Fast mode (up to 400 kbit/s) and, I2C1 also supports Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	 Extra filtering capability vs. standard requirements Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

Table 8. C	Comparison	of I ² C analog	and digital filters
		•••••••••••••••••••••••••••••••••••••••	

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripherals can be served by the DMA controller.

Refer to Table 9 for the differences between I2C1 and I2C2.

Table 9. STM32F051xx I ² C in	nplementation
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I ² C features ⁽¹⁾	I2C1	I2C2
7-bit addressing mode	Х	Х
10-bit addressing mode	Х	Х
Standard mode (up to 100 kbit/s)	Х	Х
Fast mode (up to 400 kbit/s)	Х	Х
Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive I/Os	Х	-
Independent clock	Х	-



3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I²S)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in fullduplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I²S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

SPI features ⁽¹⁾	SPI1	SPI2
Hardware CRC calculation	Х	Х
Rx/Tx FIFO	Х	Х
NSS pulse mode	Х	Х
I ² S mode	х	-
TI mode	Х	Х

Table 44	OTM00F0F4	001/120 :	
Table 11.	SIM32F051XX	SPI/I-S Ir	nplementation

1. X = supported.

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.20 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.



6.3 Operating conditions

6.3.1 General operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit		
f _{HCLK}	Internal AHB clock frequency	-	0	48	M⊔⇒		
f _{PCLK}	Internal APB clock frequency	-	0	48	IVITIZ		
V _{DD}	Standard operating voltage	-	2.0	3.6	V		
N/	Analog operating voltage (ADC and DAC not used) Must		V _{DD}	3.6	M		
VDDA	Analog operating voltage (ADC and DAC used)	to or higher than V _{DD}	2.4	3.6	V		
V _{BAT}	Backup operating voltage	-	1.65	3.6	V		
		TC and RST I/O	-0.3	V _{DDIOx} +0.3			
V _{IN}		TTa I/O	-0.3	V _{DDA} +0.3 ⁽¹⁾	N/		
	1/O input voltage	FT and FTf I/O	-0.3	5.5 ⁽¹⁾	V		
		BOOT0	0	5.5			
	LQFP64		-	444			
		LQFP48	-	364			
	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7 ⁽²⁾	LQFP32	-	357			
P _D		UFQFPN32	-	526	mW		
		UFQFPN48	-	625			
		UFBGA64	-	308			
		WLCSP36	- 333				
	Ambient temperature for the	Maximum power dissipation	-40	85	°C		
т.	suffix 6 version	Low power dissipation ⁽³⁾	-40	105	C		
IA	Ambient temperature for the	Maximum power dissipation	-40	105	°C		
	suffix 7 version	Low power dissipation ⁽³⁾			C		
т	lunction tomporature range	Suffix 6 version	-40	105	°C		
IJ	Sunction temperature range	Suffix 7 version	-40	125	C		

Table 20. General operating conditions

1. For operation with a voltage higher than V_{DDIOx} + 0.3 V, the internal pull-up resistor must be disabled.

2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} . See Section 7.8: Thermal characteristics.

3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see Section 7.8: *Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 21* are derived from tests performed under the ambient temperature condition summarized in *Table 20*.



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			Тур @ V _{BAT}					Max ⁽¹⁾				
Symbol	Parameter	Conditions	1.65 V	1.8 V	2.4 V	2.7 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	Unit
RTC domain	LSE & RTC ON; "Xtal mode": lower driving capability; LSEDRV[1:0] = '00'	0.5	0.5	0.6	0.7	0.8	0.9	1.0	1.3	1.7		
VBAT_VBAT	supply current	LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.8	0.8	0.9	1.0	1.1	1.2	1.3	1.6	2.1	μŢ

Table 28. Typical and maximum current consumption from the $\rm V_{BAT}$ supply

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = V_{DDA} = 3.3 V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to f_{HCLK} frequency:
 - 0 wait state and Prefetch OFF from 0 to 24 MHz
 - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively



Electrical characteristics

Symbol	Parameter	Conditions ⁽¹⁾	I/O toggling frequency (f _{SW})	Тур	Unit	
			4 MHz	0.07		
			8 MHz	0.15		
		$C = C_{INT}$	16 MHz	0.31		
			24 MHz	0.53		
			48 MHz	0.92		
			4 MHz	0.18		
		V _{DDIOx} = 3.3 V	8 MHz	0.37		
		C _{EXT} = 0 pF	16 MHz	0.76		
		$C = C_{INT} + C_{EXT} + C_S$	24 MHz	1.39		
			48 MHz 2.188 4 MHz 0.32 8 MHz 0.64	2.188	- - - mA	
				0.32		
		V _{DDIOx} = 3.3 V		0.64		
		C _{EXT} = 10 pF	16 MHz	1.25		
		$C = C_{INT} + C_{EXT} + C_S$	24 MHz	1.25 2.23 4.442		
low	I/O current		48 MHz	4.442		
.200	consumption		4 MHz	0.49		
		$V_{\text{DDIOx}} = 3.3 \text{ V}$	8 MHz	0.94		
		$C = C_{INT} + C_{FXT} + C_S$	16 MHz	2.38		
		INT - LAT - 5	24 MHz	0.15 0.31 0.53 0.92 0.18 0.37 0.76 1.39 2.188 0.32 0.64 1.25 2.23 4.442 0.49 0.94 2.38 3.99 0.64 1.25 3.24 5.02 0.81 1.7 3.67 0.66 1.43 2.45		
				4 MHz	0.64	
		$V_{\text{DDIOx}} = 3.3 \text{ V}$	8 MHz 1.2	1.25	7	
		$C = C_{INT} + C_{EXT} + C_S$	16 MHz	3.24		
			24 MHz	5.02		
		V _{DDIOx} = 3.3 V	4 MHz	0.81		
		$C_{EXT} = 47 \text{ pF}$	8 MHz	1.7		
		$C = C_{INT} + C_{EXT} + C_{S}$ $C = C_{int}$	16 MHz	3.67	1	
		V _{DDIOX} = 2.4 V	4 MHz	0.66		
		$C_{EXT} = 47 \text{ pF}$	8 MHz	1.43		
		$C = C_{INT} + C_{EXT} + C_{S}$	16 MHz	2.45		
		C = C _{int}	24 MHz	4.97		

Table 30. S	Switching	output I/O	current	consumption
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1. C_S = 7 pF (estimated value).



	Peripheral	Typical consumption at 25 °C	Unit
	APB-Bridge ⁽²⁾	3	
	SYSCFG	3	
	ADC ⁽³⁾	5	
	TIM1	17	
	SPI1	10	
	USART1	19	
	TIM15	11	
	TIM16	8	
	TIM17	8	
	DBG (MCU Debug Support)	0.5	
	TIM2	17	
APB	TIM3	13	µA/MHz
	TIM6	3	
	TIM14	6	
	WWDG	1	
	SPI2	7	
	USART2	7	
	I2C1	4	
	I2C2	5	
	DAC	2	
	PWR	1	
	CEC	2	
	All APB peripherals	149	

 Table 31. Peripheral current consumption (continued)

1. The BusMatrix automatically is active when at least one master is ON (CPU or DMA1)

2. The APBx Bridge is automatically active when at least one peripheral is ON on the same Bus.

3. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC is not included. Refer to the tables of characteristics in the subsequent sections.



Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.



Figure 18. Typical application with a 32.768 kHz crystal

Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. The provided curves are characterization results, not tested in production.



Low-speed internal (LSI) RC oscillator

Table 39. LS	l oscillator	characteristics ⁽¹⁾
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Symbol	Parameter	Min	Тур	Max	Unit
f _{LSI}	Frequency	30	40	50	kHz
t _{su(LSI)} ⁽²⁾	LSI oscillator startup time	-	-	85	μs
I _{DDA(LSI)} ⁽²⁾	LSI oscillator power consumption	-	0.75	1.2	μÂ

1. V_{DDA} = 3.3 V, T_A = –40 to 105 $^\circ\text{C}$ unless otherwise specified.

2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Symbol	Doromotor		Unit		
Symbol	Faiameter	Min	Тур	Max	Unit
f	PLL input clock ⁽¹⁾	1 ⁽²⁾	8.0	24 ⁽²⁾	MHz
^I PLL_IN	PLL input clock duty cycle	40 ⁽²⁾	-	60 ⁽²⁾	%
f _{PLL_OUT}	PLL multiplier output clock	16 ⁽²⁾	-	48	MHz
t _{LOCK}	PLL lock time	-	-	200 ⁽²⁾	μs
Jitter _{PLL}	Cycle-to-cycle jitter	-	_	300 ⁽²⁾	ps

Table 40. PLL characteristics

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.

2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

Table 41. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
t _{prog}	16-bit programming time	T _A = - 40 to +105 °C	40	53.5	60	μs
t _{ERASE}	Page (1 KB) erase time	T _A = - 40 to +105 °C	20	-	40	ms
t _{ME}	Mass erase time	T _A = - 40 to +105 °C	20	-	40	ms
I _{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.





Figure 24. Recommended NRST pin protection

1. The external capacitor protects the device against parasitic resets.

 The user must ensure that the level on the NRST pin can go below the V_{IL(NRST)} max level specified in Table 51: NRST pin characteristics. Otherwise the reset will not be taken into account by the device.

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the conditions summarized in *Table 20: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
I _{DDA (ADC)}	Current consumption of the $ADC^{(1)}$	V _{DDA} = 3.3 V	-	0.9 -		mA
f _{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f _S ⁽²⁾	Sampling rate	12-bit resolution	0.043	-	1	MHz
f _{TRIG} ⁽²⁾	External trigger frequency	f _{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	1/f _{ADC}
V _{AIN}	Conversion voltage range	-	0	-	V _{DDA}	V
R _{AIN} ⁽²⁾	External input impedance	See <i>Equation 1</i> and <i>Table 53</i> for details	-	-	50	kΩ
R _{ADC} ⁽²⁾	Sampling switch resistance	-	-	-	1	kΩ
C _{ADC} ⁽²⁾	Internal sample and hold capacitor	-	-	-	8	pF
+ (2)(3)	Calibration time	f _{ADC} = 14 MHz	5.9			μs
'CAL		-	83			1/f _{ADC}

Table 52. ADC characteristics



Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
		ADC clock = HSI14	1.5 ADC cycles + 2 - f _{PCLK} cycles		1.5 ADC cycles + 3 f _{PCLK} cycles	-
W _{LATENCY} ⁽²⁾⁽⁴⁾	ADC_DR register ready latency	ADC clock = PCLK/2	-	4.5	-	f _{PCLK} cycle
		ADC clock = PCLK/4	- 8.5		-	f _{PCLK} cycle
t _{latr} (2)		$f_{ADC} = f_{PCLK}/2 = 14 \text{ MHz}$		μs		
	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$	5.5			1/f _{PCLK}
		$f_{ADC} = f_{PCLK}/4 = 12 \text{ MHz}$		μs		
		$f_{ADC} = f_{PCLK}/4$		1/f _{PCLK}		
		f _{ADC} = f _{HSI14} = 14 MHz	0.179	-	0.250	μs
Jitter _{ADC}	ADC jitter on trigger conversion	f _{ADC} = f _{HSI14}	-	1	-	1/f _{HSI14}
+ (2)	Sampling time	f _{ADC} = 14 MHz	0.107	-	17.1	μs
LS'-7		-	1.5	-	239.5	1/f _{ADC}
t _{STAB} ⁽²⁾	Stabilization time	-		14		1/f _{ADC}
+ (2)	Total conversion time	f _{ADC} = 14 MHz, 12-bit resolution	1	-	18	μs
^L CONV` ′	(including sampling time)	12-bit resolution	14 to 252 (t _S for sampling +12.5 for successive approximation)		1/f _{ADC}	

 Table 52. ADC characteristics (continued)

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 μ A on I_{DD} and 60 μ A on I_{DD} should be taken into account.

2. Guaranteed by design, not tested in production.

3. Specified value includes only ADC timing. It does not include the latency of the register access.

4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_{S}}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

T _s (cycles)	t _S (μs)	R _{AIN} max (kΩ) ⁽¹⁾
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4

Table 53. R_{AIN} max for f_{ADC} = 14 MHz



6.3.17 DAC electrical specifications

Symbol	Parameter	Min	Тур	Max	Unit	Comments
V _{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	V	-
D (1)	Resistive load with buffer	5	-	-	kΩ	Load connected to V _{SSA}
►LOAD` ′	ON	25	-	-	kΩ	Load connected to V _{DDA}
R ₀ ⁽¹⁾	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
C _{LOAD} ⁽¹⁾	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xE1C) at
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer ON	-	-	V _{DDA} – 0.2	V	$V_{DDA} = 3.6 V \text{ and } (0x155) \text{ and}$ (0xEAB) at $V_{DDA} = 2.4 V$
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer OFF	-	-	V _{DDA} – 1LSB	V	excursion of the DAC.
lpp (¹)	DAC DC current consumption in quiescent mode ⁽²⁾	-	-	600	μA	With no load, middle code (0x800) on the input
'DDA		-	-	700	μA	With no load, worst code (0xF1C) on the input
DNL ⁽³⁾	Differential non linearity Difference between two	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
	consecutive code-1LSB)	-	-	±2	LSB	Given for the DAC in 12-bit configuration
	Integral non linearity (difference between	-	-	±1	LSB	Given for the DAC in 10-bit configuration
INL ⁽³⁾	measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±4	LSB	Given for the DAC in 12-bit configuration
	Offset error	-	-	±10	mV	-
Offset ⁽³⁾	(difference between measured value at Code	-	-	±3	LSB	Given for the DAC in 10-bit at V _{DDA} = 3.6 V
	(0x800) and the ideal value = V _{DDA} /2)	-	-	±12	LSB	Given for the DAC in 12-bit at $V_{DDA} = 3.6 V$

Table	55.	DAC	charact	teristics
Table	55.	DAO	charac	



Symbol	Parameter	Conditio	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit	
V _{hys}		No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
			High speed mode	3		13	
	Comparator hysteresis	(COMPxHYST[1:0]=01)	All other power modes	5	8	10	
		Madium hustorasia	High speed mode	7		26	
		(COMPxHYST[1:0]=10)	All other power modes	9	15	19	
		High hystoresis	High speed mode	18		49	
		(COMPxHYST[1:0]=11)	All other power modes	19	31	40	

Table 56. Comparator characteristics (continued)

1. Data based on characterization results, not tested in production.

2. For more details and conditions see Figure 28: Maximum V_{REFINT} scaler startup time from power down.



Figure 28. Maximum V_{REFINT} scaler startup time from power down



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.

7.1 UFBGA64 package information

UFBGA64 is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra-fine-profile ball grid array package.



Figure 34. UFBGA64 package outline

1. Drawing is not to scale.

Symbol	millimeters			inches ⁽¹⁾				
	Min	Тур	Max	Min	Тур	Max		
А	0.460	0.530	0.600	0.0181	0.0209	0.0236		
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043		
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197		
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071		
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146		



Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.



Figure 48. WLCSP36 package marking example

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



Using the values obtained in *Table* 74 T_{Jmax} is calculated as follows:

- For LQFP64, 45 °C/W
- $T_{Jmax} = 100 \text{ °C} + (45 \text{ °C/W} \times 134 \text{ mW}) = 100 \text{ °C} + 6.03 \text{ °C} = 106.03 \text{ °C}$

This is above the range of the suffix 6 version parts ($-40 < T_J < 105 \text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 55* to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements.







8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 75. Ordering information scheme										
Example:	STM32	F	051	R	8	Т	6	х		
Device family										
STM32 = ARM-based 32-bit microcontroll	er									
Product type										
F = General-purpose										
Sub-family										
051 = STM32F051xx										
Pin count										
K = 32 pins										
T = 36 pins										
C = 48 pins										
R = 64 pins										
User code memory size										
4 = 16 Kbyte										
6 = 32 Kbyte										
8 = 64 Kbyte										
Package										
H = UFBGA										
T = LQFP										
U = UFQFPN										
Y = WLCSP										
Temperature range										
6 = -40 °C to +85 °C										
7 = -40 °C to +105 °C										
Options										
xxx = code ID of programmed parts (inclu	des nackin	n tvne)							

xxx = code ID of programmed parts (includes packing type) TR = tape and reel packing blank = tray packing

