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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051c6t7

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2 Description

The STM32F051xx microcontrollers incorporate the high-performance ARM[®] Cortex[®]-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 64 Kbytes of Flash memory and 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I²Cs, up to two SPIs, one I²S, one HDMI CEC and up to two USARTs), one 12-bit ADC, one 12-bit DAC, six 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F051xx microcontrollers operate in the -40 to +85 $^{\circ}$ C and -40 to +105 $^{\circ}$ C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F051xx microcontrollers include devices in seven different packages ranging from 32 pins to 64 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F051xx microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.



Perip	STM32F051Kx STM32F051T8 STM32F051Cx				1Cx	STM32F051Rx					
Flash mem	16	32	64	64	16	32	64	16	32	64	
SRAM		8									
	Advanced control		1 (16-bit)								
Timers	General purpose		5 (16-bit) 1 (32-bit)								
	Basic		1 (16-bit)								
	SPI [l ² S] ⁽¹⁾		1 [1] ⁽²⁾		1 [1] ⁽²⁾	1 [1	I] ⁽²⁾	2 [1]		2 [1]	
Comm.	l ² C		1 ⁽³⁾		1 ⁽³⁾	1((3)	2	1((3)	2
interfaces	USART	1 ⁽⁴⁾	2		2	1 ⁽⁴⁾	2	2	1 ⁽⁴⁾	2	2
	CEC		1								
12-bit (number o		1 1 (10 ext. + 3 int.) (16 ext. + 3 int.)							int.)		
12-bit (number o	t DAC f channels)	1 (1)									
Analog co	omparator	2									
GP	llOs	25 (0 27 (or	on LQF 1 UFQF	P32) PN32)	29	39			55		
Capacitive ser	nsing channels	13 (0 14 (or	on LQF 1 UFQF	P32) PN32)	14	17			18		
Max. CPU	frequency	48 MHz									
Operatin	2.0 to 3.6 V										
Operating temperature			Amt	pient op Junctio	erating temperatu n temperature: -4	re: -40° 0°C to 1	C to 85 05°C /	°C / -40 -40°C to	°C to 10 0 125°C)5°C	
Packages		U	LQFP32 FQFPN	2 32	WLCSP36	l UI	LQFP48 FQFPN	3 48	U	∟QFP64 JFBGA6	↓ 64

Table 2. STM32F051xx family device features and peripheral count

1. The SPI1 interface can be used either in SPI mode or in I^2S audio mode.

2. SPI2 is not present.

3. I2C2 is not present.

4. USART2 is not present.





Figure 1. Block diagram



3 Functional overview

Figure 1 shows the general block diagram of the STM32F051xx devices.

3.1 ARM[®]-Cortex[®]-M0 core

The ARM[®] Cortex[®]-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F051xx devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
 - 16 to 64 Kbytes of embedded Flash memory for programs and data
 - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.



In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F051xx microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1,, COMPx or the CEC.

The CEC, USART1 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

• Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.



	P	Pin nu	umbe	er						Pin fu	nctions
LQFP64	UFBGA64	LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
58	D3	42	C4	29	29	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_IO3	-
59	C3	43	A4	30	30	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4	-
60	B4	44	B4	31	31	BOOT0	Ι	В	-	Boot memo	ry selection
61	В3	45	-	-	32	PB8	I/O	FTf	(4)(5)	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC	-
62	A3	46	-	-	-	PB9	I/O	FTf	(5)	I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-
63	D5	47	D6	32	0	VSS	S	-	-	Gro	und
64	E5	48	A5	1	1	VDD	S	-	-	Digital pov	ver supply

Table 13. Pin definitions (continued)

 PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
 The speed should not exceed 2 MHz with a maximum load of 30 pF.

The speed should not exceed 2 MHZ with a maximum load of 30 pF.
 These GPIOs must not be used as current sources (e.g. to drive an LED).

After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content
of the RTC registers which are not reset by the main reset. For details on how to manage these GPIOs, refer to the RTC
domain and RTC register descriptions in the reference manual.

3. Distinct VSSA pin is only available on packages with 48 and more pins. For all other packages, the pin number corresponds to the VSS pin to which VSSA pad of the silicon die is connected.

4. On the LQFP32 package, PB2 and PB8 must be set to defined levels by software, as their corresponding pads on the silicon die are left unconnected. Apply the same recommendations as for unconnected pins.

5. On the WLCSP36 package, PB8, PB9, PB10, PB11, PB12, PB13, PB14 and PB15 must be set to defined levels by software, as their corresponding pads on the silicon die are left unconnected. Apply the same recommendations as for unconnected pins.

6. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.



Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
ANDZ	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
AHB1	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
APB	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 16. STM32F051xx peripheral register boundary addresses



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25$ °C and $T_A = T_A max$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25$ °C, $V_{DD} = V_{DDA} = 3.3$ V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.







Figure 17. Typical application with an 8 MHz crystal

1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 36*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Тур	Max ⁽²⁾	Unit	
		low drive capability	-	0.5	0.9		
	ISE current consumption	medium-low drive capability	-	-	1		
IDD		medium-high drive capability	-	-	1.3	μΑ	
		high drive capability	-	-	1.6		
		low drive capability	5	-	-		
~	Oscillator transconductance	medium-low drive capability	8	-	-		
9 _m		medium-high drive capability	15	-	-	μΑνν	
		high drive capability	25	-	-		
$t_{\rm SU(LSE)}^{(3)}$	Startup time	V _{DDIOx} is stabilized	-	2	-	s	

Table 36. LSE oscillato	r characteristics	(f _{LSE} = 32.768 kHz)
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1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

2. Guaranteed by design, not tested in production.

 t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer



High-speed internal (HSI) RC oscillator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit			
f _{HSI}	Frequency	-	-	8	-	MHz			
TRIM	HSI user trimming step	-	-	-	1 ⁽²⁾	%			
DuCy _(HSI)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%			
		T _A = -40 to 105°C	-2.8 ⁽³⁾	-	3.8 ⁽³⁾				
		T _A = -10 to 85°C	-1.9 ⁽³⁾	-	2.3 ⁽³⁾				
	Accuracy of the HSI	$T_A = 0$ to $85^{\circ}C$	-1.9 ⁽³⁾	-	2 ⁽³⁾	0/			
ACCHSI	oscillator	$T_A = 0$ to $70^{\circ}C$	-1.3 ⁽³⁾	-	2 ⁽³⁾	70			
		$T_A = 0$ to 55°C	-1 ⁽³⁾	-	2 ⁽³⁾				
		$T_A = 25^{\circ}C^{(4)}$	-1	-	1				
t _{su(HSI)}	HSI oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs			
I _{DDA(HSI)}	HSI oscillator power consumption	-	-	80	100 ⁽²⁾	μA			

Table 37. HSI oscillator characteristics⁽¹⁾

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.

2. Guaranteed by design, not tested in production.

3. Data based on characterization results, not tested in production.

4. Factory calibrated, parts not soldered.



Figure 19. HSI oscillator accuracy characterization results for soldered parts



Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
N _{END}	Endurance	T _A = -40 to +105 °C	10	kcycle
t _{RET}		1 kcycle ⁽²⁾ at T _A = 85 °C	30	
	Data retention	1 kcycle ⁽²⁾ at T _A = 105 °C	10	Year
		10 kcycle ⁽²⁾ at T _A = 55 °C	20	

 Table 42. Flash memory endurance and data retention

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 43*. They are based on the EMS levels and classes defined in application note AN1709.

Symbol	Parameter	Conditions	Level/ Class
V _{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T _A = +25 °C, f _{HCLK} = 48 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f _{HCLK} = 48 MHz, conforming to IEC 61000-4-4	4B

Table 43. EMS characteristics

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section 6.2:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 17: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 17: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OL}	Output low level voltage for an I/O pin	CMOS port ⁽²⁾	-	0.4	
V _{OH}	Output high level voltage for an I/O pin	I _{IO} = 8 mA V _{DDIOx} ≥ 2.7 V	V _{DDIOx} –0.4	-	V
V _{OL}	Output low level voltage for an I/O pin	TTL port ⁽²⁾	-	0.4	
V _{OH}	Output high level voltage for an I/O pin	I _{IO} = 8 mA V _{DDIOx} ≥ 2.7 V	2.4	-	V
V _{OL} ⁽³⁾	Output low level voltage for an I/O pin	I _{IO} = 20 mA	-	1.3	V
V _{OH} ⁽³⁾	Output high level voltage for an I/O pin	V _{DDIOx} ≥2.7 V	V _{DDIOx} -1.3	-	v
V _{OL} ⁽³⁾	Output low level voltage for an I/O pin	11.1=6 mA	-	0.4	V
V _{OH} ⁽³⁾	Output high level voltage for an I/O pin	1101 – 0 MA	V _{DDIOx} -0.4	-	v
V _{OLFm+} ⁽³⁾	Output low level voltage for an FTf I/O pin in	I _{IO} = 20 mA V _{DDIOx} ≥ 2.7 V	-	0.4	V
OEI III.		I _{IO} = 10 mA	-	0.4	V

Table 49. Output voltage characteristics⁽¹⁾

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 17: Voltage characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO} .

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

3. Data based on characterization results. Not tested in production.



6.3.17 DAC electrical specifications

Symbol	Parameter	Min	Тур	Max	Unit	Comments
V _{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	V	-
D (1)	Resistive load with buffer	5	-	-	kΩ	Load connected to V _{SSA}
►LOAD` ′	ON	25	-	-	kΩ	Load connected to V _{DDA}
R ₀ ⁽¹⁾	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
C _{LOAD} ⁽¹⁾	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xE1C) at
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer ON	-	-	V _{DDA} – 0.2	V	$V_{DDA} = 3.6 V \text{ and } (0x155) \text{ and}$ (0xEAB) at $V_{DDA} = 2.4 V$
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer OFF	-	-	V _{DDA} – 1LSB	V	excursion of the DAC.
lpo (¹)	DAC DC current	-	-	600	μA	With no load, middle code (0x800) on the input
'DDA	mode ⁽²⁾	-	-	700	μA	With no load, worst code (0xF1C) on the input
DNL ⁽³⁾	Differential non linearity Difference between two	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
	consecutive code-1LSB)	-	-	±2	LSB	Given for the DAC in 12-bit configuration
	Integral non linearity (difference between	-	-	±1	LSB	Given for the DAC in 10-bit configuration
INL ⁽³⁾	and the value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±4	LSB	Given for the DAC in 12-bit configuration
	Offset error	-	-	±10	mV	-
Offset ⁽³⁾	(difference between measured value at Code	-	-	±3	LSB	Given for the DAC in 10-bit at V _{DDA} = 3.6 V
	(0x800) and the ideal value = V _{DDA} /2)	-	-	±12	LSB	Given for the DAC in 12-bit at $V_{DDA} = 3.6 V$

Table	55.	DAC	charact	teristics
Table	55.	DAO	charac	



Symbol	Parameter	Min	Тур	Мах	Unit	Comments
Gain error ⁽³⁾	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
t _{SETTLING} ⁽³⁾	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	μs	C _{LOAD} ≤ 50 pF, R _{LOAD} ≥ 5 kΩ
Update rate ⁽³⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	C _{LOAD} ≤ 50 pF, R _{LOAD} ≥ 5 kΩ
t _{WAKEUP} ⁽³⁾	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	μs	$C_{LOAD} \le 50 \text{ pF}, R_{LOAD} \ge 5 \text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR+ ⁽¹⁾	Power supply rejection ratio (to V _{DDA}) (static DC measurement	-	-67	-40	dB	No R _{LOAD} , C _{LOAD} = 50 pF

Table 55. DAC characteristics (continued)

1. Guaranteed by design, not tested in production.

2. The DAC is in "quiescent mode" when it keeps the value steady on the output so no dynamic consumption is involved.

3. Data based on characterization results, not tested in production.



Figure 27. 12-bit buffered / non-buffered DAC

The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register. 1.



Symbol	Parameter	Conditio	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit	
V _{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	mV
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

Table 56. Comparator characteristics (continued)

1. Data based on characterization results, not tested in production.

2. For more details and conditions see Figure 28: Maximum V_{REFINT} scaler startup time from power down.



Figure 28. Maximum V_{REFINT} scaler startup time from power down





Figure 29. SPI timing diagram - slave mode and CPHA = 0





1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}



Symbol	Parameter	Conditions	Min	Мах	Unit
t _{su(SD_MR)}	Data input actus timo	Master receiver	6	-	
t _{su(SD_SR)}	Data input setup time	Slave receiver	2	-	
t _{h(SD_MR)} ⁽²⁾	Data input hold time	Master receiver	4	-	
t _{h(SD_SR)} ⁽²⁾		Slave receiver	0.5	-	
t _{v(SD_MT)} ⁽²⁾	Data output valid time	Master transmitter	-	4	115
t _{v(SD_ST)} ⁽²⁾		Slave transmitter	-	20	l
t _{h(SD_MT)}	Data output hold time	Master transmitter	0	-	
t _{h(SD_ST)}		Slave transmitter	13	-	

Table 64. I²S characteristics⁽¹⁾ (continued)

1. Data based on design simulation and/or characterization results, not tested in production.

2. Depends on f_{PCLK} . For example, if f_{PCLK} = 8 MHz, then T_{PCLK} = 1/ f_{PLCLK} = 125 ns.



Figure 32. I²S slave timing diagram (Philips protocol)

1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx}

2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.



Figure 45. UFQFPN48 package marking example

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.



Figure 54. UFQFPN32 package marking example

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



Date	Revision	Changes	
		Modified datasheet title. Added packages UFQFPN48 and UFBGA64. Replaced "backup domain with "RTC domain" throughout the document. Changed SRAM value from "4 to 8 Kbyte" to "8 Kbyte"	
		Replaced IWWDG with IWDG in <i>Figure: Block diagram.</i> Added inputs LSI and LSE to the multiplexer in <i>Figure: Clock</i> <i>tree</i>	
		Added feature "Reference clock detection" in Section: Real-time clock (RTC) and backup registers.	
		Modified junction temperature in <i>Table: Thermal characteristics.</i> Renamed <i>Table: Internal voltage reference calibration values.</i>	
		Replaced V_{DD} with V_{DDA} and V_{RERINT} with ΔV_{REFINT} in <i>Table: Embedded internal reference voltage.</i>	
		Rephrased introduction of Section: Touch sensing controller (TSC).	
13-Jan-2014	4	Rephrased Section: Voltage regulator. Added sentence "If this is used when the voltage regulator is put in low power mode" under "Stop mode" in Section: Low-power modes.	
		Removed sentence "The internal voltage reference is also connected to ADC_IN17 input channel of the ADC." in <i>Section: Comparators (COMP).</i>	
		Removed feature "Periodic wakeup from Stop/Standby" in Section: Real-time clock (RTC) and backup registers.	
		Replaced I _{DD} with I _{DDA} in <i>Table: HSI</i> oscillator characteristics, <i>Table: HSI14</i> oscillator characteristics and <i>Table: LSI</i> oscillator characteristics.	
		Moved section "Wakeup time from low-power mode" to <i>Section 6.3.6</i> and rephrased the section.	
		Added lines D2 and E2 in <i>Table: UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package mechanical data.</i>	
		Added "The peripheral clock used is 48 MHz." in Section On- chip peripheral current consumption.	

Table 76. Document revision history (continued)

