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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 39 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 13x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051c8t7 |

# Contents

# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F051xx microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

**Table 2. STM32F051xx family device features and peripheral count**

| Peripheral | | STM32F051Kx | | | STM32F051T8 | STM32F051Cx | | | STM32F051Rx | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Flash memory (Kbyte) | | 16 | 32 | 64 | 64 | 16 | 32 | 64 | 16 | 32 | 64 |
| SRAM (Kbyte) | | 8 | | | | | | | | | |
| Timers | Advanced control | 1 (16-bit) | | | | | | | | | |
| | General purpose | 5 (16-bit)<br>1 (32-bit) | | | | | | | | | |
| | Basic | 1 (16-bit) | | | | | | | | | |
| Comm. interfaces | SPI [$I^2S$](1) | 1 [1](2) | | | 1 [1](2) | 1 [1](2) | | 2 [1] | 2 [1] | | |
| | $I^2C$ | 1(3) | | | 1(3) | 1(3) | | 2 | 1(3) | | 2 |
| | USART | 1(4) | 2 | | 2 | 1(4) | 2 | | 1(4) | 2 | |
| | CEC | 1 | | | | | | | | | |
| 12-bit ADC<br>(number of channels) | | 1<br>(10 ext. + 3 int.) | | | | | | | 1<br>(16 ext. + 3 int.) | | |
| 12-bit DAC<br>(number of channels) | | 1<br>(1) | | | | | | | | | |
| Analog comparator | | 2 | | | | | | | | | |
| GPIOs | | 25 (on LQFP32)<br>27 (on UFQFPN32) | | | 29 | 39 | | | 55 | | |
| Capacitive sensing channels | | 13 (on LQFP32)<br>14 (on UFQFPN32) | | | 14 | 17 | | | 18 | | |
| Max. CPU frequency | | 48 MHz | | | | | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | | | | | |
| Operating temperature | | Ambient operating temperature: -40°C to 85°C / -40°C to 105°C<br>Junction temperature: -40°C to 105°C / -40°C to 125°C | | | | | | | | | |
| Packages | | LQFP32<br>UFQFPN32 | | | WLCSP36 | LQFP48<br>UFQFPN48 | | | LQFP64<br>UFBGA64 | | |

1. The SPI1 interface can be used either in SPI mode or in $I^2S$ audio mode.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART2 is not present.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

## 3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14), DAC and ADC.

## 3.9 Interrupts and events

### 3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 55 GPIOs can be connected to the 16 external interrupt lines.

## 3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 3 internal (temperature

## 3.14 Timers and watchdogs

The STM32F051xx devices include up to six general-purpose timers, one basic timer and an advanced control timer.

*Table 7* compares the features of the different timers.

**Table 7. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | 3 |
| General purpose | TIM2 | 32-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM3 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM14 | 16-bit | Up | integer from 1 to 65536 | No | 1 | - |
| | TIM15 | 16-bit | Up | integer from 1 to 65536 | Yes | 2 | 1 |
| | TIM16 TIM17 | 16-bit | Up | integer from 1 to 65536 | Yes | 1 | 1 |
| Basic | TIM6 | 16-bit | Up | integer from 1 to 65536 | Yes | - | - |

### 3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

**Figure 8. LQFP32 package pinout**

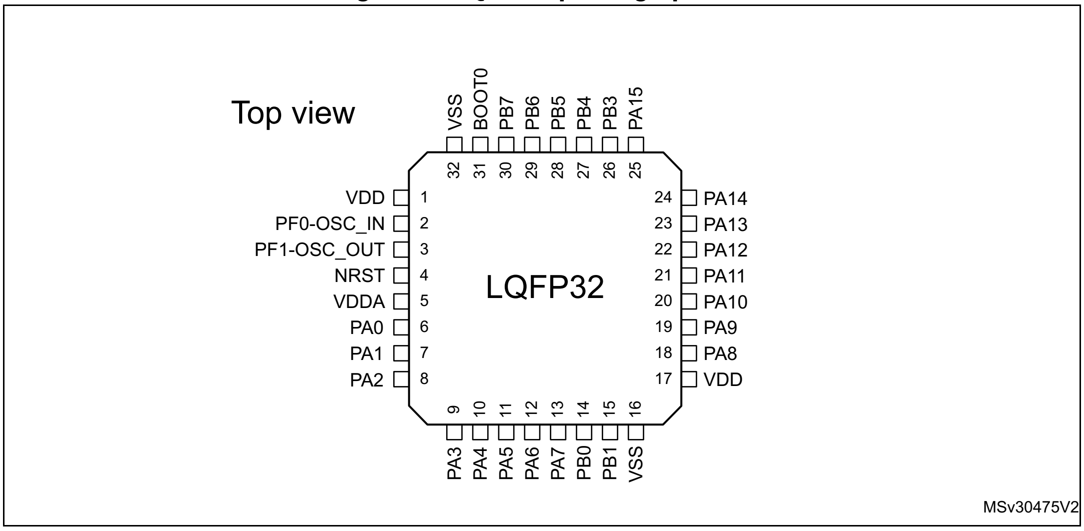



**Figure 9. UFQFPN32 package pinout**

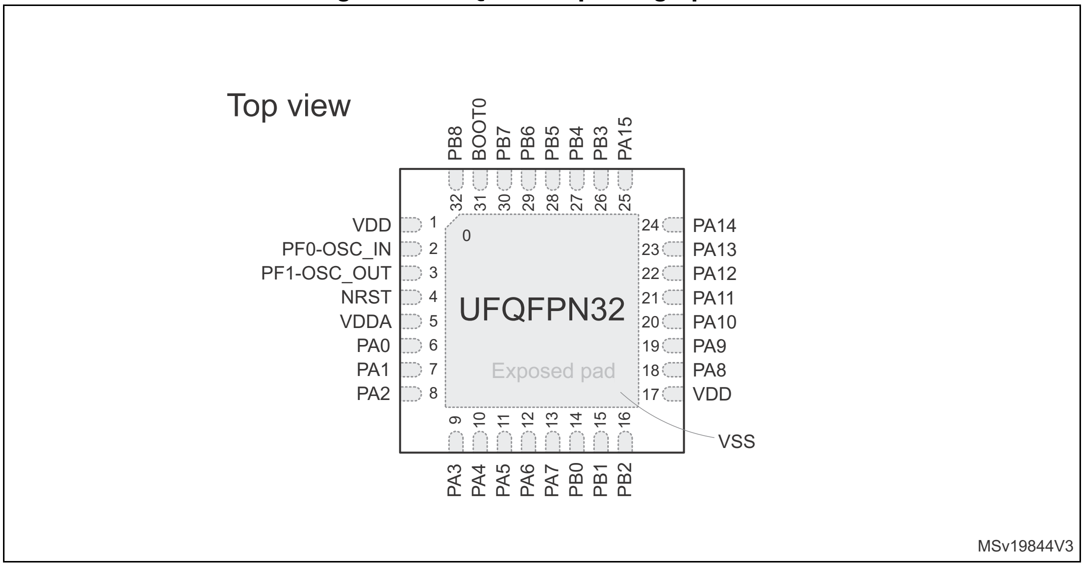


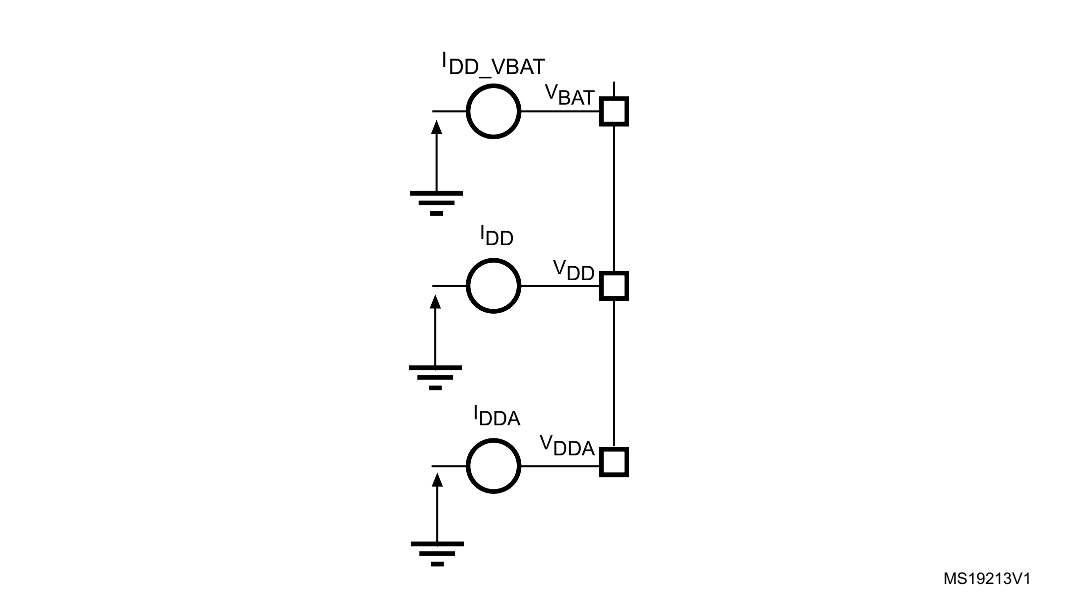
**Table 13. Pin definitions (continued)**

| Pin number | | | | | | Pin name (function upon reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | UFBGA64 | LQFP48/UFQFPN48 | WLCSP36 | LQFP32 | UFQFPN32 | | | | | Alternate functions | Additional functions |
| 58 | D3 | 42 | C4 | 29 | 29 | PB6 | I/O | FTf | - | I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_IO3 | - |
| 59 | C3 | 43 | A4 | 30 | 30 | PB7 | I/O | FTf | - | I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4 | - |
| 60 | B4 | 44 | B4 | 31 | 31 | BOOT0 | I | B | - | Boot memory selection | |
| 61 | B3 | 45 | - | - | 32 | PB8 | I/O | FTf | (4)(5) | I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC | - |
| 62 | A3 | 46 | - | - | - | PB9 | I/O | FTf | (5) | I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT | - |
| 63 | D5 | 47 | D6 | 32 | 0 | VSS | S | - | - | Ground | |
| 64 | E5 | 48 | A5 | 1 | 1 | VDD | S | - | - | Digital power supply | |

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the main reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. Distinct VSSA pin is only available on packages with 48 and more pins. For all other packages, the pin number corresponds to the VSS pin to which VSSA pad of the silicon die is connected.
4. On the LQFP32 package, PB2 and PB8 must be set to defined levels by software, as their corresponding pads on the silicon die are left unconnected. Apply the same recommendations as for unconnected pins.
5. On the WLCSP36 package, PB8, PB9, PB10, PB11, PB12, PB13, PB14 and PB15 must be set to defined levels by software, as their corresponding pads on the silicon die are left unconnected. Apply the same recommendations as for unconnected pins.
6. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

### 6.1.7 Current consumption measurement

**Figure 14. Current consumption measurement scheme**



## 6.3 Operating conditions

### 6.3.1 General operating conditions

**Table 20. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 48 | MHz |
| $f_{PCLK}$ | Internal APB clock frequency | - | 0 | 48 | |
| $V_{DD}$ | Standard operating voltage | - | 2.0 | 3.6 | V |
| $V_{DDA}$ | Analog operating voltage (ADC and DAC not used) | Must have a potential equal to or higher than $V_{DD}$ | $V_{DD}$ | 3.6 | V |
| | Analog operating voltage (ADC and DAC used) | | 2.4 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | - | 1.65 | 3.6 | V |
| $V_{IN}$ | I/O input voltage | TC and RST I/O | –0.3 | $V_{DDIOx}$+0.3 | V |
| | | TTa I/O | –0.3 | $V_{DDA}$+0.3(1) | |
| | | FT and FTf I/O | –0.3 | 5.5(1) | |
| | | BOOT0 | 0 | 5.5 | |
| $P_D$ | Power dissipation at $T_A$ = 85 °C for suffix 6 or $T_A$ = 105 °C for suffix 7(2) | LQFP64 | - | 444 | mW |
| | | LQFP48 | - | 364 | |
| | | LQFP32 | - | 357 | |
| | | UFQFPN32 | - | 526 | |
| | | UFQFPN48 | - | 625 | |
| | | UFBGA64 | - | 308 | |
| | | WLCSP36 | - | 333 | |
| $T_A$ | Ambient temperature for the suffix 6 version | Maximum power dissipation | –40 | 85 | °C |
| | | Low power dissipation(3) | –40 | 105 | |
| | Ambient temperature for the suffix 7 version | Maximum power dissipation | –40 | 105 | °C |
| | | Low power dissipation(3) | –40 | 125 | |
| $T_J$ | Junction temperature range | Suffix 6 version | –40 | 105 | °C |
| | | Suffix 7 version | –40 | 125 | |

1. For operation with a voltage higher than $V_{DDIOx}$ + 0.3 V, the internal pull-up resistor must be disabled.
2. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$. See *Section 7.8: Thermal characteristics*.
3. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$ (see *Section 7.8: Thermal characteristics*).

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 21* are derived from tests performed under the ambient temperature condition summarized in *Table 20*.

**Table 23. Programmable voltage detector characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD6}$ | PVD threshold 6 | Rising edge | 2.66 | 2.78 | 2.9 | V |
| | | Falling edge | 2.56 | 2.68 | 2.8 | V |
| $V_{PVD7}$ | PVD threshold 7 | Rising edge | 2.76 | 2.88 | 3 | V |
| | | Falling edge | 2.66 | 2.78 | 2.9 | V |
| $V_{PVDhyst}$(1) | PVD hysteresis | - | - | 100 | - | mV |
| $I_{DD(PVD)}$ | PVD current consumption | - | - | 0.15 | 0.26(1) | µA |

1. Guaranteed by design, not tested in production.

### 6.3.4 Embedded reference voltage

The parameters given in *Table 24* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

**Table 24. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +105 °C | 1.2 | 1.23 | 1.25 | V |
| $t_{START}$ | ADC_IN17 buffer startup time | - | - | - | 10(1) | µs |
| $t_{S\_vrefint}$ | ADC sampling time when reading the internal reference voltage | - | 4(1) | - | - | µs |
| $\Delta V_{REFINT}$ | Internal reference voltage spread over the temperature range | $V_{DDA}$ = 3 V | - | - | 10(1) | mV |
| $T_{Coeff}$ | Temperature coefficient | - | - 100(1) | - | 100(1) | ppm/°C |

1. Guaranteed by design, not tested in production.

### 6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

**Table 25. Typical and maximum current consumption from $V_{DD}$ at 3.6 V (continued)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | All peripherals enabled | | | | All peripherals disabled | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ $T_A$ (1) | | | Typ | Max @ $T_A$ (1) | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | HSE bypass, PLL on | 48 MHz | 14.0 | 15.3(2) | 15.3 | 16.0(2) | 2.8 | 3.0(2) | 3.0 | 3.2(2) | mA |
| | | | 32 MHz | 9.5 | 10.2 | 10.2 | 10.7 | 2.0 | 2.1 | 2.1 | 2.3 | |
| | | | 24 MHz | 7.3 | 7.8 | 7.8 | 8.3 | 1.5 | 1.7 | 1.7 | 1.9 | |
| | | HSE bypass, PLL off | 8 MHz | 2.6 | 2.9 | 2.9 | 3.0 | 0.6 | 0.8 | 0.8 | 0.8 | |
| | | | 1 MHz | 0.4 | 0.6 | 0.6 | 0.6 | 0.2 | 0.4 | 0.4 | 0.4 | |
| | | HSI clock, PLL on | 48 MHz | 14.0 | 15.3 | 15.3 | 16.0 | 3.8 | 4.0 | 4.1 | 4.2 | |
| | | | 32 MHz | 9.5 | 10.2 | 10.2 | 10.7 | 2.6 | 2.7 | 2.8 | 2.8 | |
| | | | 24 MHz | 7.3 | 7.8 | 7.8 | 8.3 | 2.0 | 2.1 | 2.1 | 2.1 | |
| | | HSI clock, PLL off | 8 MHz | 2.6 | 2.9 | 2.9 | 3.0 | 0.6 | 0.8 | 0.8 | 0.8 | |

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of $I_{DD}$ and $I_{DDA}$).

**Table 26. Typical and maximum current consumption from the $V_{DDA}$ supply**

| Symbol | Parameter | Conditions (1) | $f_{HCLK}$ | $V_{DDA}$ = 2.4 V | | | | $V_{DDA}$ = 3.6 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ $T_A$ (2) | | | Typ | Max @ $T_A$ (2) | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| $I_{DDA}$ | Supply current in Run or Sleep mode, code executing from Flash memory or RAM | HSE bypass, PLL on | 48 MHz | 150 | 170(3) | 178 | 182(3) | 164 | 183(3) | 195 | 198(3) | µA |
| | | | 32 MHz | 104 | 121 | 126 | 128 | 113 | 129 | 135 | 138 | |
| | | | 24 MHz | 82 | 96 | 100 | 103 | 88 | 102 | 106 | 108 | |
| | | HSE bypass, PLL off | 8 MHz | 2.0 | 2.7 | 3.1 | 3.3 | 3.5 | 3.8 | 4.1 | 4.4 | |
| | | | 1 MHz | 2.0 | 2.7 | 3.1 | 3.3 | 3.5 | 3.8 | 4.1 | 4.4 | |
| | | HSI clock, PLL on | 48 MHz | 220 | 240 | 248 | 252 | 244 | 263 | 275 | 278 | |
| | | | 32 MHz | 174 | 191 | 196 | 198 | 193 | 209 | 215 | 218 | |
| | | | 24 MHz | 152 | 167 | 173 | 174 | 168 | 183 | 190 | 192 | |
| | | HSI clock, PLL off | 8 MHz | 72 | 79 | 82 | 83 | 83.5 | 91 | 94 | 95 | |

1. Current consumption from the $V_{DDA}$ supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, $I_{DDA}$ is independent of clock frequencies.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of $I_{DD}$ and $I_{DDA}$).

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 31*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 17: Voltage characteristics*

**Table 31. Peripheral current consumption**

| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| AHB | BusMatrix[1] | 5 | µA/MHz |
| | DMA1 | 7 | |
| | SRAM | 1 | |
| | Flash memory interface | 14 | |
| | CRC | 2 | |
| | GPIOA | 9 | |
| | GPIOB | 12 | |
| | GPIOC | 2 | |
| | GPIOD | 1 | |
| | GPIOF | 1 | |
| | TSC | 6 | |
| | **All AHB peripherals** | **55** | |

## High-speed internal (HSI) RC oscillator

Table 37. HSI oscillator characteristics(1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 8 | - | MHz |
| TRIM | HSI user trimming step | - | - | - | 1(2) | % |
| $DuCy_{(HSI)}$ | Duty cycle | - | 45(2) | - | 55(2) | % |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator | $T_A$ = -40 to 105°C | -2.8(3) | - | 3.8(3) | % |
| | | $T_A$ = -10 to 85°C | -1.9(3) | - | 2.3(3) | |
| | | $T_A$ = 0 to 85°C | -1.9(3) | - | 2(3) | |
| | | $T_A$ = 0 to 70°C | -1.3(3) | - | 2(3) | |
| | | $T_A$ = 0 to 55°C | -1(3) | - | 2(3) | |
| | | $T_A$ = 25°C(4) | -1 | - | 1 | |
| $t_{su(HSI)}$ | HSI oscillator startup time | - | 1(2) | - | 2(2) | µs |
| $I_{DDA(HSI)}$ | HSI oscillator power consumption | - | - | 80 | 100(2) | µA |

1. $V_{DDA}$ = 3.3 V, $T_A$ = -40 to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 19. HSI oscillator accuracy characterization results for soldered parts

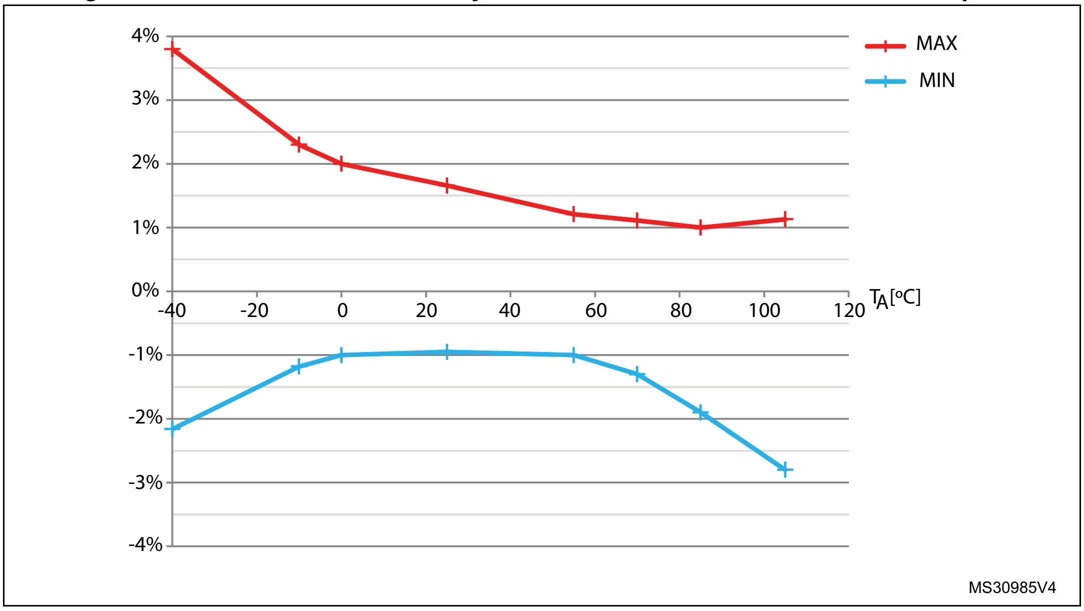


**Table 45. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Packages | Class | Maximum value[1] | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to JESD22-A114 | All | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to ANSI/ESD STM5.3.1 | All | C3 | 250 | V |

1. Data based on characterization results, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 46. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DDIOx}$ (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 47*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 23* and *Table 50*, respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

**Table 50. I/O AC characteristics(1)(2)**

| OSPEEDRy [1:0] value(1) | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| x0 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF | - | 2 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 125 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 125 | |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF | - | 10 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 25 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 25 | |
| 11 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 30 pF, $V_{DDIOx} \geq 2.7$ V | - | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DDIOx} \geq 2.7$ V | - | 30 | |
| | | | $C_L$ = 50 pF, $V_{DDIOx} < 2.7$ V | - | 20 | |
| | $t_{f(IO)out}$ | Output fall time | $C_L$ = 30 pF, $V_{DDIOx} \geq 2.7$ V | - | 5 | ns |
| | | | $C_L$ = 50 pF, $V_{DDIOx} \geq 2.7$ V | - | 8 | |
| | | | $C_L$ = 50 pF, $V_{DDIOx} < 2.7$ V | - | 12 | |
| | $t_{r(IO)out}$ | Output rise time | $C_L$ = 30 pF, $V_{DDIOx} \geq 2.7$ V | - | 5 | |
| | | | $C_L$ = 50 pF, $V_{DDIOx} \geq 2.7$ V | - | 8 | |
| | | | $C_L$ = 50 pF, $V_{DDIOx} < 2.7$ V | - | 12 | |
| Fm+ configuration(4) | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF | - | 2 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 12 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 34 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 10 | - | ns |

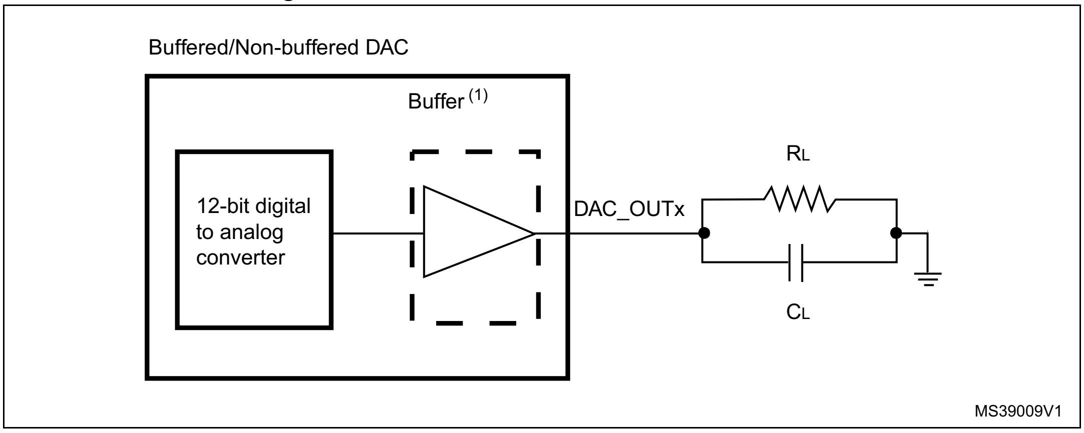
1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 23*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

**Table 55. DAC characteristics (continued)**

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Gain error(3) | Gain error | - | - | ±0.5 | % | Given for the DAC in 12-bit configuration |
| $t_{SETTLING}$(3) | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | - | 3 | 4 | µs | $C_{LOAD}$ ≤ 50 pF, $R_{LOAD}$ ≥ 5 kΩ |
| Update rate(3) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | 1 | MS/s | $C_{LOAD}$ ≤ 50 pF, $R_{LOAD}$ ≥ 5 kΩ |
| $t_{WAKEUP}$(3) | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | 6.5 | 10 | µs | $C_{LOAD}$ ≤ 50 pF, $R_{LOAD}$ ≥ 5 kΩ input code between lowest and highest possible ones. |
| PSRR+ (1) | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement | - | –67 | –40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF |

1. Guaranteed by design, not tested in production.
2. The DAC is in “quiescent mode” when it keeps the value steady on the output so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

**Figure 27. 12-bit buffered / non-buffered DAC**




1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

**Figure 29. SPI timing diagram - slave mode and CPHA = 0**

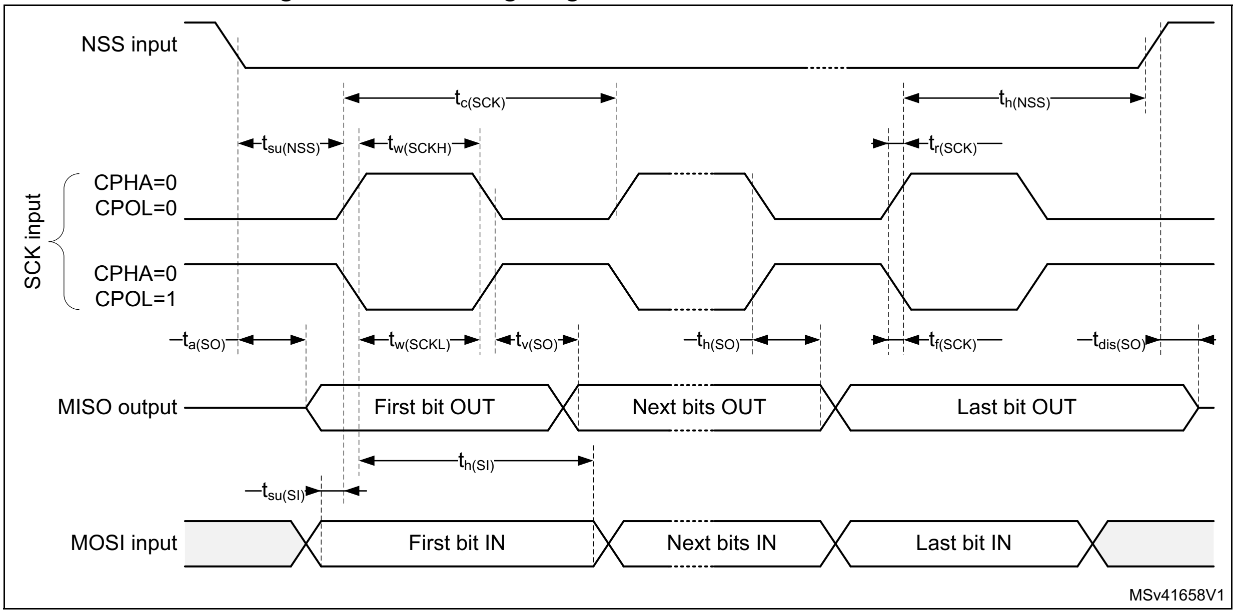
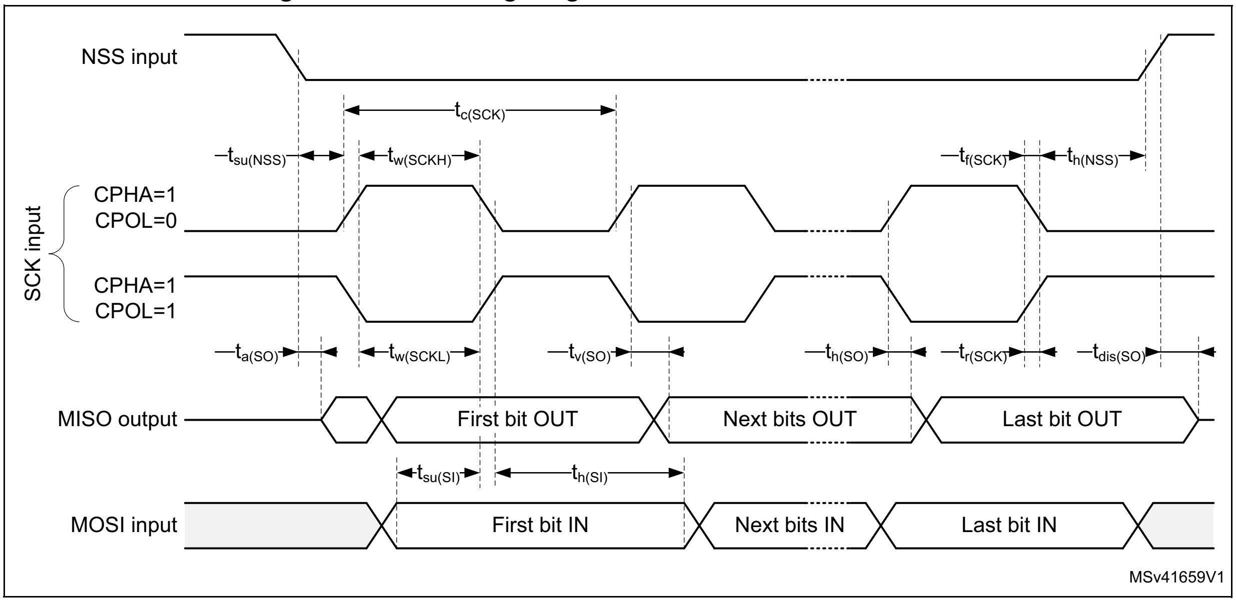



**Figure 30. SPI timing diagram - slave mode and CPHA = 1**



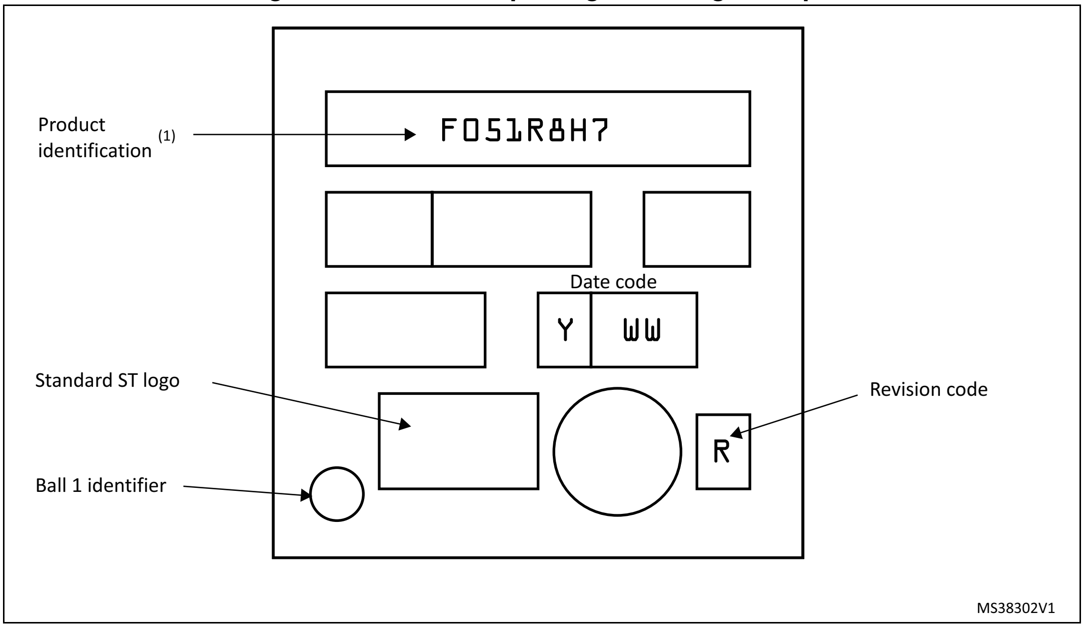

1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

### Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 36. UFBGA64 package marking example**

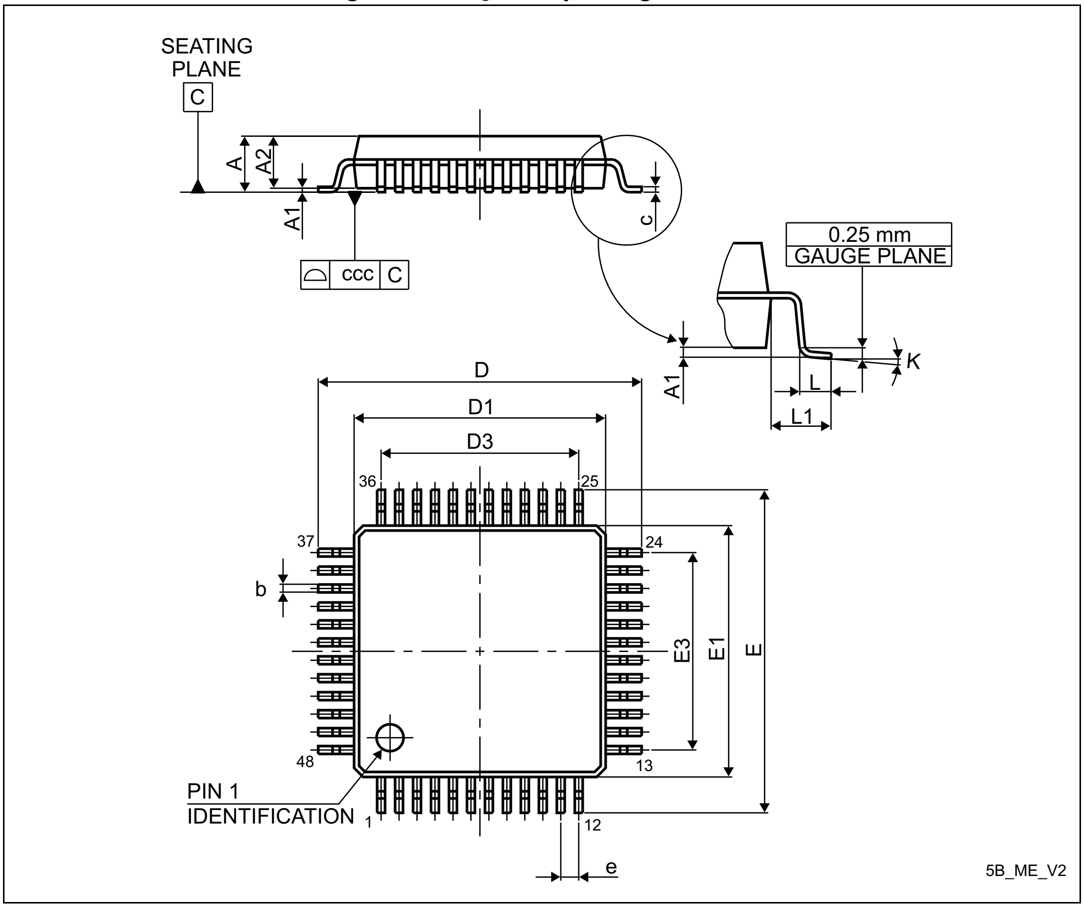



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.3 LQFP48 package information

**LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.**

**Figure 40. LQFP48 package outline**



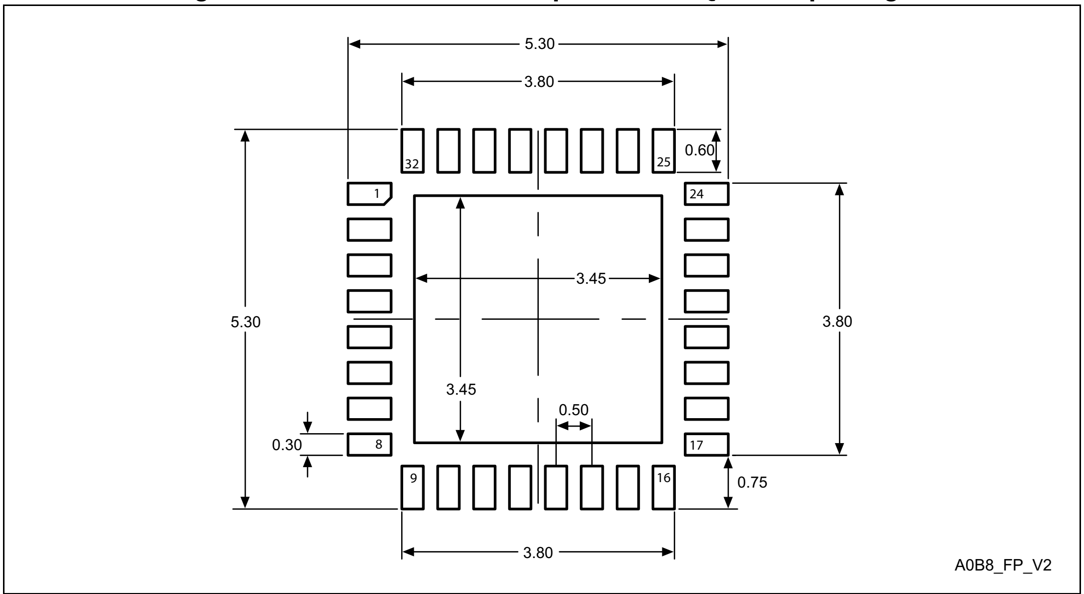

1. Drawing is not to scale.

**Table 73. UFQFPN32 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| A3 | - | 0.152 | - | - | 0.0060 | - |
| b | 0.180 | 0.230 | 0.280 | 0.0071 | 0.0091 | 0.0110 |
| D | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| D1 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| D2 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| E | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| E1 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| E2 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 53. Recommended footprint for UFQFPN32 package**




1. Dimensions are expressed in millimeters.