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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 39 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 13x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-UFQFN Exposed Pad |
| Supplier Device Package | 48-UFQFPN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051c8u6 |

### 3.10.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the $V_{BAT}$ battery voltage using the internal ADC channel ADC_IN18. As the $V_{BAT}$ voltage may be higher than $V_{DDA}$, and thus outside the ADC input range, the $V_{BAT}$ pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the $V_{BAT}$ voltage.

## 3.11 Digital-to-analog converter (DAC)

The 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- DMA capability
- External triggers for conversion

Five DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

## 3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).Refer to *Table 24: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

## 3.13 Touch sensing controller (TSC)

The STM32F051xx devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the

can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

## 3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on $V_{DD}$ supply when present or through the $V_{BAT}$ pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when $V_{DD}$ power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

**Table 9. STM32F051xx I²C implementation (continued)**

| I²C features(1) | I2C1 | I2C2 |
|---|---|---|
| SMBus | X | - |
| Wakeup from STOP | X | - |

1. X = supported.

## 3.17 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds up to two universal synchronous/asynchronous receivers/transmitters (USART1, USART2) which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent of the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

**Table 10. STM32F051xx USART implementation**

| USART modes/features(1) | USART1 | USART2 |
|---|---|---|
| Hardware flow control for modem | X | X |
| Continuous communication using DMA | X | X |
| Multiprocessor communication | X | X |
| Synchronous mode | X | X |
| Smartcard mode | X | - |
| Single-wire half-duplex communication | X | X |
| IrDA SIR ENDEC block | X | - |
| LIN mode | X | - |
| Dual clock domain and wakeup from Stop mode | X | - |
| Receiver timeout interrupt | X | - |
| Modbus communication | X | - |
| Auto baud rate detection | X | - |
| Driver Enable | X | X |

1. X = supported.

**Table 15. Alternate functions selected through GPIOB_AFR registers for port B**

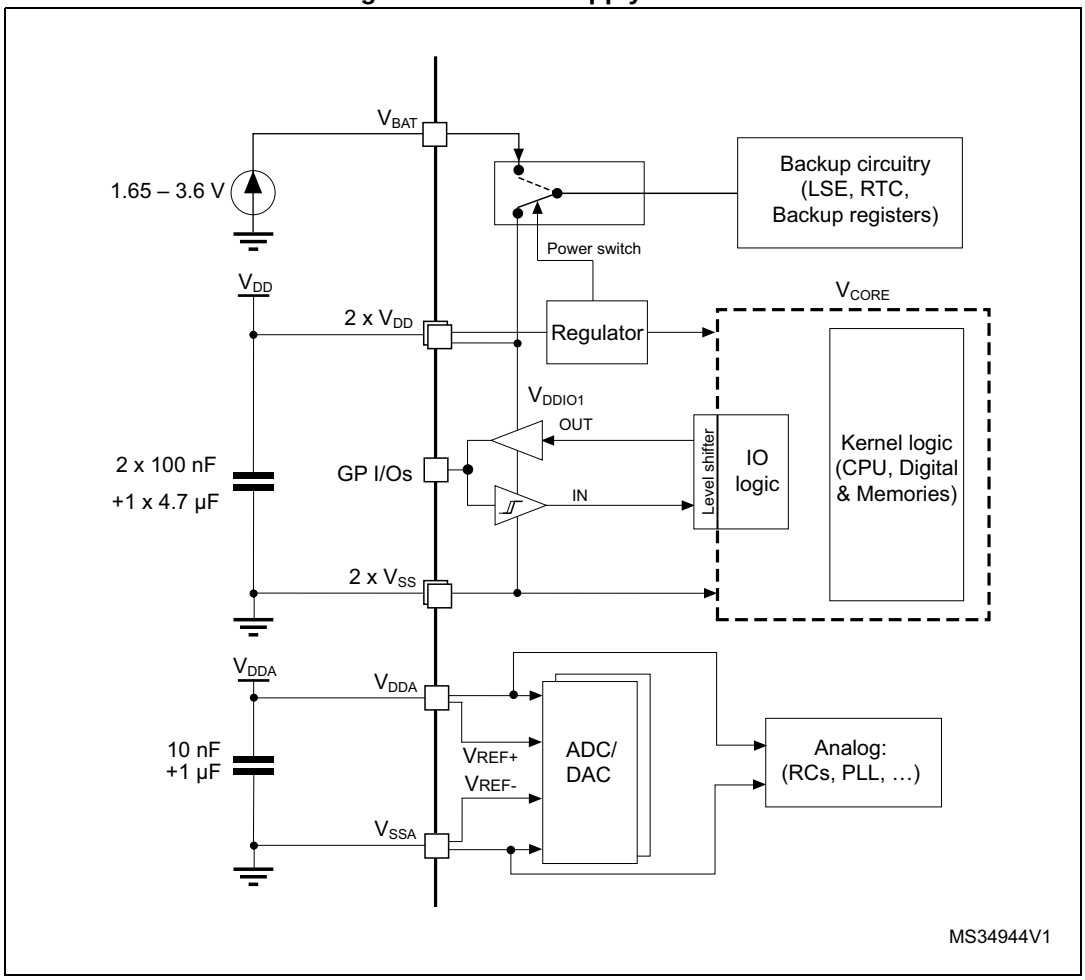
| Pin name | AF0 | AF1 | AF2 | AF3 |
|---|---|---|---|---|
| PB0 | EVENTOUT | TIM3_CH3 | TIM1_CH2N | TSC_G3_IO2 |
| PB1 | TIM14_CH1 | TIM3_CH4 | TIM1_CH3N | TSC_G3_IO3 |
| PB2 | | | | TSC_G3_IO4 |
| PB3 | SPI1_SCK, I2S1_CK | EVENTOUT | TIM2_CH2 | TSC_G5_IO1 |
| PB4 | SPI1_MISO, I2S1_MCK | TIM3_CH1 | EVENTOUT | TSC_G5_IO2 |
| PB5 | SPI1_MOSI, I2S1_SD | TIM3_CH2 | TIM16_BKIN | I2C1_SMBA |
| PB6 | USART1_TX | I2C1_SCL | TIM16_CH1N | TSC_G5_IO3 |
| PB7 | USART1_RX | I2C1_SDA | TIM17_CH1N | TSC_G5_IO4 |
| PB8 | CEC | I2C1_SCL | TIM16_CH1 | TSC_SYNC |
| PB9 | IR_OUT | I2C1_SDA | TIM17_CH1 | EVENTOUT |
| PB10 | CEC | I2C2_SCL | TIM2_CH3 | TSC_SYNC |
| PB11 | EVENTOUT | I2C2_SDA | TIM2_CH4 | TSC_G6_IO1 |
| PB12 | SPI2_NSS | EVENTOUT | TIM1_BKIN | TSC_G6_IO2 |
| PB13 | SPI2_SCK | | TIM1_CH1N | TSC_G6_IO3 |
| PB14 | SPI2_MISO | TIM15_CH1 | TIM1_CH2N | TSC_G6_IO4 |
| PB15 | SPI2_MOSI | TIM15_CH2 | TIM1_CH3N | TIM15_CH1N |

**Table 16. STM32F051xx peripheral register boundary addresses (continued)**

| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| APB | 0x4000 7C00 - 0x4000 7FFF | 1 KB | Reserved |
| | 0x4000 7800 - 0x4000 7BFF | 1 KB | CEC |
| | 0x4000 7400 - 0x4000 77FF | 1 KB | DAC |
| | 0x4000 7000 - 0x4000 73FF | 1 KB | PWR |
| | 0x4000 5C00 - 0x4000 6FFF | 5 KB | Reserved |
| | 0x4000 5800 - 0x4000 5BFF | 1 KB | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | 1 KB | I2C1 |
| | 0x4000 4800 - 0x4000 53FF | 3 KB | Reserved |
| | 0x4000 4400 - 0x4000 47FF | 1 KB | USART2 |
| | 0x4000 3C00 - 0x4000 43FF | 2 KB | Reserved |
| | 0x4000 3800 - 0x4000 3BFF | 1 KB | SPI2 |
| | 0x4000 3400 - 0x4000 37FF | 1 KB | Reserved |
| | 0x4000 3000 - 0x4000 33FF | 1 KB | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | 1 KB | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | 1 KB | RTC |
| | 0x4000 2400 - 0x4000 27FF | 1 KB | Reserved |
| | 0x4000 2000 - 0x4000 23FF | 1 KB | TIM14 |
| | 0x4000 1400 - 0x4000 1FFF | 3 KB | Reserved |
| | 0x4000 1000 - 0x4000 13FF | 1 KB | TIM6 |
| | 0x4000 0800 - 0x4000 0FFF | 2 KB | Reserved |
| | 0x4000 0400 - 0x4000 07FF | 1 KB | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | 1 KB | TIM2 |

### 6.1.6 Power supply scheme

**Figure 13. Power supply scheme**




**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 25* to *Table 31* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

**Table 25. Typical and maximum current consumption from $V_{DD}$ at 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | All peripherals enabled | | | | All peripherals disabled | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ $T_A$(1) | | | Typ | Max @ $T_A$(1) | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| $I_{DD}$ | Supply current in Run mode, code executing from Flash memory | HSE bypass, PLL on | 48 MHz | 22.0 | 22.8 | 22.8 | 23.8 | 11.8 | 12.7 | 12.7 | 13.3 | mA |
| | | | 32 MHz | 15.0 | 15.5 | 15.5 | 16.0 | 7.6 | 8.7 | 8.7 | 9.0 | |
| | | | 24 MHz | 12.2 | 13.2 | 13.2 | 13.6 | 7.2 | 7.9 | 7.9 | 8.1 | |
| | | HSE bypass, PLL off | 8 MHz | 4.4 | 5.2 | 5.2 | 5.4 | 2.7 | 2.9 | 2.9 | 3.0 | |
| | | | 1 MHz | 1.0 | 1.3 | 1.3 | 1.4 | 0.7 | 0.9 | 0.9 | 0.9 | |
| | | HSI clock, PLL on | 48 MHz | 22.0 | 22.8 | 22.8 | 23.8 | 11.8 | 12.7 | 12.7 | 13.3 | |
| | | | 32 MHz | 15.0 | 15.5 | 15.5 | 16.0 | 7.6 | 8.7 | 8.7 | 9.0 | |
| | | | 24 MHz | 12.2 | 13.2 | 13.2 | 13.6 | 7.2 | 7.9 | 7.9 | 8.1 | |
| | | HSI clock, PLL off | 8 MHz | 4.4 | 5.2 | 5.2 | 5.4 | 2.7 | 2.9 | 2.9 | 3.0 | |
| | Supply current in Run mode, code executing from RAM | HSE bypass, PLL on | 48 MHz | 22.2 | 23.2(2) | 23.2 | 24.4(2) | 12.0 | 12.7(2) | 12.7 | 13.3(2) | |
| | | | 32 MHz | 15.4 | 16.3 | 16.3 | 16.8 | 7.8 | 8.7 | 8.7 | 9.0 | |
| | | | 24 MHz | 11.2 | 12.2 | 12.2 | 12.8 | 6.2 | 7.9 | 7.9 | 8.1 | |
| | | HSE bypass, PLL off | 8 MHz | 4.0 | 4.5 | 4.5 | 4.7 | 1.9 | 2.9 | 2.9 | 3.0 | |
| | | | 1 MHz | 0.6 | 0.8 | 0.8 | 0.9 | 0.3 | 0.6 | 0.6 | 0.7 | |
| | | HSI clock, PLL on | 48 MHz | 22.2 | 23.2 | 23.2 | 24.4 | 12.0 | 12.7 | 12.7 | 13.3 | |
| | | | 32 MHz | 15.4 | 16.3 | 16.3 | 16.8 | 7.8 | 8.7 | 8.7 | 9.0 | |
| | | | 24 MHz | 11.2 | 12.2 | 12.2 | 12.8 | 6.2 | 7.9 | 7.9 | 8.1 | |
| | | HSI clock, PLL off | 8 MHz | 4.0 | 4.5 | 4.5 | 4.7 | 1.9 | 2.9 | 2.9 | 3.0 | |

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 35*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 35. HSE oscillator characteristics**

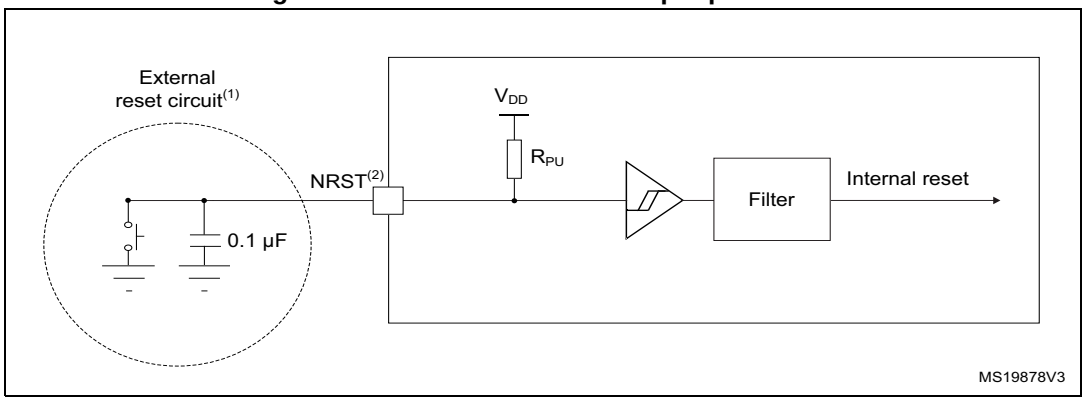
| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | - | 4 | 8 | 32 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| $I_{DD}$ | HSE current consumption | During startup(3) | - | - | 8.5 | mA |
| | | $V_{DD}$ = 3.3 V, Rm = 30 Ω, CL = 10 pF@8 MHz | - | 0.4 | - | |
| | | $V_{DD}$ = 3.3 V, Rm = 45 Ω, CL = 10 pF@8 MHz | - | 0.5 | - | |
| | | $V_{DD}$ = 3.3 V, Rm = 30 Ω, CL = 5 pF@32 MHz | - | 0.8 | - | |
| | | $V_{DD}$ = 3.3 V, Rm = 30 Ω, CL = 10 pF@32 MHz | - | 1 | - | |
| | | $V_{DD}$ = 3.3 V, Rm = 30 Ω, CL = 20 pF@32 MHz | - | 1.5 | - | |
| $g_m$ | Oscillator transconductance | Startup | 10 | - | - | mA/V |
| $t_{SU(HSE)}$(4) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.*

**Figure 24. Recommended NRST pin protection**




1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 51: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

## 6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the conditions summarized in *Table 20: General operating conditions*.

*Note: It is recommended to perform a calibration after each power-up.*

**Table 52. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage for ADC ON | - | 2.4 | - | 3.6 | V |
| $I_{DDA\ (ADC)}$ | Current consumption of the ADC(1) | $V_{DDA}$ = 3.3 V | - | 0.9 | - | mA |
| $f_{ADC}$ | ADC clock frequency | - | 0.6 | - | 14 | MHz |
| $f_S$(2) | Sampling rate | 12-bit resolution | 0.043 | - | 1 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 14 MHz, 12-bit resolution | - | - | 823 | kHz |
| | | 12-bit resolution | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | - | 0 | - | $V_{DDA}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* and *Table 53* for details | - | - | 50 | kΩ |
| $R_{ADC}$(2) | Sampling switch resistance | - | - | - | 1 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | - | - | - | 8 | pF |
| $t_{CAL}$(2)(3) | Calibration time | $f_{ADC}$ = 14 MHz | 5.9 | | | µs |
| | | - | 83 | | | $1/f_{ADC}$ |

**Table 52. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $W_{LATENCY}$(2)(4) | ADC_DR register ready latency | ADC clock = HSI14 | 1.5 ADC cycles + 2 $f_{PCLK}$ cycles | - | 1.5 ADC cycles + 3 $f_{PCLK}$ cycles | - |
| | | ADC clock = PCLK/2 | - | 4.5 | - | $f_{PCLK}$ cycle |
| | | ADC clock = PCLK/4 | - | 8.5 | - | $f_{PCLK}$ cycle |
| $t_{latr}$(2) | Trigger conversion latency | $f_{ADC} = f_{PCLK}/2 = 14$ MHz | 0.196 | | | µs |
| | | $f_{ADC} = f_{PCLK}/2$ | 5.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{PCLK}/4 = 12$ MHz | 0.219 | | | µs |
| | | $f_{ADC} = f_{PCLK}/4$ | 10.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{HSI14} = 14$ MHz | 0.179 | - | 0.250 | µs |
| $Jitter_{ADC}$ | ADC jitter on trigger conversion | $f_{ADC} = f_{HSI14}$ | - | 1 | - | $1/f_{HSI14}$ |
| $t_S$(2) | Sampling time | $f_{ADC} = 14$ MHz | 0.107 | - | 17.1 | µs |
| | | - | 1.5 | - | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Stabilization time | - | 14 | | | $1/f_{ADC}$ |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC} = 14$ MHz, 12-bit resolution | 1 | - | 18 | µs |
| | | 12-bit resolution | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on $I_{DDA}$ and 60 µA on $I_{DD}$ should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

**Equation 1: $R_{AIN}$ max formula**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 53. $R_{AIN}$ max for $f_{ADC}$ = 14 MHz**

| $T_s$ (cycles) | $t_S$ (µs) | $R_{AIN}$ max (kΩ)(1) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |

**Table 56. Comparator characteristics (continued)**

| Symbol | Parameter | Conditions | | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Comparator hysteresis | No hysteresis (COMPxHYST[1:0]=00) | - | - | 0 | - | mV |
| | | Low hysteresis (COMPxHYST[1:0]=01) | High speed mode | 3 | 8 | 13 | |
| | | | All other power modes | 5 | | 10 | |
| | | Medium hysteresis (COMPxHYST[1:0]=10) | High speed mode | 7 | 15 | 26 | |
| | | | All other power modes | 9 | | 19 | |
| | | High hysteresis (COMPxHYST[1:0]=11) | High speed mode | 18 | 31 | 49 | |
| | | | All other power modes | 19 | | 40 | |

1. Data based on characterization results, not tested in production.
2. For more details and conditions see *Figure 28: Maximum $V_{REFINT}$ scaler startup time from power down*.

**Figure 28. Maximum $V_{REFINT}$ scaler startup time from power down**

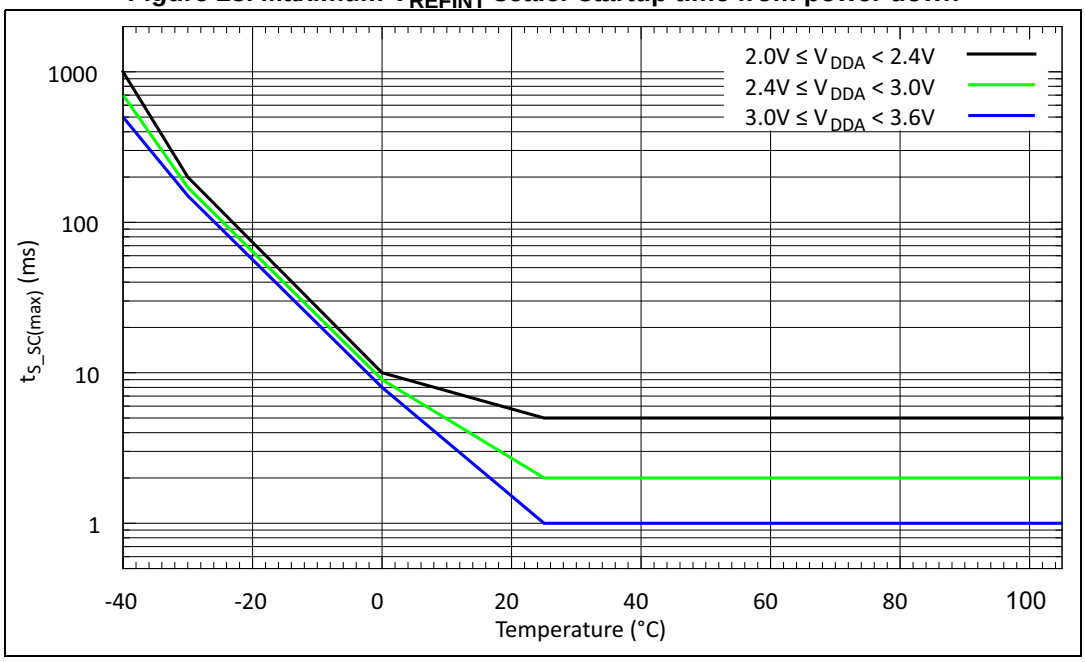


**Table 60. IWDG min/max timeout period at 40 kHz (LSI)(1)**

| Prescaler divider | PR[2:0] bits | Min timeout RL[11:0]= 0x000 | Max timeout RL[11:0]= 0xFFF | Unit |
|---|---|---|---|---|
| /4 | 0 | 0.1 | 409.6 | ms |
| /8 | 1 | 0.2 | 819.2 | |
| /16 | 2 | 0.4 | 1638.4 | |
| /32 | 3 | 0.8 | 3276.8 | |
| /64 | 4 | 1.6 | 6553.6 | |
| /128 | 5 | 3.2 | 13107.2 | |
| /256 | 6 or 7 | 6.4 | 26214.4 | |

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

**Table 61. WWDG min/max timeout value at 48 MHz (PCLK)**

| Prescaler | WDGTB | Min timeout value | Max timeout value | Unit |
|---|---|---|---|---|
| 1 | 0 | 0.0853 | 5.4613 | ms |
| 2 | 1 | 0.1706 | 10.9226 | |
| 4 | 2 | 0.3413 | 21.8453 | |
| 8 | 3 | 0.6826 | 43.6906 | |

## 6.3.22 Communication interfaces

### $I^2C$ interface characteristics

The $I^2C$ interface meets the timings requirements of the $I^2C$-bus specification and user manual rev. 03 for:

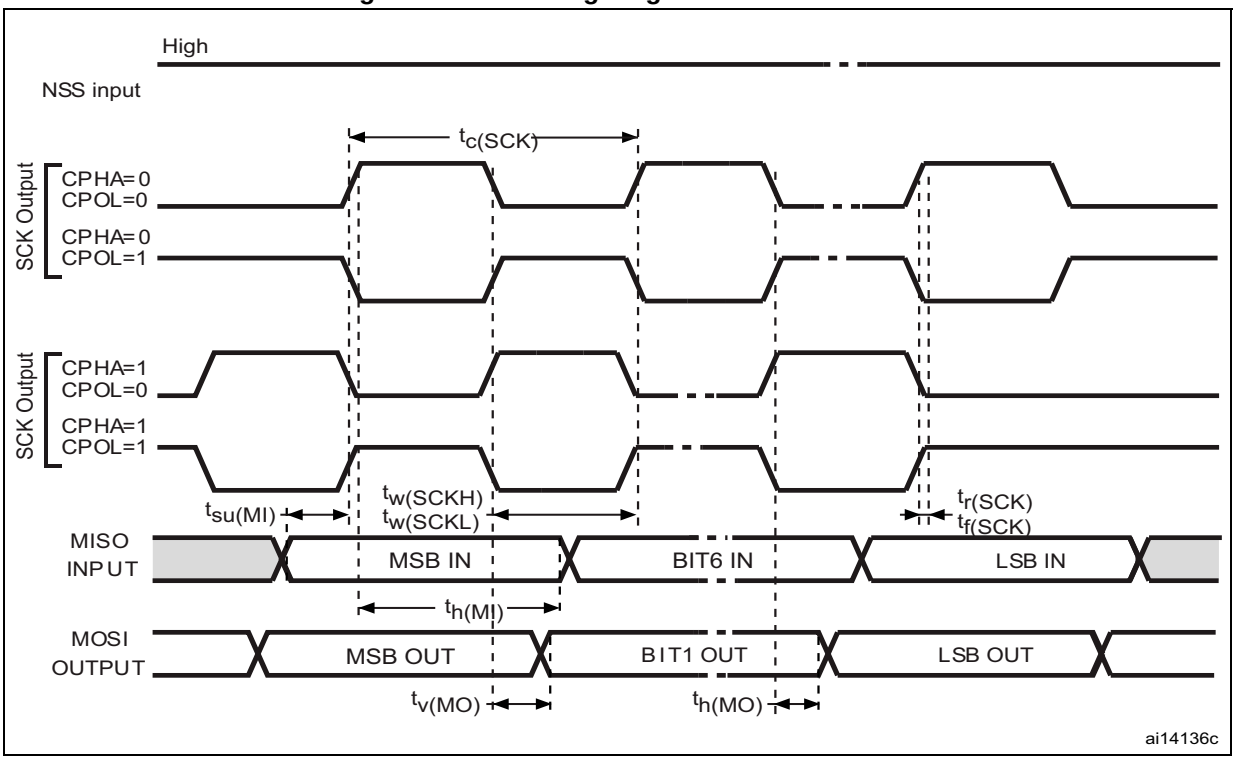
- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The $I^2C$ timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DDIOx}$ is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the $I^2C$ I/Os characteristics.

All $I^2C$ SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

**Figure 31. SPI timing diagram - master mode**




1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Table 64. $I^2S$ characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CK}$ $1/t_{c(CK)}$ | $I^2S$ clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | 1.597 | 1.601 | MHz |
| | | Slave mode | 0 | 6.5 | |
| $t_{r(CK)}$ | $I^2S$ clock rise time | Capacitive load $C_L$ = 15 pF | - | 10 | ns |
| $t_{f(CK)}$ | $I^2S$ clock fall time | | - | 12 | |
| $t_{w(CKH)}$ | $I^2S$ clock high time | Master $f_{PCLK}$= 16 MHz, audio frequency = 48 kHz | 306 | - | |
| $t_{w(CKL)}$ | $I^2S$ clock low time | | 312 | - | |
| $t_{v(WS)}$ | WS valid time | Master mode | 2 | - | |
| $t_{h(WS)}$ | WS hold time | Master mode | 2 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 7 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 0 | - | |
| DuCy(SCK) | $I^2S$ slave input clock duty cycle | Slave mode | 25 | 75 | % |

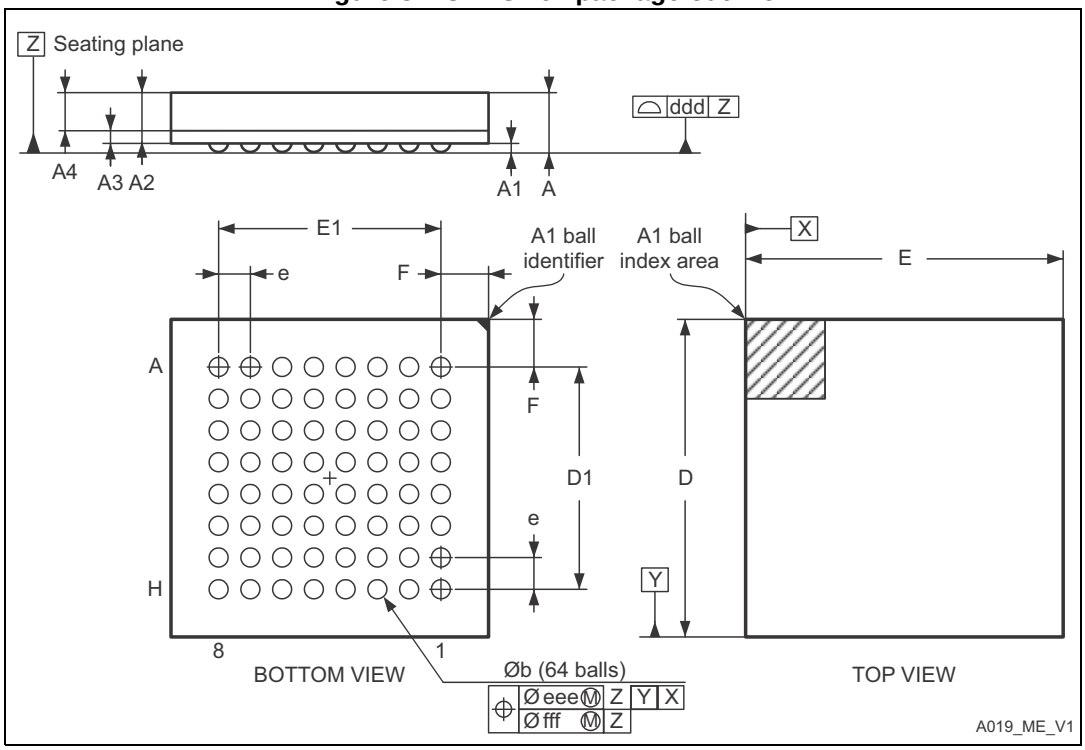
# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 7.1 UFBGA64 package information

**UFBGA64 is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra-fine-profile ball grid array package.**

**Figure 34. UFBGA64 package outline**




1. Drawing is not to scale.

**Table 65. UFBGA64 package mechanical data**

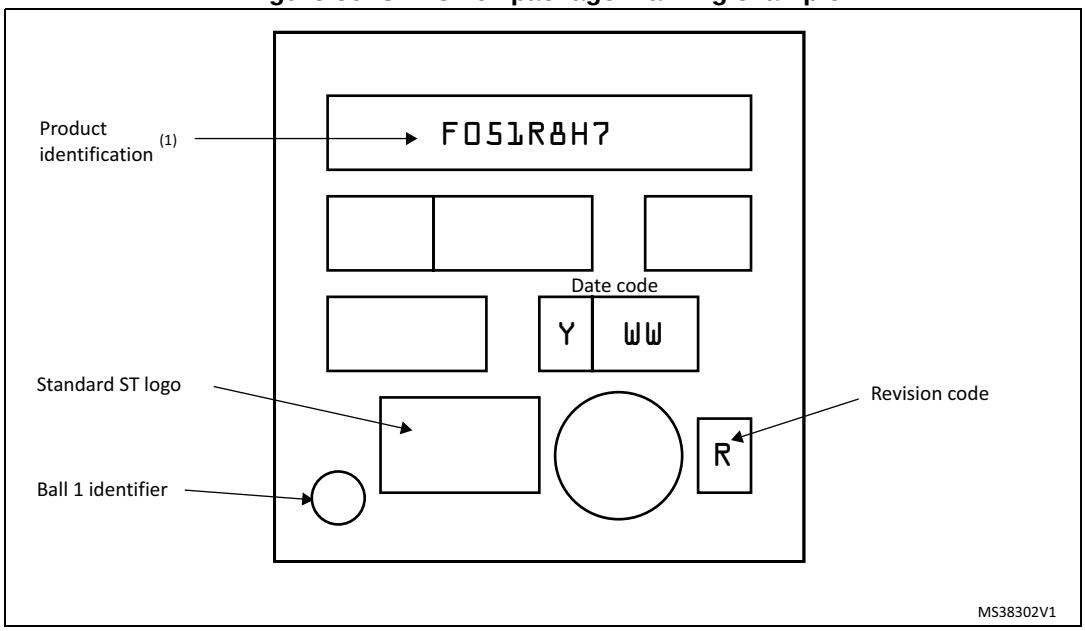
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | 0.080 | 0.130 | 0.180 | 0.0031 | 0.0051 | 0.0071 |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |

### Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 36. UFBGA64 package marking example**

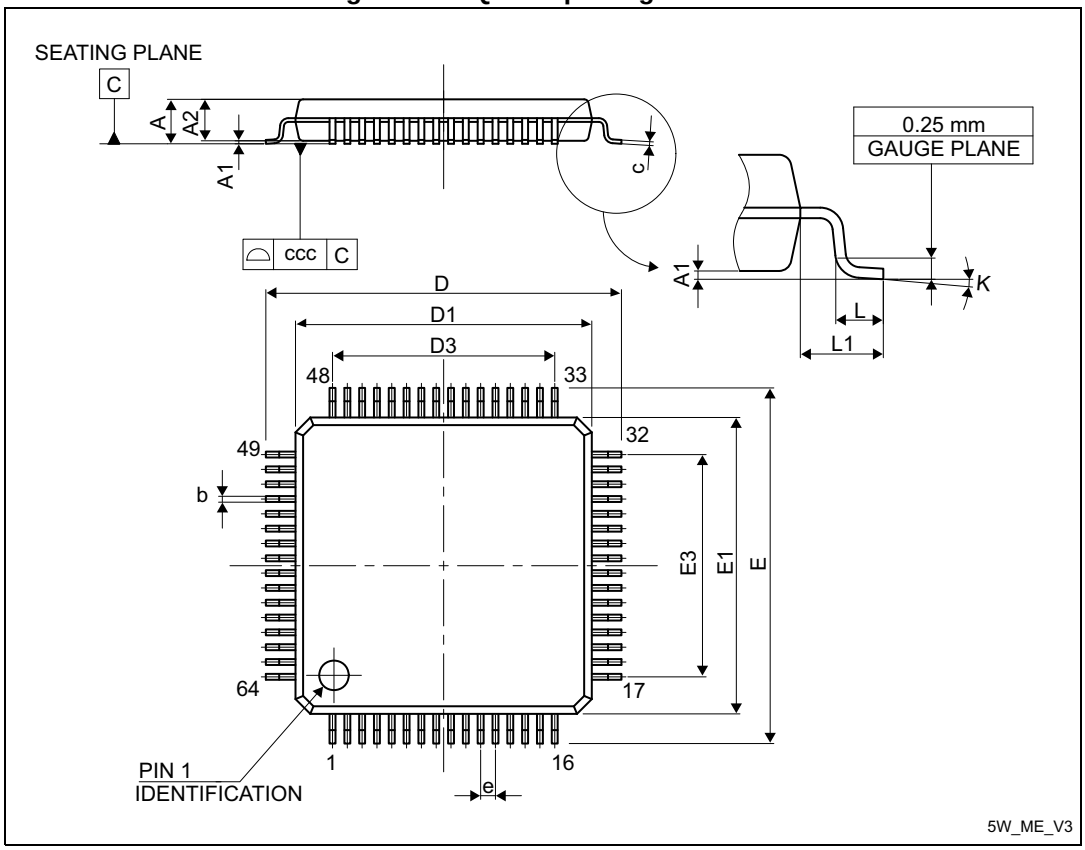



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.2 LQFP64 package information

**LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.**

**Figure 37. LQFP64 package outline**




1. Drawing is not to scale.

**Table 67. LQFP64 package mechanical data**

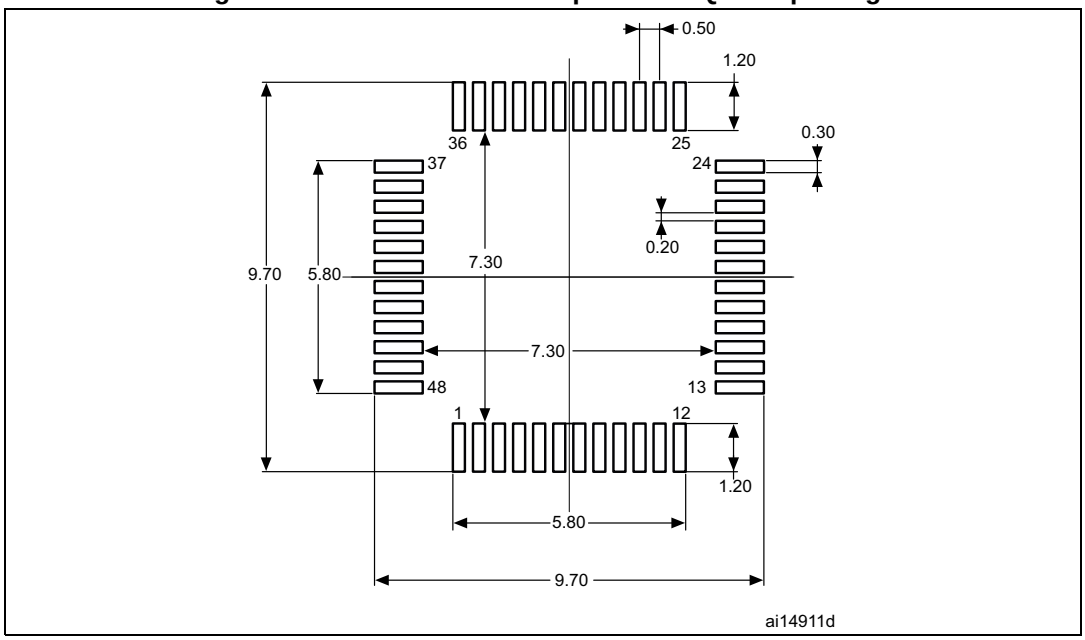
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |

**Table 68. LQFP48 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 41. Recommended footprint for LQFP48 package**



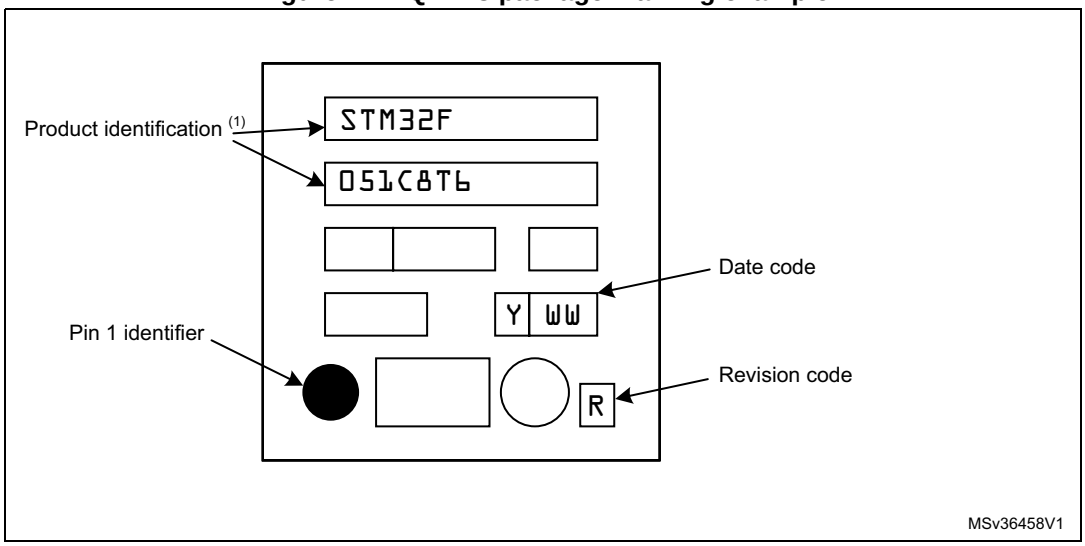

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 42. LQFP48 package marking example**



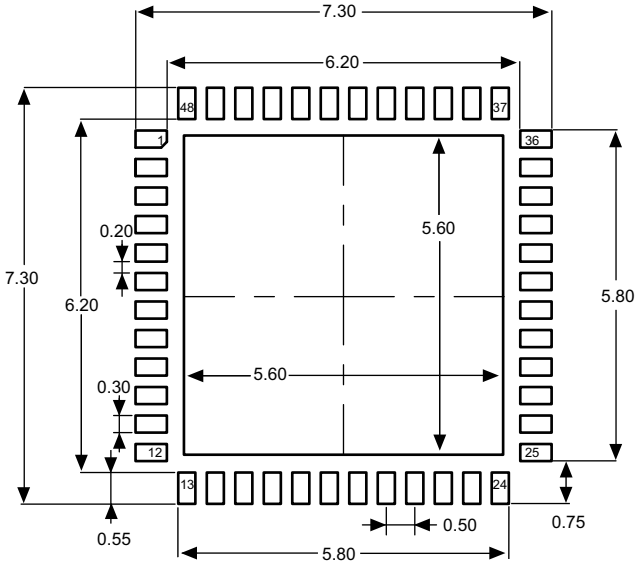

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

**Table 69. UFQFPN48 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| D | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| E | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| D2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| E2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| T | - | 0.152 | - | - | 0.0060 | - |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 44. Recommended footprint for UFQFPN48 package**




1. Dimensions are expressed in millimeters.