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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	39
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051c8u6tr

List of tables

List of figures

3.14 Timers and watchdogs

The STM32F051xx devices include up to six general-purpose timers, one basic timer and an advanced control timer.

Table 7 compares the features of the different timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6	16-bit	Up	integer from 1 to 65536	Yes	-	-

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input-only pin
		I/O	Input / output pin
I/O structure		FT	5 V-tolerant I/O
		FTf	5 V-tolerant I/O, FM+ capable
		TTa	3.3 V-tolerant I/O directly connected to ADC
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. Pin definitions

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	UFBGA64	LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32					Alternate functions	Additional functions
1	B2	1	-	-	-	VBAT	S	-	-	Backup power supply	
2	A2	2	A6	-	-	PC13	I/O	TC	(1)(2)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	A1	3	B6	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1)(2)	-	OSC32_IN
4	B1	4	C6	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1)(2)	-	OSC32_OUT
5	C1	5	B5	2	2	PF0-OSC_IN (PF0)	I/O	FT	-	-	OSC_IN
6	D1	6	C5	3	3	PF1-OSC_OUT (PF1)	I/O	FT	-	-	OSC_OUT

Table 13. Pin definitions (continued)

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	UFBGA64	LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32					Alternate functions	Additional functions
22	G4	16	E3	12	12	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT	ADC_IN6
23	H4	17	F4	13	13	PA7	I/O	TTa	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
24	H5	-	-	-	-	PC4	I/O	TTa	-	EVENTOUT	ADC_IN14
25	H6	-	-	-	-	PC5	I/O	TTa	-	TSC_G3_IO1	ADC_IN15
26	F5	18	F3	14	14	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	ADC_IN8
27	G5	19	F2	15	15	PB1	I/O	TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
28	G6	20	D2	-	16	PB2	I/O	FT	(4)	TSC_G3_IO4	-
29	G7	21	-	-	-	PB10	I/O	FT	(5)	I2C2_SCL, CEC, TIM2_CH3, TSC_SYNC	-
30	H7	22	-	-	-	PB11	I/O	FT	(5)	I2C2_SDA, TIM2_CH4, TSC_G6_IO1, EVENTOUT	-
31	D4	23	F1	16	0	VSS	S	-	-	Ground	
32	E4	24	E1	17	17	VDD	S	-	-	Digital power supply	

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme

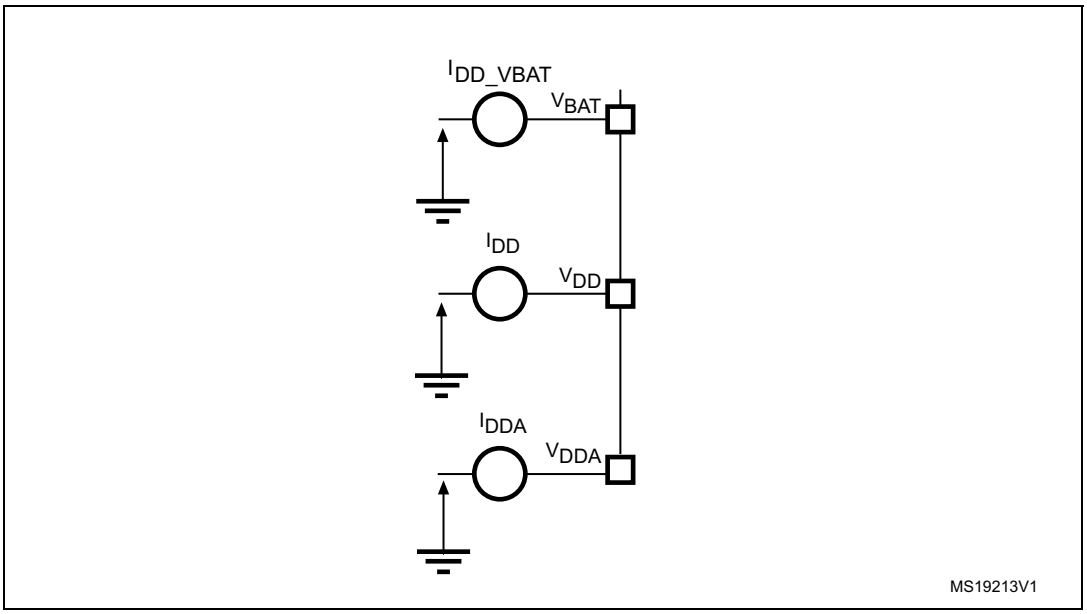


Table 21. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 22. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge(2)	1.80	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.00	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(4)	Reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

Table 23. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 31*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 17: Voltage characteristics*

Table 31. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB	BusMatrix(1)	5	µA/MHz
	DMA1	7	
	SRAM	1	
	Flash memory interface	14	
	CRC	2	
	GPIOA	9	
	GPIOB	12	
	GPIOC	2	
	GPIOD	1	
	GPIOF	1	
	TSC	6	
	All AHB peripherals	**55**	

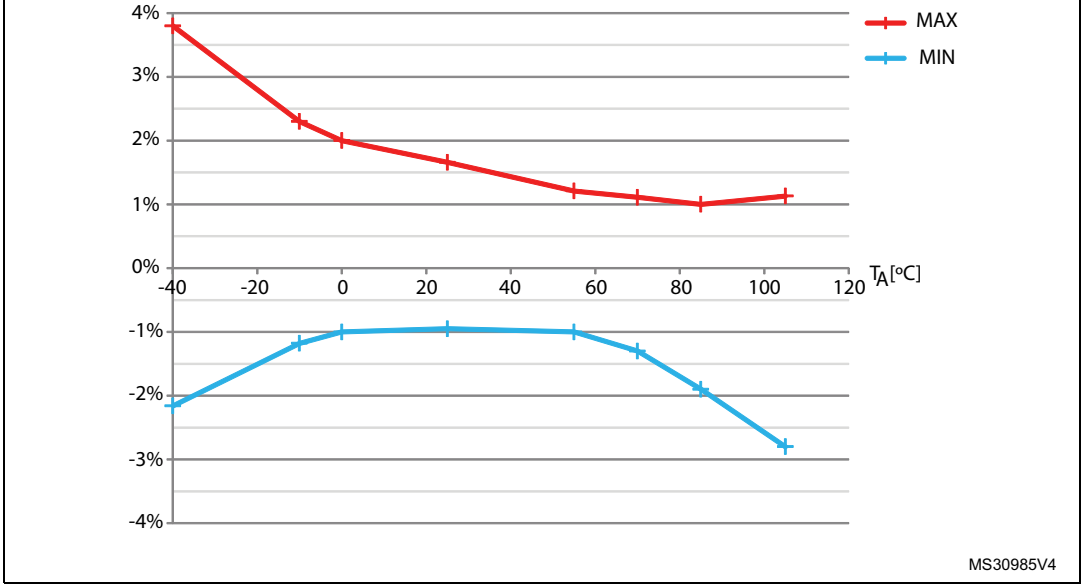
High-speed internal (HSI) RC oscillator

Table 37. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 19. HSI oscillator accuracy characterization results for soldered parts



High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 38. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1(2)	%
$DuCy_{(HSI14)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 105 °C	–4.2(3)	-	5.1(3)	%
		T_A = –10 to 85 °C	–3.2(3)	-	3.1(3)	%
		T_A = 0 to 70 °C	–2.5(3)	-	2.3(3)	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI14)}$	HSI14 oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption	-	-	100	150(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 20. HSI14 oscillator accuracy characterization results

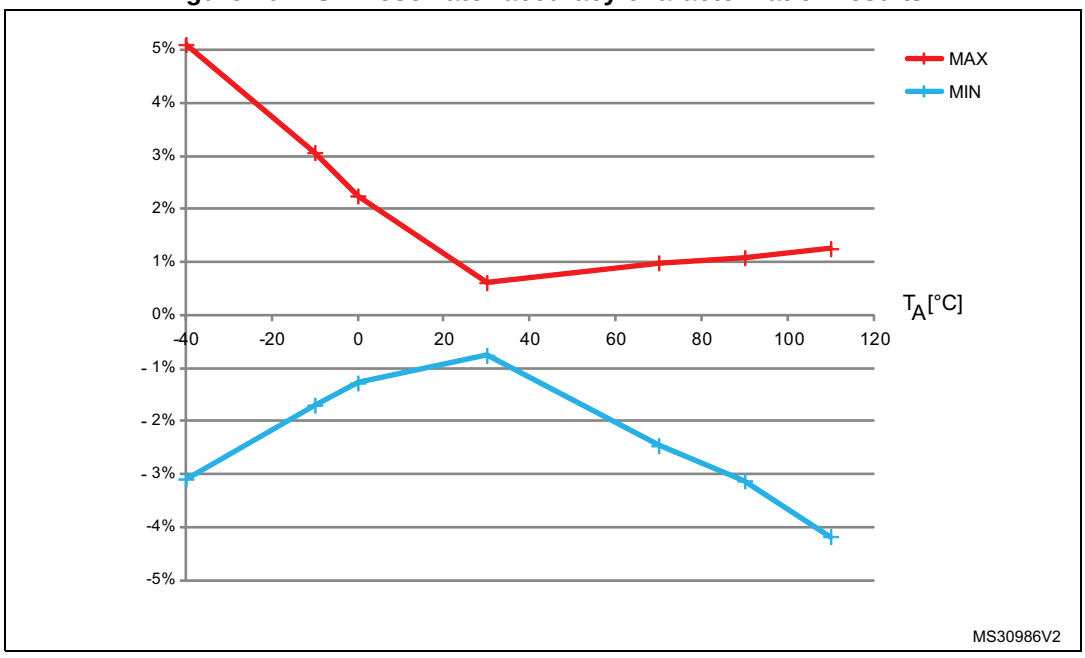


Table 42. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycle
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Year
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycle(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 43*. They are based on the EMS levels and classes defined in application note AN1709.

Table 43. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-4	4B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Table 45. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	All	C3	250	V

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 46. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 47*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Figure 21. TC and TTa I/O input characteristics

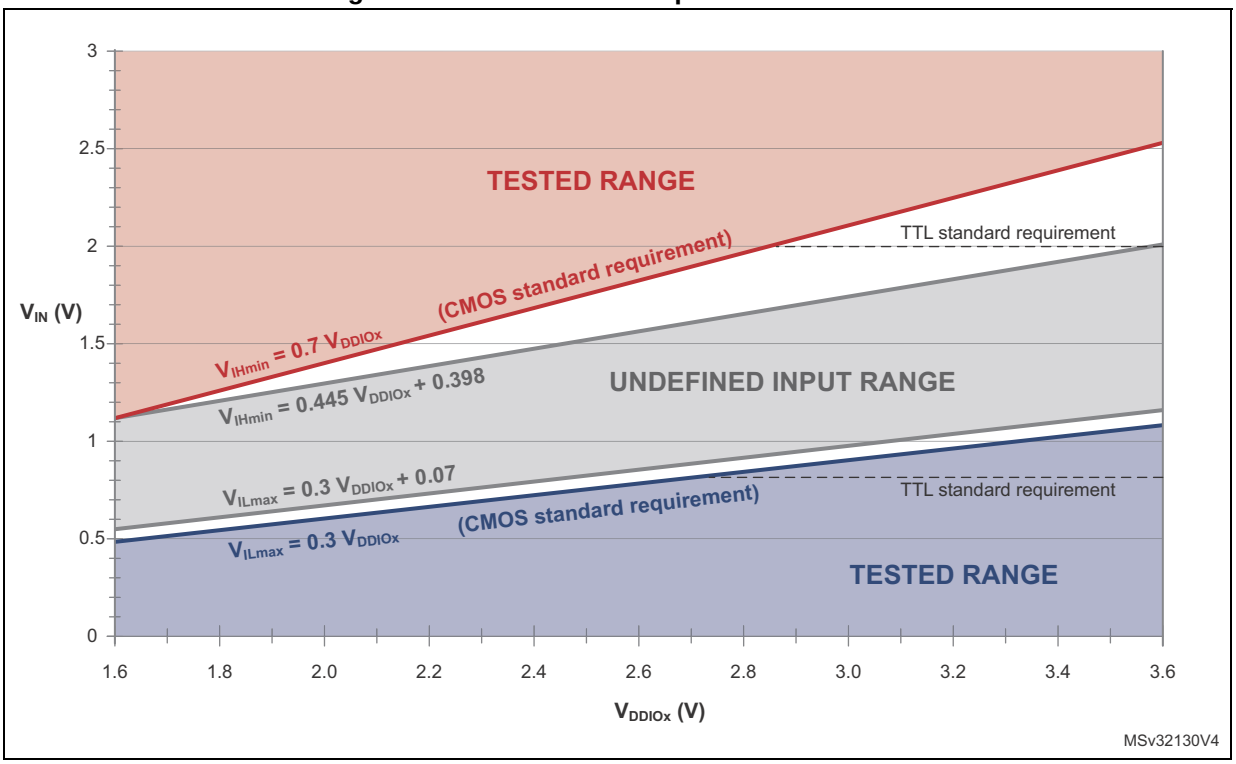
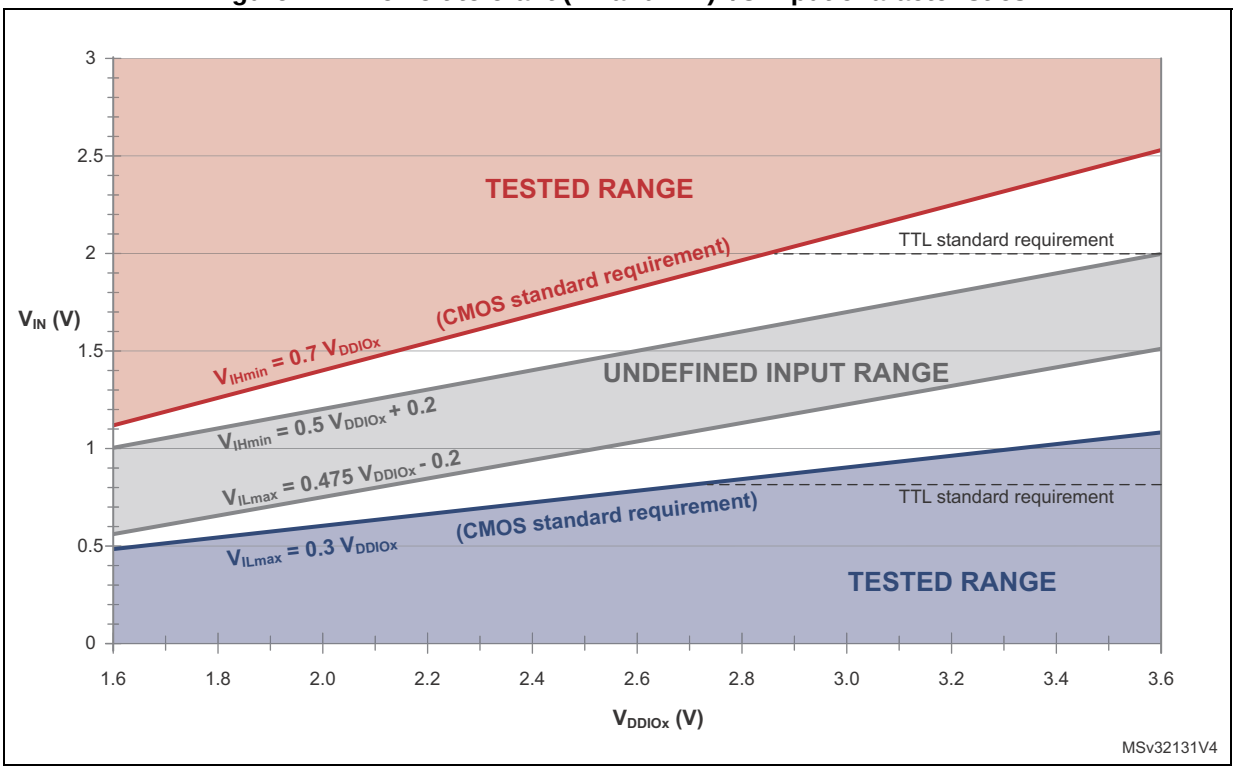


Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 17: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 17: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 49. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}–1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 6 mA	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OLFm+}(3)	Output low level voltage for an FTf I/O pin in Fm+ mode	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
		$\|I_{IO}\|$ = 10 mA	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 17: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.

Table 52. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$W_{LATENCY}$(2)(4)	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(2)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 14$ MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 12$ MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14} = 14$ MHz	0.179	-	0.250	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S(2)	Sampling time	$f_{ADC} = 14$ MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Stabilization time	-	14			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	$f_{ADC} = 14$ MHz, 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 53. R_{AIN} max for f_{ADC} = 14 MHz

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4

6.3.17 DAC electrical specifications

Table 55. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	Load connected to V_{SSA}
		25	-	-	kΩ	Load connected to V_{DDA}
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{DDA} – 1LSB	V	
I_{DDA}(1)	DAC DC current consumption in quiescent mode(2)	-	-	600	µA	With no load, middle code (0x800) on the input
		-	-	700	µA	With no load, worst code (0xF1C) on the input
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	±2	LSB	Given for the DAC in 12-bit configuration
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration
		-	-	±4	LSB	Given for the DAC in 12-bit configuration
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{DDA}/2)	-	-	±10	mV	-
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{DDA} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{DDA} = 3.6 V

6.3.18 Comparator characteristics

Table 56. Comparator characteristics

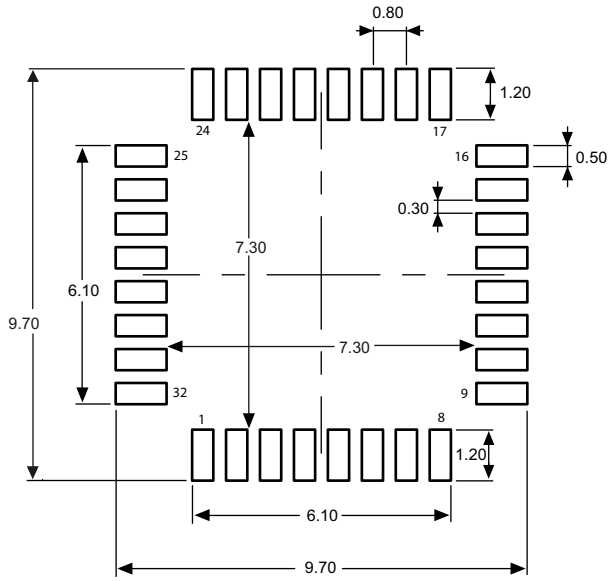
Symbol	Parameter	Conditions		Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-		V_{DD}	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	-
V_{SC}	V_{REFINT} scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1000 (2)	ms
		Next activations		-	-	0.2	
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

Table 72. LQFP32 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 50. Recommended footprint for LQFP32 package



1. Dimensions are expressed in millimeters.

7.8 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 20: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 74. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP32 - 7 × 7 mm	56	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm	65	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	
	Thermal resistance junction-ambient UFQFPN32 - 5 × 5 mm	38	
	Thermal resistance junction-ambient WLCSP36 - 2.6 × 2.7 mm	60	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 75. Ordering information scheme

Example: STM32 F 051 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

051 = STM32F051xx

Pin count

K = 32 pins
T = 36 pins
C = 48 pins
R = 64 pins

User code memory size

4 = 16 Kbyte
6 = 32 Kbyte
8 = 64 Kbyte

Package

H = UFBGA
T = LQFP
U = UFQFPN
Y = WLCSP

Temperature range

6 = –40 °C to +85 °C
7 = –40 °C to +105 °C

Options

xxx = code ID of programmed parts (includes packing type)
TR = tape and reel packing
blank = tray packing