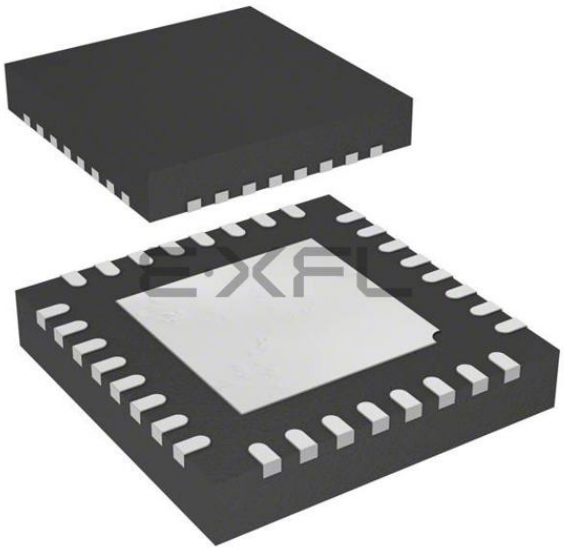

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051k4u6tr

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In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F051xx microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1,, COMPx or the CEC.

  The CEC, USART1 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- DMA capability
- External triggers for conversion

Five DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).Refer to *Table 24: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.13 Touch sensing controller (TSC)

The STM32F051xx devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the

hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 5. Capacitive sensing GPIOs available on STM32F051xx devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	4	TSC_G4_IO1	PA9
	TSC_G1_IO2	PA1		TSC_G4_IO2	PA10
	TSC_G1_IO3	PA2		TSC_G4_IO3	PA11
	TSC_G1_IO4	PA3		TSC_G4_IO4	PA12
2	TSC_G2_IO1	PA4	5	TSC_G5_IO1	PB3
	TSC_G2_IO2	PA5		TSC_G5_IO2	PB4
	TSC_G2_IO3	PA6		TSC_G5_IO3	PB6
	TSC_G2_IO4	PA7		TSC_G5_IO4	PB7
3	TSC_G3_IO1	PC5	6	TSC_G6_IO1	PB11
	TSC_G3_IO2	PB0		TSC_G6_IO2	PB12
	TSC_G3_IO3	PB1		TSC_G6_IO3	PB13
	TSC_G3_IO4	PB2		TSC_G6_IO4	PB14

Table 6. Effective number of capacitive sensing channels on STM32F051xx

Analog I/O group	Number of capacitive sensing channels				
	STM32F051Rx	STM32F051Cx	STM32F051Tx	STM32F051KxU (UFQFPN32)	STM32F051KxT (LQFP32)
G1	3	3	3	3	3
G2	3	3	3	3	3
G3	3	2	2	2	1
G4	3	3	3	3	3
G5	3	3	3	3	3
G6	3	3	0	0	0
Number of capacitive sensing channels	18	17	14	14	13

3.14 Timers and watchdogs

The STM32F051xx devices include up to six general-purpose timers, one basic timer and an advanced control timer.

Table 7 compares the features of the different timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6	16-bit	Up	integer from 1 to 65536	Yes	-	-

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.14.2 General-purpose timers (TIM2, 3, 14, 15, 16, 17)

There are six synchronizable general-purpose timers embedded in the STM32F051xx devices (see *Table 7* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F051xx devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate withTIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.14.3 Basic timer TIM6

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

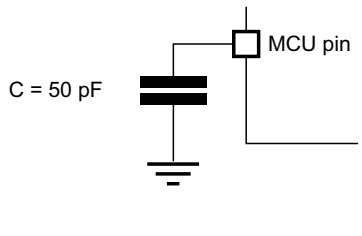


Figure 12. Pin input voltage

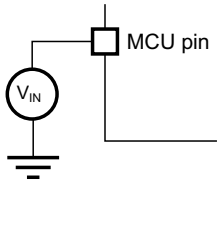


Table 25. Typical and maximum current consumption from V_{DD} at 3.6 V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Sleep mode	HSE bypass, PLL on	48 MHz	14.0	15.3(2)	15.3	16.0(2)	2.8	3.0(2)	3.0	3.2(2)	mA
			32 MHz	9.5	10.2	10.2	10.7	2.0	2.1	2.1	2.3	
			24 MHz	7.3	7.8	7.8	8.3	1.5	1.7	1.7	1.9	
		HSE bypass, PLL off	8 MHz	2.6	2.9	2.9	3.0	0.6	0.8	0.8	0.8	
			1 MHz	0.4	0.6	0.6	0.6	0.2	0.4	0.4	0.4	
		HSI clock, PLL on	48 MHz	14.0	15.3	15.3	16.0	3.8	4.0	4.1	4.2	
			32 MHz	9.5	10.2	10.2	10.7	2.6	2.7	2.8	2.8	
			24 MHz	7.3	7.8	7.8	8.3	2.0	2.1	2.1	2.1	
		HSI clock, PLL off	8 MHz	2.6	2.9	2.9	3.0	0.6	0.8	0.8	0.8	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 26. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSE bypass, PLL on	48 MHz	150	170(3)	178	182(3)	164	183(3)	195	198(3)	µA
			32 MHz	104	121	126	128	113	129	135	138	
			24 MHz	82	96	100	103	88	102	106	108	
		HSE bypass, PLL off	8 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
			1 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
		HSI clock, PLL on	48 MHz	220	240	248	252	244	263	275	278	
			32 MHz	174	191	196	198	193	209	215	218	
			24 MHz	152	167	173	174	168	183	190	192	
		HSI clock, PLL off	8 MHz	72	79	82	83	83.5	91	94	95	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent of clock frequencies.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 35*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 35. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.4	-	
		V_{DD} = 3.3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 5 pF@32 MHz	-	0.8	-	
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 10 pF@32 MHz	-	1	-	
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

6.3.17 DAC electrical specifications

Table 55. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	Load connected to V_{SSA}
		25	-	-	kΩ	Load connected to V_{DDA}
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{DDA} – 1LSB	V	
I_{DDA}(1)	DAC DC current consumption in quiescent mode(2)	-	-	600	µA	With no load, middle code (0x800) on the input
		-	-	700	µA	With no load, worst code (0xF1C) on the input
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	±2	LSB	Given for the DAC in 12-bit configuration
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration
		-	-	±4	LSB	Given for the DAC in 12-bit configuration
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{DDA}/2)	-	-	±10	mV	-
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{DDA} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{DDA} = 3.6 V

6.3.18 Comparator characteristics

Table 56. Comparator characteristics

Symbol	Parameter	Conditions		Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-		V_{DD}	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	-
V_{SC}	V_{REFINT} scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1000 (2)	ms
		Next activations		-	-	0.2	
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

Table 56. Comparator characteristics (continued)

Symbol	Parameter	Conditions		Min(1)	Typ	Max(1)	Unit
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

1. Data based on characterization results, not tested in production.
2. For more details and conditions see *Figure 28: Maximum V_{REFINT} scaler startup time from power down*.

Figure 28. Maximum V_{REFINT} scaler startup time from power down

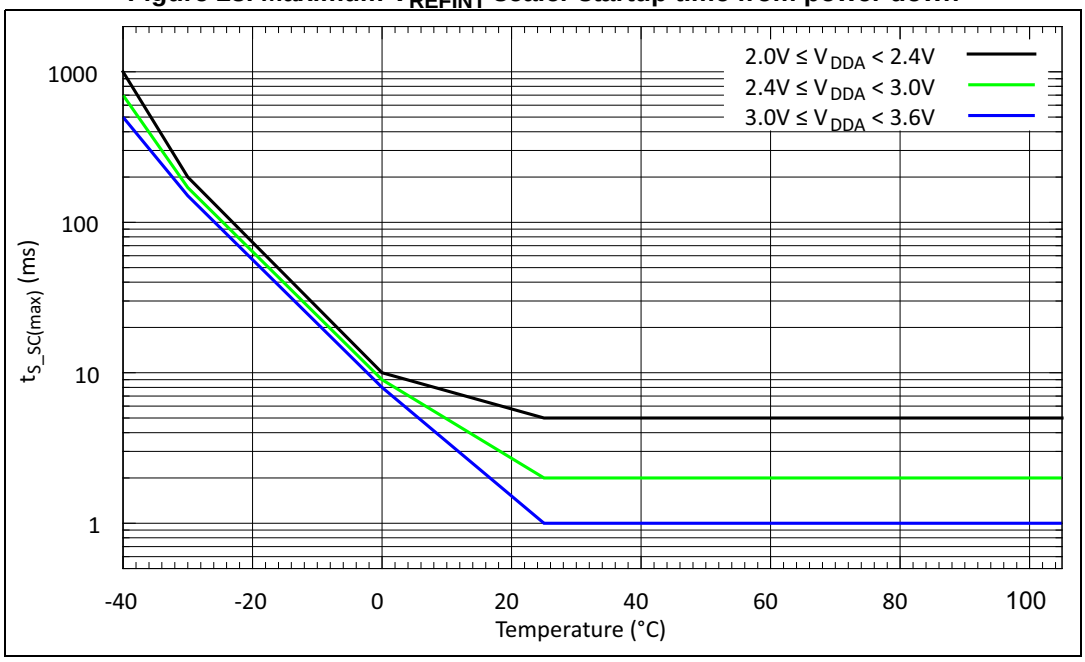


Table 62. I²C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 63* for SPI or in *Table 64* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 20: General operating conditions*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 63. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 29. SPI timing diagram - slave mode and CPHA = 0

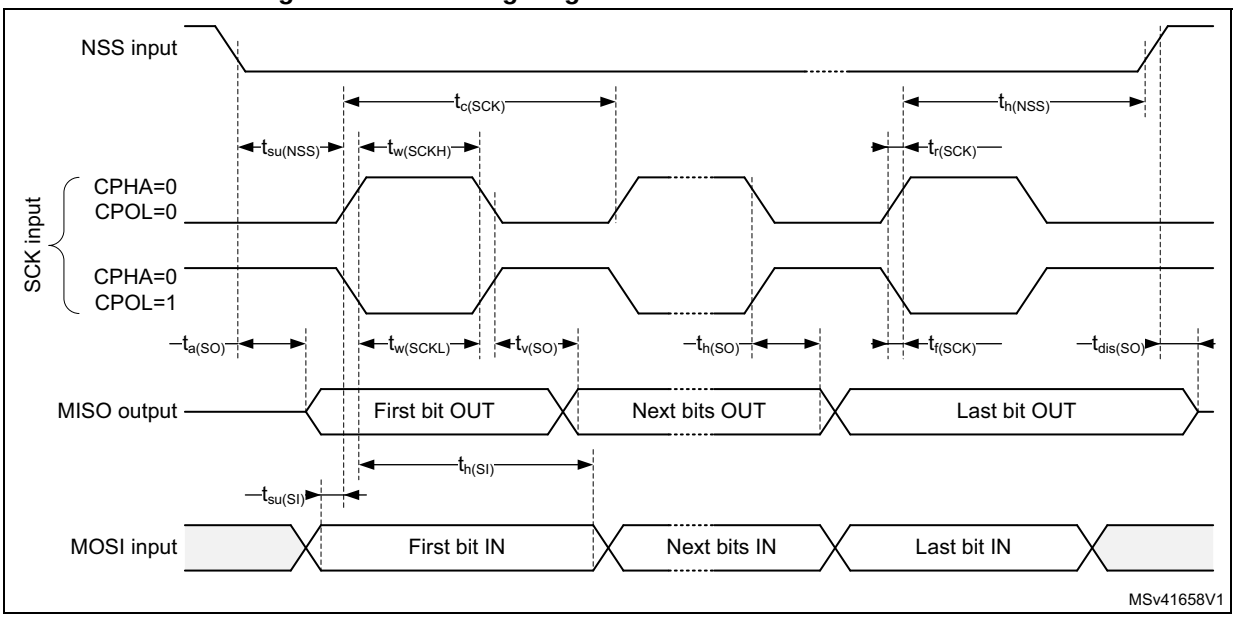
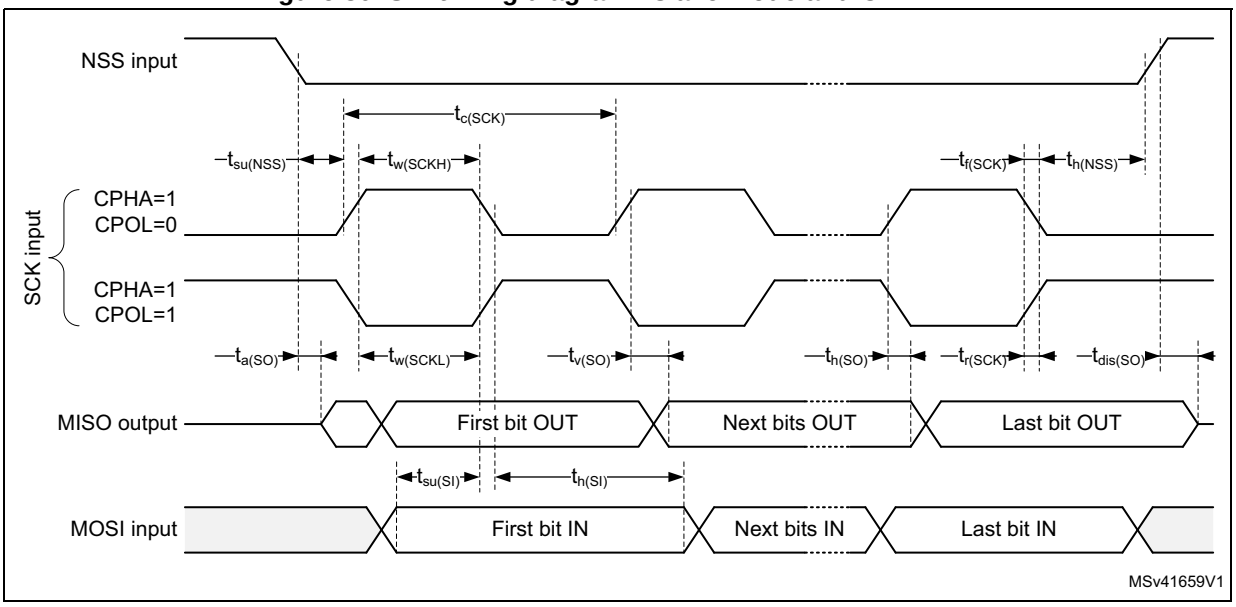


Figure 30. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

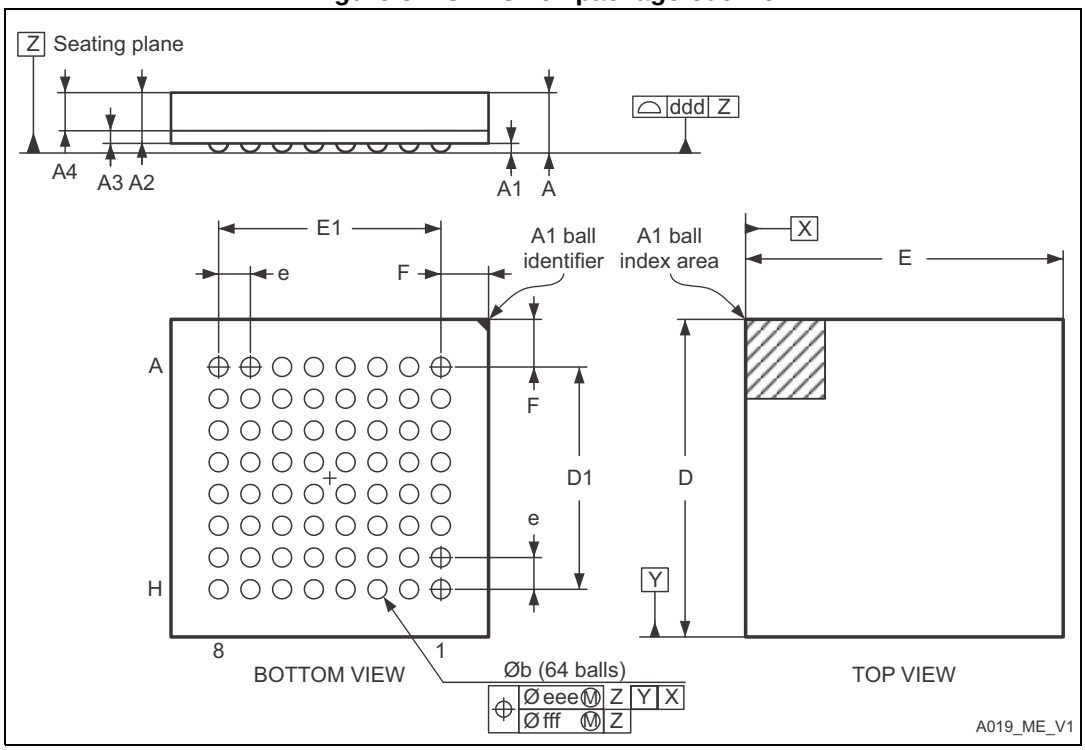
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 UFBGA64 package information

UFBGA64 is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra-fine-profile ball grid array package.

Figure 34. UFBGA64 package outline



1. Drawing is not to scale.

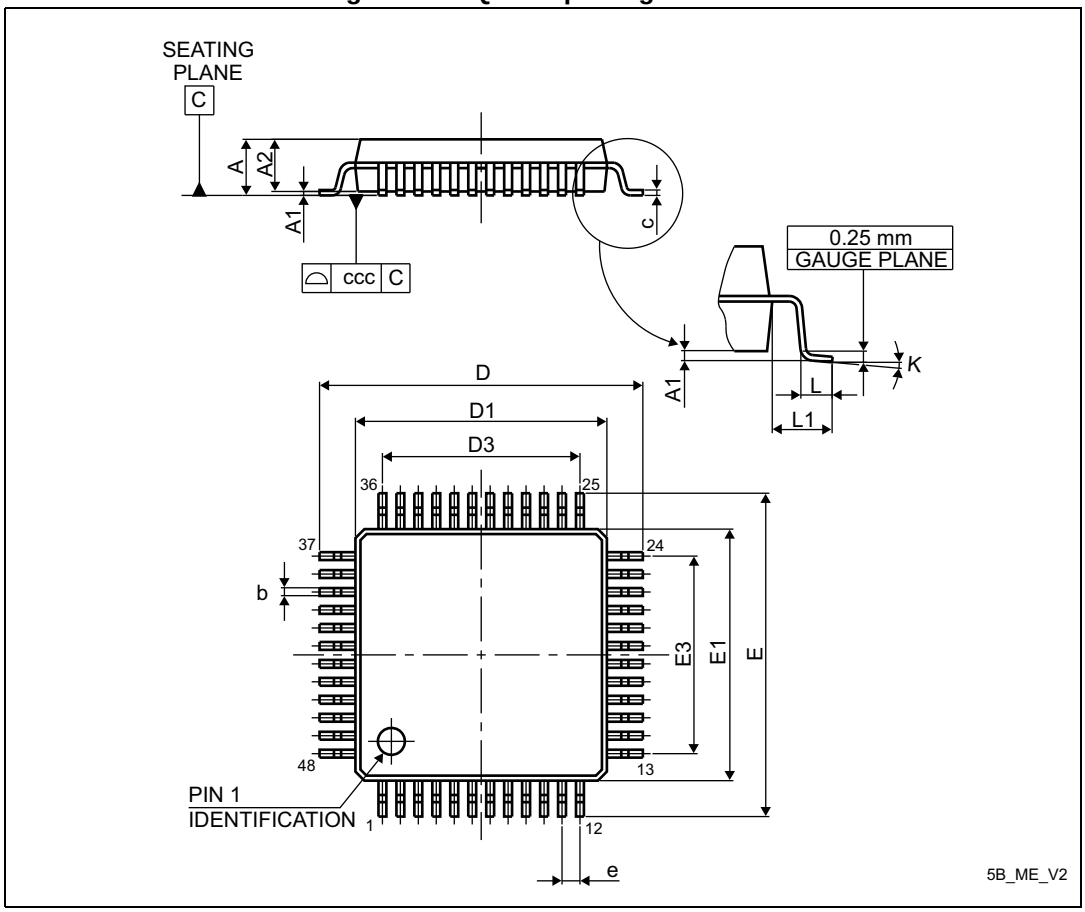
Table 65. UFBGA64 package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146

7.3 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

Figure 40. LQFP48 package outline

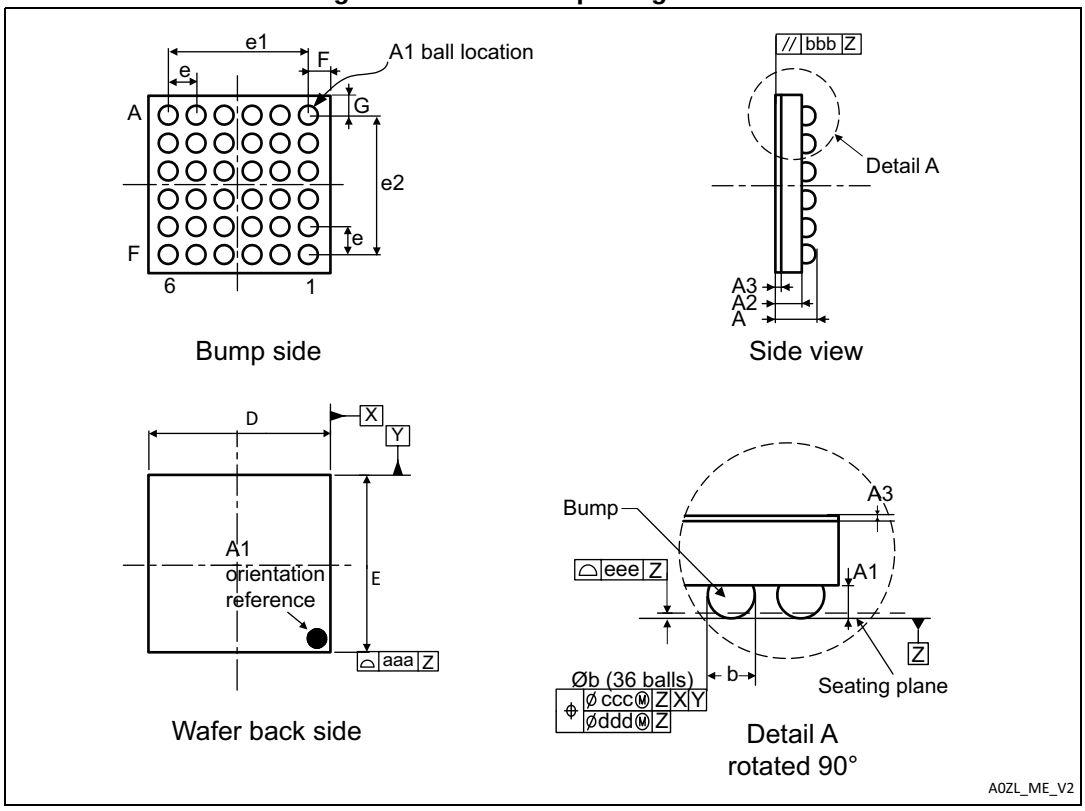


1. Drawing is not to scale.

7.5 WLCSP36 package information

WLCSP36 is a 36-ball, 2.605 x 2.703 mm, 0.4 mm pitch wafer-level chip-scale package.

Figure 46. WLCSP36 package outline



1. Drawing is not to scale.

Table 70. WLCSP36 package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3(2)	-	0.025	-	-	0.0010	-
b(3)	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.570	2.605	2.640	0.1012	0.1026	0.1039
E	2.668	2.703	2.738	0.1050	0.1064	0.1078
e	-	0.400	-	-	0.0157	-
e1	-	2.000	-	-	0.0787	-
e2	-	2.000	-	-	0.0787	-

Table 70. WLCSP36 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	-	0.3025	-	-	0.0119	-
G	-	0.3515	-	-	0.0138	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 47. Recommended pad footprint for WLCSP36 package

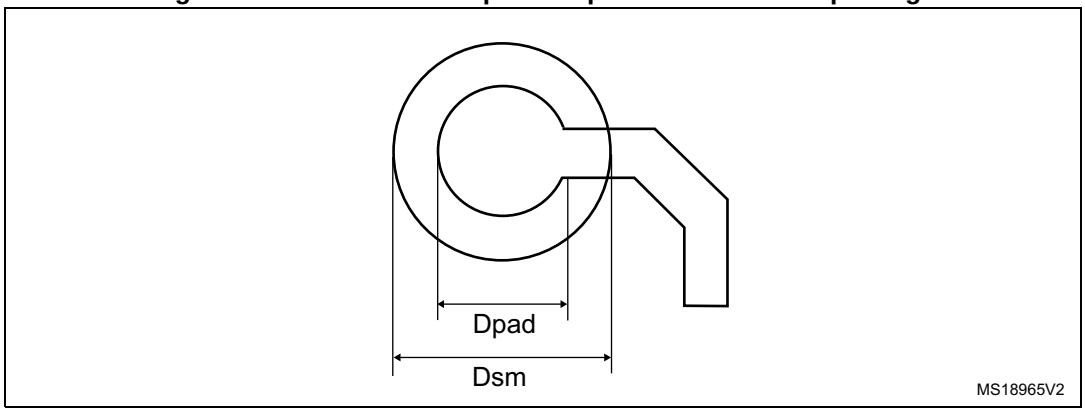


Table 71. WLCSP36 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

Table 76. Document revision history (continued)

Date	Revision	Changes
13-Jan-2014	4 (continued)	Added “Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection” in *Section Functional susceptibility to I/O current injection.* Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in *Table : ESD absolute maximum ratings*. Merged *Table: Typical and maximum VDD consumption in Stop and Standby modes* and *Table: Typical and maximum VDDA consumption in Stop and Standby modes* into *Table: Typical and maximum current consumption in Stop and Standby modes.* Updated: – *Table: Temperature sensor calibration values,* – *Table: Internal voltage reference calibration values,* – *Table: Current characteristics,* – *Table: General operating conditions,* – *Table: Typical and maximum current consumption from the VDDA supply,* – *Table: Low-power mode wakeup timings,* – *Table: I/O current injection susceptibility,* – *Table: I/O static characteristics,* – *Table: Output voltage characteristics,* – *Table: NRST pin characteristics,* – *Table: I^2C analog filter characteristics,* – *Figure: Power supply scheme,* – *Figure: TC and TTa I/O input characteristics,* – *Figure: Five volt tolerant (FT and FTf) I/O input characteristics,* – *Figure: I/O AC characteristics definition,* – *Figure: ADC accuracy characteristics,* – *Figure: Typical connection diagram using the ADC,* – *Figure: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline,* – *Figure: LQFP64 recommended footprint,* – *Figure: LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline,* – *Figure: LQFP48 recommended footprint,* – *Figure: LQFP32 – 7 x 7 mm 32-pin low-profile quad flat package outline,* – *Figure: LQFP32 recommended footprint,* – *Figure: UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package outline.*