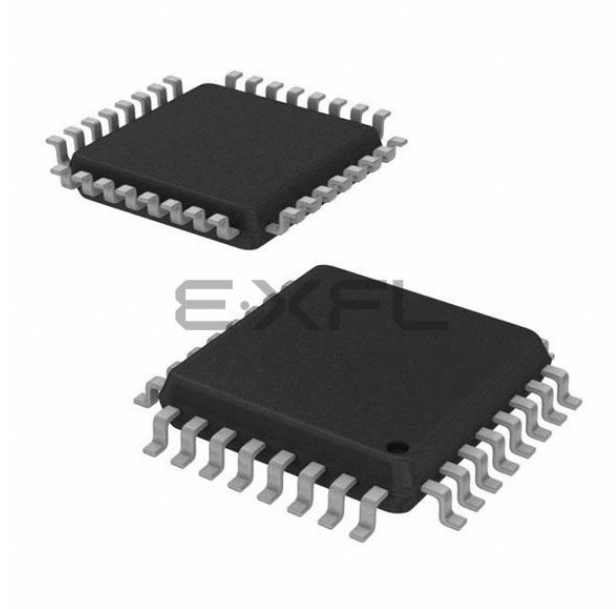


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051k6t6tr

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F051xx microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 5. Capacitive sensing GPIOs available on STM32F051xx devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	4	TSC_G4_IO1	PA9
	TSC_G1_IO2	PA1		TSC_G4_IO2	PA10
	TSC_G1_IO3	PA2		TSC_G4_IO3	PA11
	TSC_G1_IO4	PA3		TSC_G4_IO4	PA12
2	TSC_G2_IO1	PA4	5	TSC_G5_IO1	PB3
	TSC_G2_IO2	PA5		TSC_G5_IO2	PB4
	TSC_G2_IO3	PA6		TSC_G5_IO3	PB6
	TSC_G2_IO4	PA7		TSC_G5_IO4	PB7
3	TSC_G3_IO1	PC5	6	TSC_G6_IO1	PB11
	TSC_G3_IO2	PB0		TSC_G6_IO2	PB12
	TSC_G3_IO3	PB1		TSC_G6_IO3	PB13
	TSC_G3_IO4	PB2		TSC_G6_IO4	PB14

Table 6. Effective number of capacitive sensing channels on STM32F051xx

Analog I/O group	Number of capacitive sensing channels				
	STM32F051Rx	STM32F051Cx	STM32F051Tx	STM32F051KxU (UFQFPN32)	STM32F051KxT (LQFP32)
G1	3	3	3	3	3
G2	3	3	3	3	3
G3	3	2	2	2	1
G4	3	3	3	3	3
G5	3	3	3	3	3
G6	3	3	0	0	0
Number of capacitive sensing channels	18	17	14	14	13

can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I^2S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F051xx SPI/I^2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I^2S mode	X	-
TI mode	X	X

1. X = supported.

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.20 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 13. Pin definitions (continued)

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	UFBGA64	LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32					Alternate functions	Additional functions
33	H8	25	-	-	-	PB12	I/O	FT	(5)	SPI2_NSS, TIM1_BKIN, TSC_G6_IO2, EVENTOUT	-
34	G8	26	-	-	-	PB13	I/O	FT	(5)	SPI2_SCK, TIM1_CH1N, TSC_G6_IO3	-
35	F8	27	-	-	-	PB14	I/O	FT	(5)	SPI2_MISO, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	-
36	F7	28	-	-	-	PB15	I/O	FT	(5)	SPI2_MOSI, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	RTC_REFIN
37	F6	-	-	-	-	PC6	I/O	FT	-	TIM3_CH1	-
38	E7	-	-	-	-	PC7	I/O	FT	-	TIM3_CH2	-
39	E8	-	-	-	-	PC8	I/O	FT	-	TIM3_CH3	-
40	D8	-	-	-	-	PC9	I/O	FT	-	TIM3_CH4	-
41	D7	29	E2	18	18	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	C7	30	D1	19	19	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1	-
43	C6	31	C1	20	20	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2	-
44	C8	32	C2	21	21	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	-

Table 16. STM32F051xx peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme

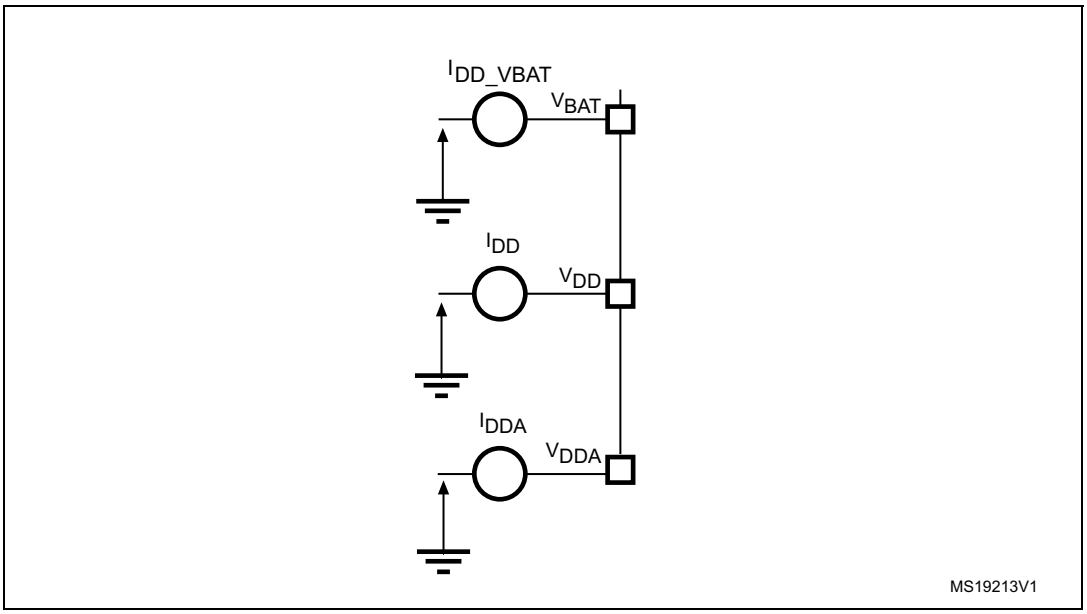


Table 25. Typical and maximum current consumption from V_{DD} at 3.6 V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Sleep mode	HSE bypass, PLL on	48 MHz	14.0	15.3(2)	15.3	16.0(2)	2.8	3.0(2)	3.0	3.2(2)	mA
			32 MHz	9.5	10.2	10.2	10.7	2.0	2.1	2.1	2.3	
			24 MHz	7.3	7.8	7.8	8.3	1.5	1.7	1.7	1.9	
		HSE bypass, PLL off	8 MHz	2.6	2.9	2.9	3.0	0.6	0.8	0.8	0.8	
			1 MHz	0.4	0.6	0.6	0.6	0.2	0.4	0.4	0.4	
		HSI clock, PLL on	48 MHz	14.0	15.3	15.3	16.0	3.8	4.0	4.1	4.2	
			32 MHz	9.5	10.2	10.2	10.7	2.6	2.7	2.8	2.8	
			24 MHz	7.3	7.8	7.8	8.3	2.0	2.1	2.1	2.1	
		HSI clock, PLL off	8 MHz	2.6	2.9	2.9	3.0	0.6	0.8	0.8	0.8	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 26. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSE bypass, PLL on	48 MHz	150	170(3)	178	182(3)	164	183(3)	195	198(3)	µA
			32 MHz	104	121	126	128	113	129	135	138	
			24 MHz	82	96	100	103	88	102	106	108	
		HSE bypass, PLL off	8 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
			1 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
		HSI clock, PLL on	48 MHz	220	240	248	252	244	263	275	278	
			32 MHz	174	191	196	198	193	209	215	218	
			24 MHz	152	167	173	174	168	183	190	192	
		HSI clock, PLL off	8 MHz	72	79	82	83	83.5	91	94	95	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent of clock frequencies.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 27. Typical and maximum current consumption in Stop and Standby modes

Sym-bol	Para-meter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF		15	15.1	15.3	15.5	15.7	16	(2)		(2)	µA
		Regulator in low-power mode, all oscillators OFF		3.2	3.3	3.4	3.5	3.7	4	(2)		(2)	
	Supply current in Standby mode	LSI ON and IWDG ON		0.8	1.0	1.1	1.2	1.4	1.5	-	-	-	
		LSI OFF and IWDG OFF		0.7	0.8	0.9	1.0	1.1	1.3	2(2)	2.5	3(2)	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.9	2	2.2	2.3	2.5	2.6	3.5(2)	3.5	4.5(2)	
			Regulator in low-power mode, all oscillators OFF	1.9	2	2.2	2.3	2.5	2.6	3.5(2)	3.5	4.5(2)	
	Supply current in Standby mode		LSI ON and IWDG ON	2.3	2.5	2.7	2.9	3.1	3.3	-	-	-	
			LSI OFF and IWDG OFF	1.8	1.9	2	2.2	2.3	2.5	3.5(2)	3.5	4.5(2)	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.1	1.2	1.2	1.2	1.3	1.4	-	-	-	
			Regulator in low-power mode, all oscillators OFF	1.1	1.2	1.2	1.2	1.3	1.4	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.5	1.6	1.7	1.8	1.9	2.0	-	-	-	
			LSI OFF and IWDG OFF	1	1.0	1.1	1.1	1.2	1.2	-	-	-	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

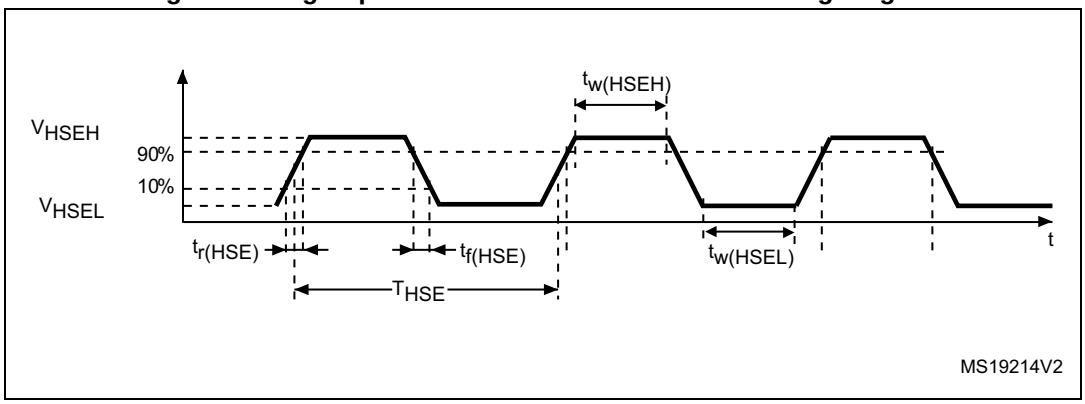
Table 30. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DDIOx} = 3.3 V C =C_{INT}	4 MHz	0.07	mA
			8 MHz	0.15	
			16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
		V_{DDIOx} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.18	
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V_{DDIOx} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.32	
			8 MHz	0.64	
			16 MHz	1.25	
			24 MHz	2.23	
			48 MHz	4.442	
		V_{DDIOx} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V_{DDIOx} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.64	
			8 MHz	1.25	
			16 MHz	3.24	
			24 MHz	5.02	
		V_{DDIOx} = 3.3 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	
		V_{DDIOx} = 2.4 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.66	
			8 MHz	1.43	
			16 MHz	2.45	
			24 MHz	4.97	

1. C_S = 7 pF (estimated value).

1. Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

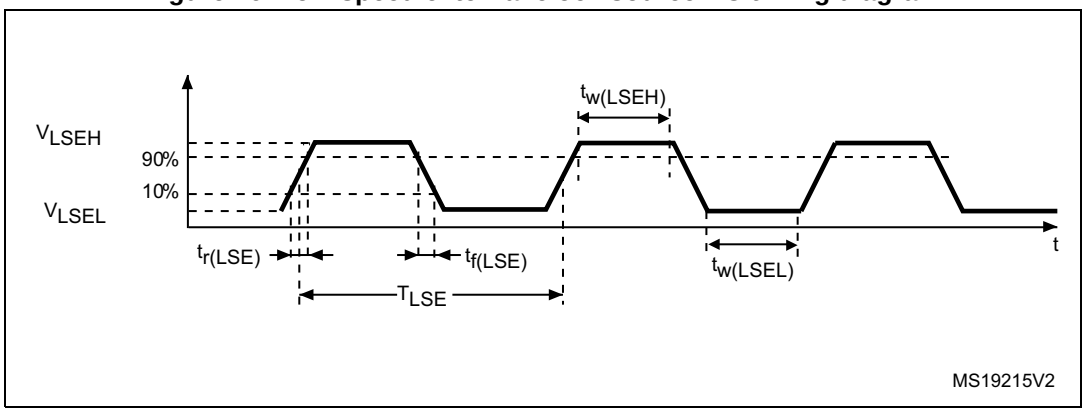
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 16*.

Table 34. Low-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

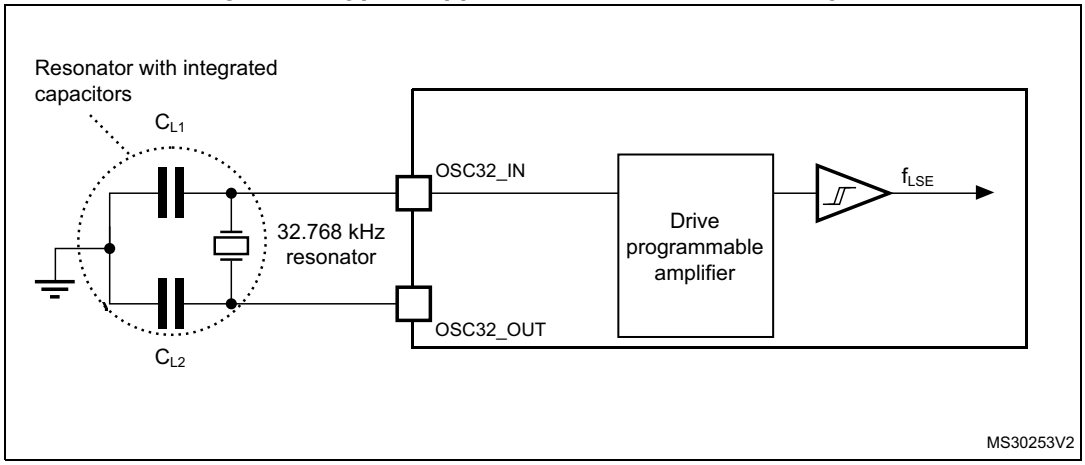
1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram



Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. The provided curves are characterization results, not tested in production.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 17: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 17: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 49. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}–1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 6 mA	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OLFm+}(3)	Output low level voltage for an FTf I/O pin in Fm+ mode	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
		$\|I_{IO}\|$ = 10 mA	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 17: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.

Table 62. I²C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 63* for SPI or in *Table 64* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 20: General operating conditions*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 63. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

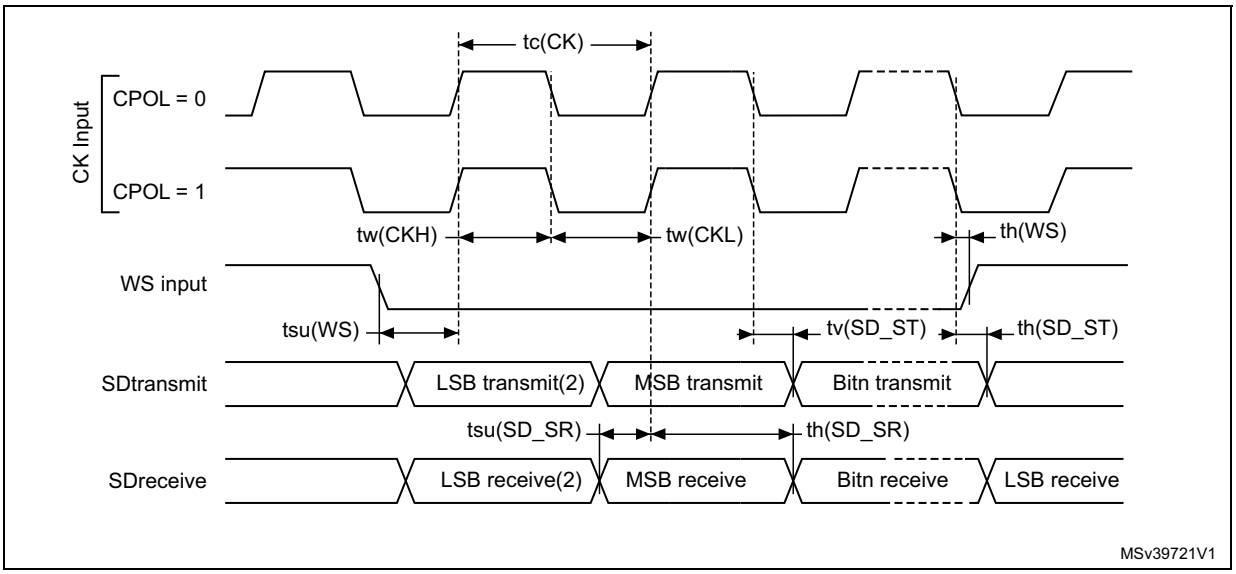
1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Table 64. I^2S characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$(2)	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$(2)		Slave receiver	0.5	-	
$t_{v(SD\_MT)}$(2)	Data output valid time	Master transmitter	-	4	
$t_{v(SD\_ST)}$(2)		Slave transmitter	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter	0	-	
$t_{h(SD\_ST)}$		Slave transmitter	13	-	

1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then T_{PCLK} = 1/f_{PLCLK} = 125 ns.

Figure 32. I^2S slave timing diagram (Philips protocol)



1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

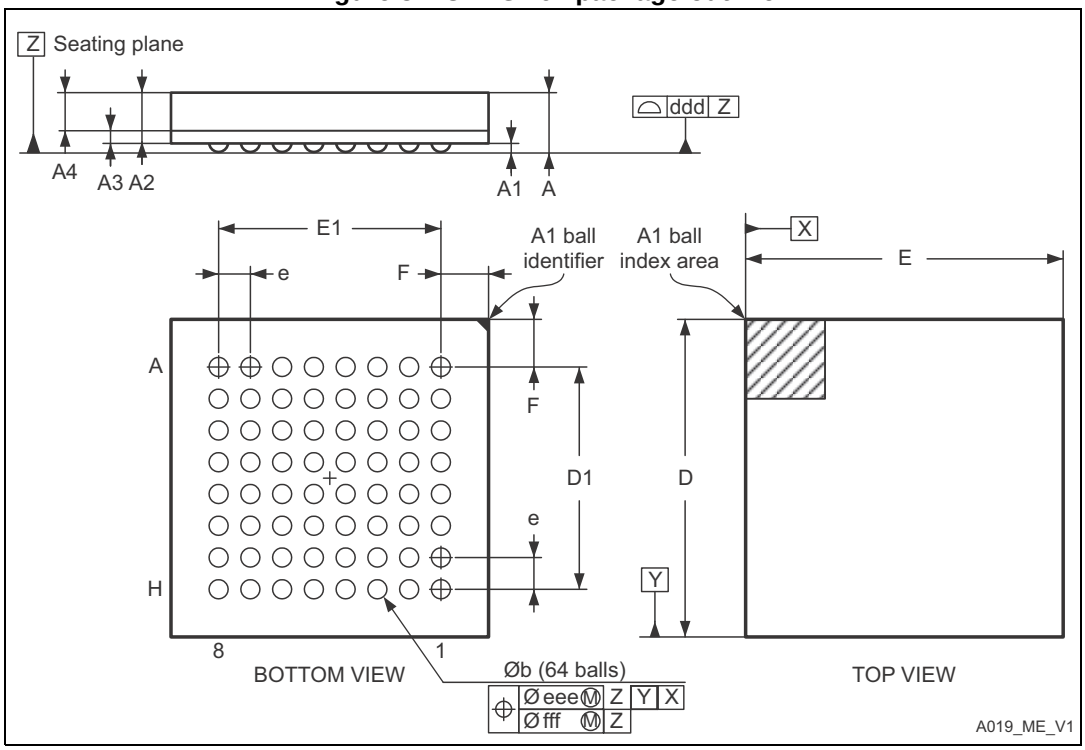
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 UFBGA64 package information

UFBGA64 is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra-fine-profile ball grid array package.

Figure 34. UFBGA64 package outline



1. Drawing is not to scale.

Table 65. UFBGA64 package mechanical data

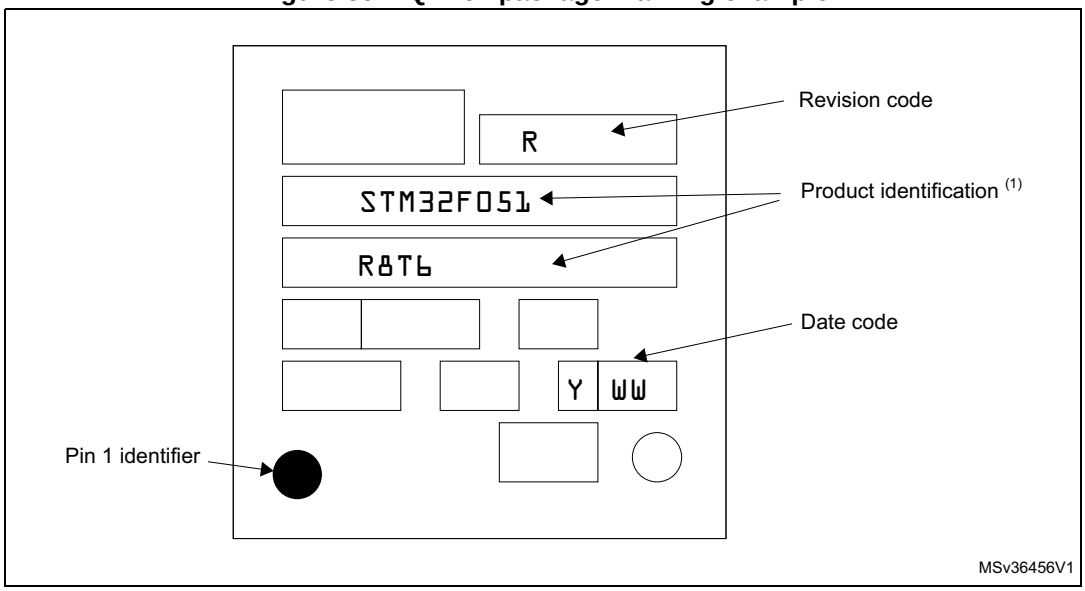
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 39. LQFP64 package marking example

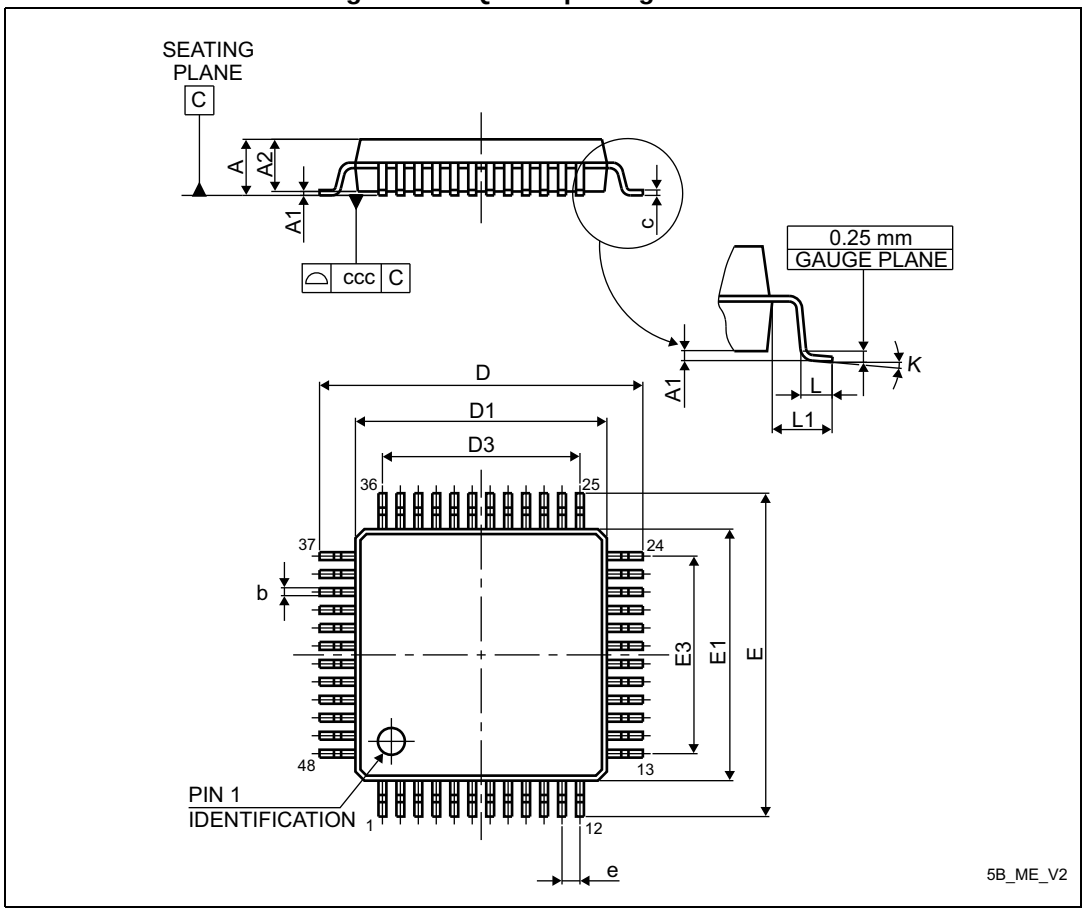


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

Figure 40. LQFP48 package outline



1. Drawing is not to scale.

Table 76. Document revision history (continued)

Date	Revision	Changes
13-Jan-2014	4 (continued)	Added “Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection” in *Section Functional susceptibility to I/O current injection.* Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in *Table : ESD absolute maximum ratings*. Merged *Table: Typical and maximum VDD consumption in Stop and Standby modes* and *Table: Typical and maximum VDDA consumption in Stop and Standby modes* into *Table: Typical and maximum current consumption in Stop and Standby modes.* Updated: – *Table: Temperature sensor calibration values,* – *Table: Internal voltage reference calibration values,* – *Table: Current characteristics,* – *Table: General operating conditions,* – *Table: Typical and maximum current consumption from the VDDA supply,* – *Table: Low-power mode wakeup timings,* – *Table: I/O current injection susceptibility,* – *Table: I/O static characteristics,* – *Table: Output voltage characteristics,* – *Table: NRST pin characteristics,* – *Table: I^2C analog filter characteristics,* – *Figure: Power supply scheme,* – *Figure: TC and TTa I/O input characteristics,* – *Figure: Five volt tolerant (FT and FTf) I/O input characteristics,* – *Figure: I/O AC characteristics definition,* – *Figure: ADC accuracy characteristics,* – *Figure: Typical connection diagram using the ADC,* – *Figure: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline,* – *Figure: LQFP64 recommended footprint,* – *Figure: LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline,* – *Figure: LQFP48 recommended footprint,* – *Figure: LQFP32 – 7 x 7 mm 32-pin low-profile quad flat package outline,* – *Figure: LQFP32 recommended footprint,* – *Figure: UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package outline.*

Table 76. Document revision history (continued)

Date	Revision	Changes
28-Aug-2015	5	Updated the following: – DAC and power management feature descriptions in *Features* – *Table 2: STM32F051xx family device features and peripheral count* – *Section 3.5.1: Power supply schemes* – *Figure 13: Power supply scheme* – *Table 17: Voltage characteristics* – *Table 20: General operating conditions:* updated the footnote for V_{IN} parameter – *Table 28: Typical and maximum current consumption from the V_{BAT} supply* – *Table 52: ADC characteristics* – *Table 33: High-speed external user clock characteristics*: replaced V_{DD} with V_{DDIOX} – *Table 34: Low-speed external user clock characteristics*: replaced V_{DD} with V_{DDIOX} – *Table 37: HSI oscillator characteristics* and *Figure 19: HSI oscillator accuracy characterization results for soldered parts* – *Table 38: HSI14 oscillator characteristics*: changed the min value for ACC_{HSI14} – *Table 41: Flash memory characteristics*: changed the values for t_{ME} and I_{DD} in write mode – *Table 43: EMS characteristics*: changed the value of V_{EFTB} – *Table 45: ESD absolute maximum ratings* – *Figure 10: STM32F051x8 memory map* – *Figure 21: TC and TTa I/O input characteristics* – *Figure 22: Five volt tolerant (FT and FTf) I/O input characteristics* – *Figure 23: I/O AC characteristics definition* – t_{START} definition in *Table 24: Embedded internal reference voltage* – t_{STAB} characteristics in *Table 52: ADC characteristics* – *Table 56: Comparator characteristics*: changed the description and values for V_{SC}, V_{DDA} and V_{REFINT} parameters. Added *Figure 28: Maximum V_{REFINT} scaler startup time from power down* – *Table 57: TS characteristics:* changed the min value for $T_{S\text{-}temp}$ – *Table 58: V_{BAT} monitoring characteristics:* changed the min value for $T_{S\text{-}vbat}$ and the typical value for R parameters – *Section 6.3.22: Communication interfaces:* updated the description and features in the subsection I^2C interface characteristics – *Table 64: I^2S characteristics:* updated the min values for data input hold time (master and slave receiver)