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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051k6u6

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In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F051xx microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1,, COMPx or the CEC.

The CEC, USART1 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14), DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 55 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 3 internal (temperature

sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = 3.3$ V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{DDA} = 3.3$ V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = 3.3$ V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

4 Pinouts and pin descriptions

Figure 3. LQFP64 package pinout

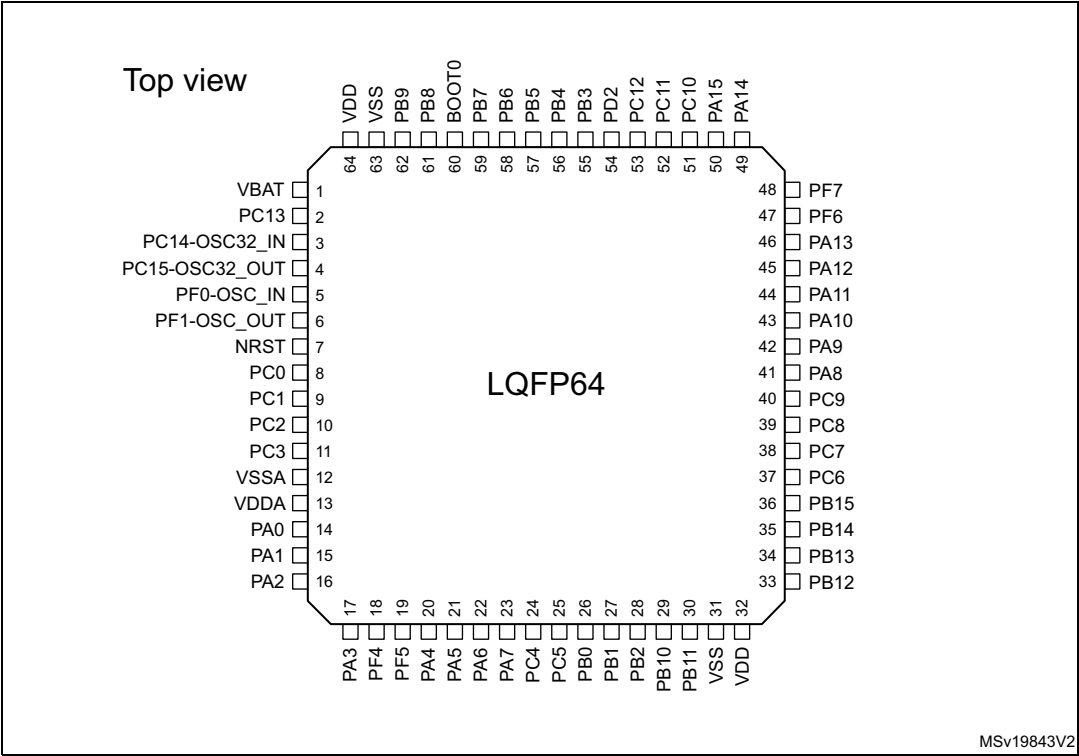
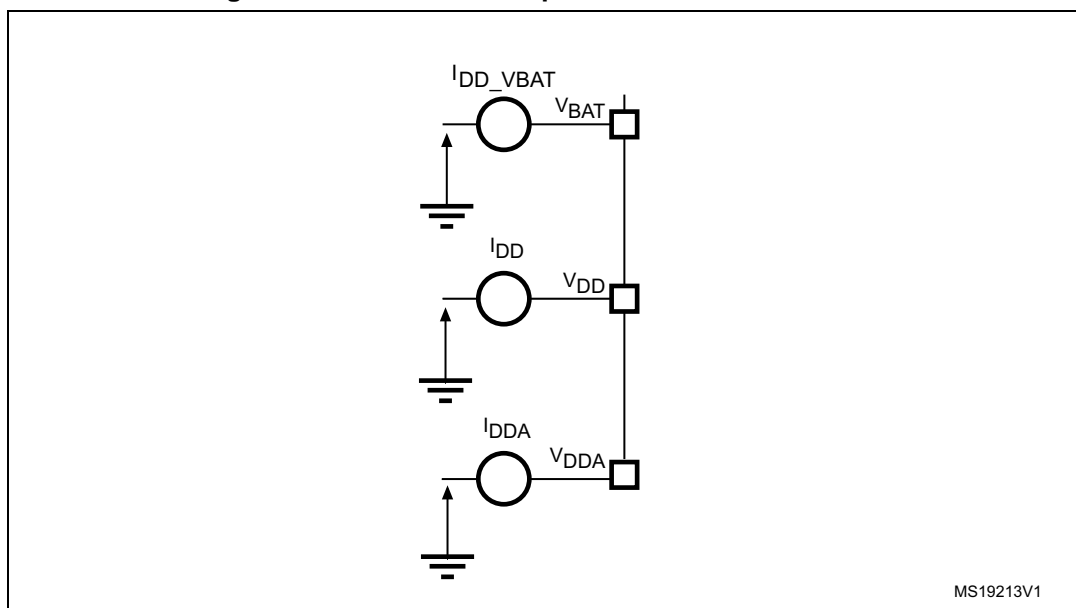


Table 13. Pin definitions (continued)

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	UFBGA64	LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32					Alternate functions	Additional functions
22	G4	16	E3	12	12	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT	ADC_IN6
23	H4	17	F4	13	13	PA7	I/O	TTa	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
24	H5	-	-	-	-	PC4	I/O	TTa	-	EVENTOUT	ADC_IN14
25	H6	-	-	-	-	PC5	I/O	TTa	-	TSC_G3_IO1	ADC_IN15
26	F5	18	F3	14	14	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	ADC_IN8
27	G5	19	F2	15	15	PB1	I/O	TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
28	G6	20	D2	-	16	PB2	I/O	FT	(4)	TSC_G3_IO4	-
29	G7	21	-	-	-	PB10	I/O	FT	(5)	I2C2_SCL, CEC, TIM2_CH3, TSC_SYNC	-
30	H7	22	-	-	-	PB11	I/O	FT	(5)	I2C2_SDA, TIM2_CH4, TSC_G6_IO1, EVENTOUT	-
31	D4	23	F1	16	0	VSS	S	-	-	Ground	
32	E4	24	E1	17	17	VDD	S	-	-	Digital power supply	

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 17: Voltage characteristics](#), [Table 18: Current characteristics](#) and [Table 19: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 17. Voltage characteristics⁽¹⁾

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage	- 0.3	4.0	V
$V_{DDA}-V_{SS}$	External analog supply voltage	- 0.3	4.0	V
$V_{DD}-V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
$V_{BAT}-V_{SS}$	External backup supply voltage	- 0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	$V_{DDIOx} + 4.0^{(3)}$	V
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	V
	BOOT0	0	9.0	V
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	V
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.12: Electrical sensitivity characteristics		-

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 18: Current characteristics](#) for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 23. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}^{(1)}$	PVD hysteresis	-	-	100	-	mV
$I_{DD(PVD)}$	PVD current consumption	-	-	0.15	0.26 ⁽¹⁾	μA

1. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in [Table 24](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 24. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10 ⁽¹⁾	μs
$t_{S_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4 ⁽¹⁾	-	-	μs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DDA} = 3\text{ V}$	-	-	10 ⁽¹⁾	mV
T_{Coeff}	Temperature coefficient	-	- 100 ⁽¹⁾	-	100 ⁽¹⁾	ppm/°C

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 14: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 29. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal

Symbol	Parameter	f _{HCLK}	Typical consumption in Run mode		Typical consumption in Sleep mode		Unit
			Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	
I _{DD}	Current consumption from V _{DD} supply	48 MHz	23.2	13.3	13.2	3.1	mA
		36 MHz	17.6	10.3	10.1	2.6	
		32 MHz	15.6	9.3	9.0	2.4	
		24 MHz	12.1	7.4	7.0	2.0	
		16 MHz	8.4	5.1	5.0	1.6	
		8 MHz	4.5	3.0	2.8	1.1	
		4 MHz	2.8	2.0	2.0	1.1	
		2 MHz	1.9	1.5	1.5	1.0	
		1 MHz	1.5	1.3	1.3	1.0	
		500 kHz	1.2	1.2	1.1	1.0	
I _{DDA}	Current consumption from V _{DDA} supply	48 MHz	151				μA
		36 MHz	113				
		32 MHz	101				
		24 MHz	79				
		16 MHz	57				
		8 MHz	2.2				
		4 MHz	2.2				
		2 MHz	2.2				
		1 MHz	2.2				
		500 kHz	2.2				

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 48: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 35](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 35. HSE oscillator characteristics

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Typ	Max ⁽²⁾	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	k Ω
I_{DD}	HSE current consumption	During startup ⁽³⁾	-	-	8.5	mA
		$V_{DD} = 3.3\text{ V}$, $R_m = 30\ \Omega$, $CL = 10\text{ pF}@8\text{ MHz}$	-	0.4	-	
		$V_{DD} = 3.3\text{ V}$, $R_m = 45\ \Omega$, $CL = 10\text{ pF}@8\text{ MHz}$	-	0.5	-	
		$V_{DD} = 3.3\text{ V}$, $R_m = 30\ \Omega$, $CL = 5\text{ pF}@32\text{ MHz}$	-	0.8	-	
		$V_{DD} = 3.3\text{ V}$, $R_m = 30\ \Omega$, $CL = 10\text{ pF}@32\text{ MHz}$	-	1	-	
		$V_{DD} = 3.3\text{ V}$, $R_m = 30\ \Omega$, $CL = 20\text{ pF}@32\text{ MHz}$	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 17](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Table 42. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
N _{END}	Endurance	T _A = -40 to +105 °C	10	kcycle
t _{RET}	Data retention	1 kcycle ⁽²⁾ at T _A = 85 °C	30	Year
		1 kcycle ⁽²⁾ at T _A = 105 °C	10	
		10 kcycle ⁽²⁾ at T _A = 55 °C	20	

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 43](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 43. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V _{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V _{DD} = 3.3 V, LQFP64, T _A = +25 °C, f _{HCLK} = 48 MHz, conforming to IEC 61000-4-2	2B
V _{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V _{DD} and V _{SS} pins to induce a functional disturbance	V _{DD} = 3.3 V, LQFP64, T _A = +25 °C, f _{HCLK} = 48 MHz, conforming to IEC 61000-4-4	4B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Table 45. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value ⁽¹⁾	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25\text{ }^{\circ}\text{C}$, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = +25\text{ }^{\circ}\text{C}$, conforming to ANSI/ESD STM5.3.1	All	C3	250	V

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 46. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105\text{ }^{\circ}\text{C}$ conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the $-5\text{ }\mu\text{A}/+0\text{ }\mu\text{A}$ range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in [Table 47](#).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 47. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on PA10, PA12, PB4, PB5, PB10, PB15 and PD2 pins with induced leakage current on adjacent pins less than –10 μ A	–5	NA	
	Injected current on all other FT and FTf pins	–5	NA	
	Injected current on PA6 and PC0	–0	+5	
	Injected current on all other TTa, TC and RST pins	–5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 48](#) are derived from tests performed under the conditions summarized in [Table 20: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 48. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3 V_{DDIOx} + 0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475 V_{DDIOx} - 0.2^{(1)}$	
		BOOT0	-	-	$0.3 V_{DDIOx} - 0.3^{(1)}$	
		All I/Os except BOOT0 pin	-	-	$0.3 V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445 V_{DDIOx} + 0.398^{(1)}$	-	-	V
		FT and FTf I/O	$0.5 V_{DDIOx} + 0.2^{(1)}$	-	-	
		BOOT0	$0.2 V_{DDIOx} + 0.95^{(1)}$	-	-	
		All I/Os except BOOT0 pin	$0.7 V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(1)}$	-	mV
		FT and FTf I/O	-	$100^{(1)}$	-	
		BOOT0	-	$300^{(1)}$	-	

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 23](#) and [Table 50](#), respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 50. I/O AC characteristics⁽¹⁾⁽²⁾

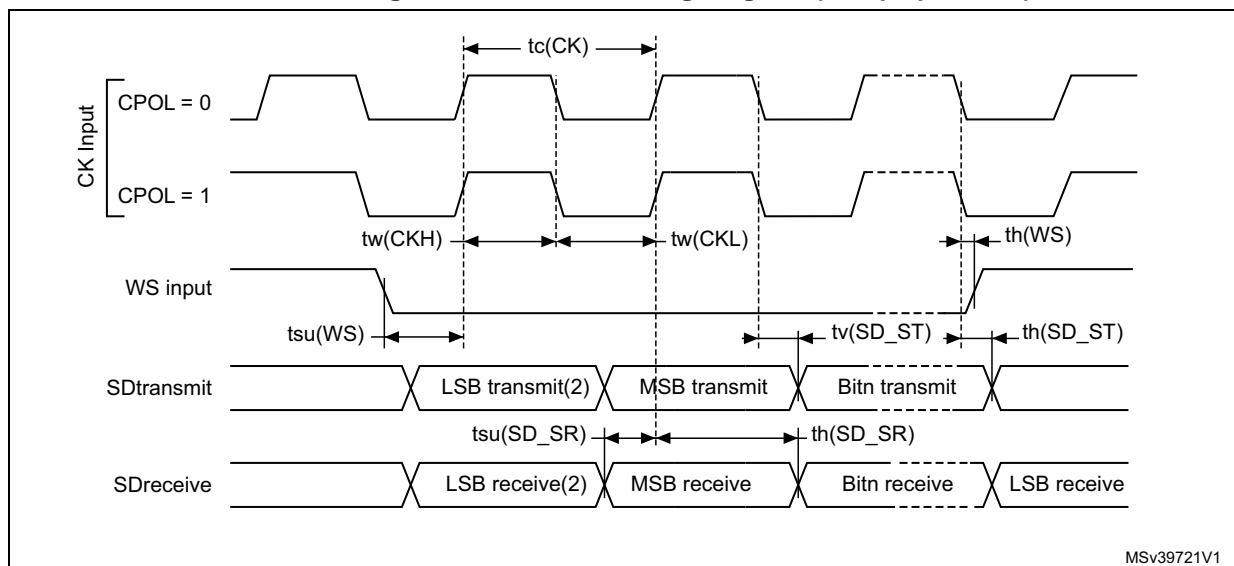
OSPEEDRx [1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$	-	2	MHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	125	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	125	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$	-	10	MHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	25	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	25	
11	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 30 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	50	MHz
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	30	
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2.7 \text{ V}$	-	20	
	$t_{f(\text{IO})\text{out}}$	Output fall time	$C_L = 30 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	5	ns
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	8	
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2.7 \text{ V}$	-	12	
	$t_{r(\text{IO})\text{out}}$	Output rise time	$C_L = 30 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	5	
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	8	
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2.7 \text{ V}$	-	12	
Fm+ configuration ⁽⁴⁾	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$	-	2	MHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	12	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	34	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in [Figure 23](#).
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

Table 64. I²S characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD_SR)}$		Slave receiver	2	-	
$t_{h(SD_MR)}^{(2)}$	Data input hold time	Master receiver	4	-	
$t_{h(SD_SR)}^{(2)}$		Slave receiver	0.5	-	
$t_{v(SD_MT)}^{(2)}$	Data output valid time	Master transmitter	-	4	
$t_{v(SD_ST)}^{(2)}$		Slave transmitter	-	20	
$t_{h(SD_MT)}$	Data output hold time	Master transmitter	0	-	
$t_{h(SD_ST)}$		Slave transmitter	13	-	

1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK} . For example, if $f_{PCLK} = 8$ MHz, then $T_{PCLK} = 1/f_{PCLK} = 125$ ns.

Figure 32. I²S slave timing diagram (Philips protocol)

1. Measurement points are done at CMOS levels: $0.3 \times V_{DDIOx}$ and $0.7 \times V_{DDIOx}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 65. UFBGA64 package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. Recommended footprint for UFBGA64 package

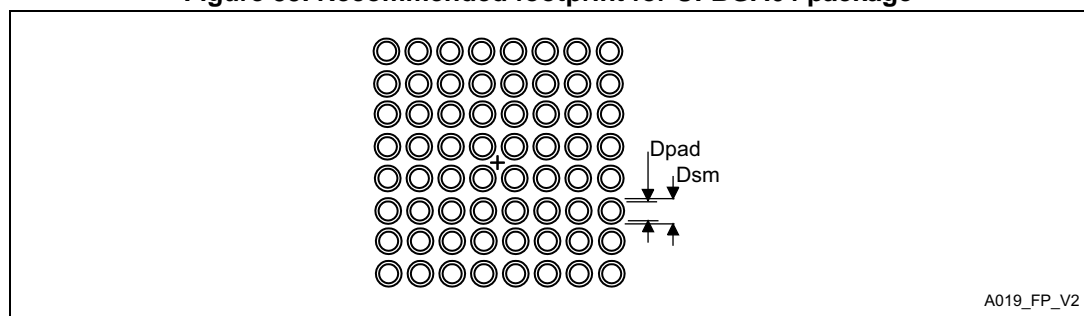


Table 66. UFBGA64 recommended PCB design rules

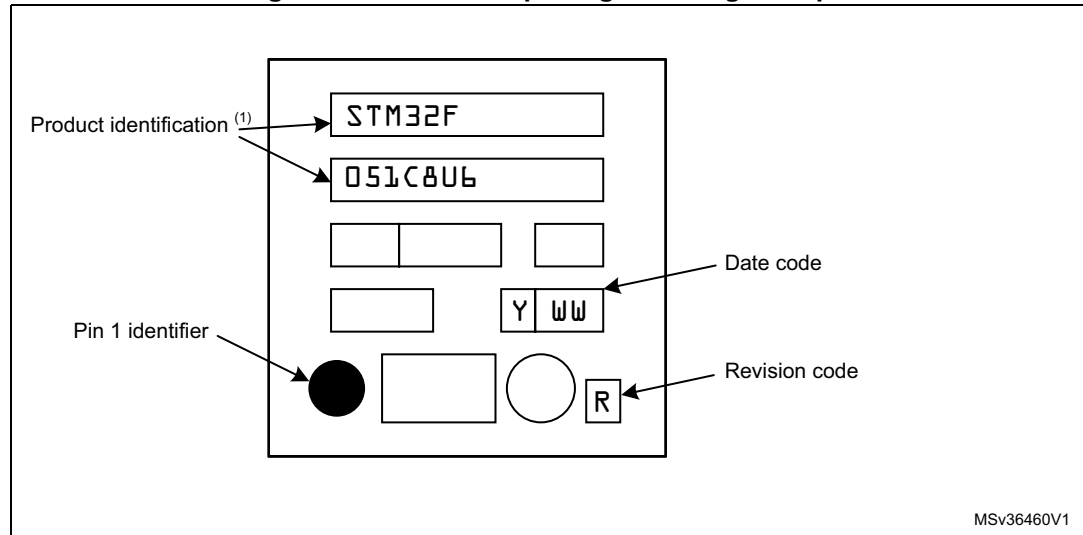
Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 45. UFQFPN48 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F051xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives: $P_{INTmax} = 175\text{ mW}$ and $P_{IOmax} = 272\text{ mW}$:

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Using the values obtained in [Table 74](#) T_{Jmax} is calculated as follows:

– For LQFP64, $45\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 82\text{ }^{\circ}\text{C} + (45\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 82\text{ }^{\circ}\text{C} + 20.115\text{ }^{\circ}\text{C} = 102.115\text{ }^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$) see [Table 20: General operating conditions](#).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Section 8: Ordering information](#)).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

$$\text{Suffix 6: } T_{Amax} = T_{Jmax} - (45\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 105 - 20.115 = 84.885\text{ }^{\circ}\text{C}$$

$$\text{Suffix 7: } T_{Amax} = T_{Jmax} - (45\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 125 - 20.115 = 104.885\text{ }^{\circ}\text{C}$$

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 100\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives: $P_{INTmax} = 70\text{ mW}$ and $P_{IOmax} = 64\text{ mW}$:

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus: $P_{Dmax} = 134\text{ mW}$