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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051k6u6tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 1. Block diagram

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In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F051xx microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1,, COMPx or the CEC.

The CEC, USART1 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

• Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.



Functional overview



Figure 2. Clock tree

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

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can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision



4 Pinouts and pin descriptions









Figure 6. UFQFPN48 package pinout

Figure 7. WLCSP36 package pinout



1. The above figure shows the package in top view, changing from bottom view in the previous document versions.



	P	Pin nu	umbe	er						Pin functions		
LQFP64	UFBGA64	LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions	
33	H8	25	-	-	-	PB12	I/O	FT	(5)	SPI2_NSS, TIM1_BKIN, TSC_G6_IO2, EVENTOUT	-	
34	G8	26	-	-	-	PB13	I/O	FT	(5)	SPI2_SCK, TIM1_CH1N, TSC_G6_IO3	-	
35	F8	27	-	-	-	PB14	I/O	FT	(5)	SPI2_MISO, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	-	
36	F7	28	-	-	-	PB15	I/O	FT	(5)	SPI2_MOSI, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	RTC_REFIN	
37	F6	-	-	-	-	PC6	I/O	FT	-	TIM3_CH1	-	
38	E7	-	-	-	-	PC7	I/O	FT	-	TIM3_CH2	-	
39	E8	-	-	-	-	PC8	I/O	FT	-	TIM3_CH3	-	
40	D8	-	-	-	-	PC9	I/O	FT	-	TIM3_CH4	-	
41	D7	29	E2	18	18	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-	
42	C7	30	D1	19	19	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1	-	
43	C6	31	C1	20	20	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2	-	
44	C8	32	C2	21	21	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	-	

Table 13. Pin definitions (continued)



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 31*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 17: Voltage characteristics*

	Peripheral	Typical consumption at 25 °C	Unit
	BusMatrix ⁽¹⁾	5	
	DMA1	7	
	SRAM	1	
	Flash memory interface	14	
	CRC	2	
	GPIOA	9	
АПБ	GPIOB	12	μΑνινιτίΖ
	GPIOC	2	
	GPIOD	1	
	GPIOF	1	
	TSC	6	
	All AHB peripherals	55	

Table 31. Peripheral current consumption



High-speed internal (HSI) RC oscillator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit		
f _{HSI}	Frequency	-	-	8	-	MHz		
TRIM	HSI user trimming step	-	-	-	1 ⁽²⁾	%		
DuCy _(HSI)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%		
		T _A = -40 to 105°C	-2.8 ⁽³⁾	-	3.8 ⁽³⁾			
	Accuracy of the HSI oscillator	T _A = -10 to 85°C	-1.9 ⁽³⁾	-	2.3 ⁽³⁾	0/		
		$T_A = 0$ to $85^{\circ}C$	-1.9 ⁽³⁾	-	2 ⁽³⁾			
ACCHSI		$T_A = 0$ to $70^{\circ}C$	-1.3 ⁽³⁾	-	2 ⁽³⁾	70		
		$T_A = 0$ to 55°C	-1 ⁽³⁾	-	2 ⁽³⁾			
		$T_A = 25^{\circ}C^{(4)}$	-1	-	1			
t _{su(HSI)}	HSI oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs		
I _{DDA(HSI)}	HSI oscillator power consumption	-	-	80	100 ⁽²⁾	μA		

Table 37. HSI oscillator characteristics⁽¹⁾

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.

2. Guaranteed by design, not tested in production.

3. Data based on characterization results, not tested in production.

4. Factory calibrated, parts not soldered.



Figure 19. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 39. LS	l oscillator	characteristics ⁽¹⁾
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Symbol	Parameter	Min	Тур	Max	Unit
f _{LSI}	Frequency	30	40	50	kHz
t _{su(LSI)} ⁽²⁾	LSI oscillator startup time	-	-	85	μs
I _{DDA(LSI)} ⁽²⁾	LSI oscillator power consumption	-	0.75	1.2	μÂ

1. V_{DDA} = 3.3 V, T_A = –40 to 105 $^\circ\text{C}$ unless otherwise specified.

2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Symbol	Parameter		Unit		
Symbol	Faiameter	Min	Тур	Max	Unit
£	PLL input clock ⁽¹⁾	1 ⁽²⁾	8.0	24 ⁽²⁾	MHz
'PLL_IN	PLL input clock duty cycle	40 ⁽²⁾	-	60 ⁽²⁾	%
f _{PLL_OUT}	PLL multiplier output clock	16 ⁽²⁾	-	48	MHz
t _{LOCK}	PLL lock time	-	-	200 ⁽²⁾	μs
Jitter _{PLL}	Cycle-to-cycle jitter	_	_	300 ⁽²⁾	ps

Table 40. PLL characteristics

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.

2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

Table 41. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
t _{prog}	16-bit programming time	T _A = - 40 to +105 °C	40	53.5	60	μs
t _{ERASE}	Page (1 KB) erase time	T _A = - 40 to +105 °C	20	-	40	ms
t _{ME}	Mass erase time	T _A = - 40 to +105 °C	20	-	40	ms
I _{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.



Symbol	Description	Func suscer	Unit	
	Description	Negative injection	Positive injection	Unit
	Injected current on BOOT0	-0	NA	
linu	Injected current on PA10, PA12, PB4, PB5, PB10, PB15 and PD2 pins with induced leakage current on adjacent pins less than $-10 \ \mu A$	-5	NA	mA
·IINJ	Injected current on all other FT and FTf pins	-5	NA	
	Injected current on PA6 and PC0	-0	+5	
	Injected current on all other TTa, TC and RST pins	-5	+5	

Table 47. I/O	current inj	jection susc	eptibility
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6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 20: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		TC and TTa I/O	-	-	0.3 V _{DDIOx} +0.07 ⁽¹⁾	
		FT and FTf I/O	-	-	0.475 V _{DDIOx} -0.2 ⁽¹⁾	
V _{IL}	voltage	BOOT0	-	-	0.3 V _{DDIOx} -0.3 ⁽¹⁾	V
		All I/Os except BOOT0 pin	-	-	0.3 V _{DDIOx}	
	High level input voltage	TC and TTa I/O	0.445 V _{DDIOx} +0.398 ⁽¹⁾	-	-	
		FT and FTf I/O	0.5 V _{DDIOx} +0.2 ⁽¹⁾	-	-	
V _{IH}		BOOT0	0.2 V _{DDIOx} +0.95 ⁽¹⁾	-	-	V
		All I/Os except BOOT0 pin	0.7 V _{DDIOx}	-	-	
		TC and TTa I/O	-	200 ⁽¹⁾	-	
V _{hys}	Schmitt trigger hysteresis	FT and FTf I/O	-	100 ⁽¹⁾	-	mV
	11931010313	BOOT0	-	300 ⁽¹⁾	-	

Table 48. I/O static characteristics



Figure 24. Recommended NRST pin protection

1. The external capacitor protects the device against parasitic resets.

 The user must ensure that the level on the NRST pin can go below the V_{IL(NRST)} max level specified in Table 51: NRST pin characteristics. Otherwise the reset will not be taken into account by the device.

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the conditions summarized in *Table 20: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
I _{DDA (ADC)}	Current consumption of the $ADC^{(1)}$	V _{DDA} = 3.3 V	-	0.9	-	mA
f _{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f _S ⁽²⁾	Sampling rate	12-bit resolution	0.043	-	1	MHz
f _{TRIG} ⁽²⁾	External trigger frequency	f _{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	1/f _{ADC}
V _{AIN}	Conversion voltage range	-	0	-	V _{DDA}	V
R _{AIN} ⁽²⁾	External input impedance	See <i>Equation 1</i> and <i>Table 53</i> for details	-	-	50	kΩ
R _{ADC} ⁽²⁾	Sampling switch resistance	-	-	-	1	kΩ
C _{ADC} ⁽²⁾	Internal sample and hold capacitor	-	-	-	8	pF
+ (2)(3)	Calibration time	f _{ADC} = 14 MHz		5.9		μs
t _{CAL} ⁽²⁾⁽³⁾		-		83		1/f _{ADC}

Table 52. ADC characteristics



T _s (cycles)	t _S (μs)	R _{AIN} max (kΩ) ⁽¹⁾
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

Table 53. R_{AIN} max for f_{ADC} = 14 MHz (continued)

1. Guaranteed by design, not tested in production.

Symbol	Parameter	Test conditions	Тур	Max ⁽⁴⁾	Unit
ET	Total unadjusted error		±1.3	±2	
EO	Offset error	f _{PCLK} = 48 MHz,	±1	±1.5	
EG	Gain error	$T_{ADC} = 14 \text{ MHz}, R_{AIN} < 10 \text{ k}\Omega$	±0.5	±1.5	LSB
ED	Differential linearity error	$T_A = 25 \text{ °C}$	±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error		±3.3	±4	
EO	Offset error	$f_{PCLK} = 48 \text{ MHz},$	±1.9	±2.8	
EG	Gain error	$T_{ADC} = 14 \text{ MHz}, R_{AIN} < 10 \text{ k}\Omega$ VDA = 2.7 V to 3.6 V	±2.8	±3	LSB
ED	Differential linearity error	$T_A = -40$ to 105 °C	±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error		±3.3	±4	
EO	Offset error	f _{PCLK} = 48 MHz,	±1.9	±2.8	
EG	Gain error	$T_{ADC} = 14 \text{ MHz}, R_{AIN} < 10 \text{ k}\Omega$ VDA = 2.4 V to 3.6 V	±2.8	±3	LSB
ED	Differential linearity error	$T_A = 25 \text{ °C}$	±0.7	±1.3	
EL	Integral linearity error	1	±1.2	±1.7	

Table 54. ADC accuracy $^{(1)(2)(3)}$

1. ADC DC accuracy values are measured after internal calibration.

 ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I_{INJ(PIN)} and ΣI_{INJ(PIN)} in Section 6.3.14 does not affect the ADC

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.14 does not affect the ADC accuracy.

3. Better performance may be achieved in restricted V_{DDA} , frequency and temperature ranges.

4. Data based on characterization results, not tested in production.



Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit			
/4	0	0.1	409.6				
/8	1	0.2	819.2				
/16	2	0.4	1638.4				
/32	3	0.8	3276.8	ms			
/64	4	1.6	6553.6				
/128	5	3.2	13107.2				
/256	6 or 7	6.4	26214.4				

Table 60. IWDG min/max timeout period at 40 kHz (LSI)⁽¹⁾

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	
2	1	0.1706	10.9226	me
4	2	0.3413 21.8453		1115
8	3	0.6826	43.6906	

Table 61. WWDG min/max timeout value at 48 MHz (PCLK)

6.3.22 Communication interfaces

I²C interface characteristics

The I^2C interface meets the timings requirements of the I^2C -bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to Section 6.3.14: I/O port characteristics for the I²C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:



Symbol	Parameter	Min	Max	Unit
t _{AF}	Maximum width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

Table 62. I²C analog filter characteristics⁽¹⁾

1. Guaranteed by design, not tested in production.

2. Spikes with widths below $t_{AF(min)}$ are filtered.

3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 63* for SPI or in *Table 64* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 20: General operating conditions*.

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Symbol	Parameter	Conditions	Min	Мах	Unit
f _{SCK}	SDI clock froguency	Master mode	-	18	M⊔⇒
1/t _{c(SCK)}	SPI Clock frequency	Slave mode	-	18	IVITIZ
$t_{r(SCK)} \ t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
t _{su(NSS)}	NSS setup time	Slave mode	4Tpclk	-	
t _{h(NSS)}	NSS hold time	Slave mode	2Tpclk + 10	-	
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode, f _{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
t _{su(MI)}	Data input satur timo	Master mode	4	-	
t _{su(SI)}		Slave mode	5	-	
t _{h(MI)}	Data input hold time	Master mode	4	-	
t _{h(SI)}		Slave mode	5	-	ns
t _{a(SO)} ⁽²⁾	Data output access time	Slave mode, f _{PCLK} = 20 MHz	0	3Tpclk	
t _{dis(SO)} ⁽³⁾	Data output disable time	Slave mode	0	18	
t _{v(SO)}	Data output valid time	Slave mode (after enable edge)	-	22.5	
t _{v(MO)}	Data output valid time	Master mode (after enable edge)	-	6	
t _{h(SO)}	Data output hold time	Slave mode (after enable edge)	11.5	-	
t _{h(MO)}		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

Table	63.	SPI	characteristics(1))
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1. Data based on characterization results, not tested in production.

2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z



Symbol		millimeters			inches ⁽¹⁾	
Symbol	Min		Мах	Min	Тур	Мах
E3	-	7.500	-	-	0.2953	-
е	-	0.500	-	-	0.0197	-
К	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
CCC	-	-	0.080	-	-	0.0031

Table 67. LQFP64 package mechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.



Figure 38. Recommended footprint for LQFP64 package

1. Dimensions are expressed in millimeters.



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.



Figure 51. LQFP32 package marking example

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.7 UFQFPN32 package information

UFQFPN32 is a 32-pin, 5x5 mm, 0.5 mm pitch ultra-thin fine-pitch quad flat package.



Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F051xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

 $P_{INTmax} = 50 \text{ mA} \times 3.5 \text{ V} = 175 \text{ mW}$

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 74* T_{Jmax} is calculated as follows:

- For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts ($-40 < T_J < 105 \text{ °C}$) see *Table 20: General operating conditions*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: $T_{Amax} = T_{Jmax} - (45^{\circ}C/W \times 447 \text{ mW}) = 105\text{-}20.115 = 84.885 ^{\circ}C$ Suffix 7: $T_{Amax} = T_{Jmax} - (45^{\circ}C/W \times 447 \text{ mW}) = 125\text{-}20.115 = 104.885 ^{\circ}C$

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 100 \text{ °C}$ (measured according to JESD51-2), $I_{DDmax} = 20 \text{ mA}, V_{DD} = 3.5 \text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8 \text{ mA}, V_{OL} = 0.4 \text{ V}$ $P_{INTmax} = 20 \text{ mA} \times 3.5 \text{ V} = 70 \text{ mW}$ $P_{IOmax} = 20 \times 8 \text{ mA} \times 0.4 \text{ V} = 64 \text{ mW}$ This gives: $P_{INTmax} = 70 \text{ mW}$ and $P_{IOmax} = 64 \text{ mW}$: $P_{Dmax} = 70 + 64 = 134 \text{ mW}$

Thus: P_{Dmax} = 134 mW



Note:

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8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 75. Or	dering inf	orma	tion s	chem	е			
Example:	STM32	F	051	R	8	Т	6	х
Device family								
STM32 = ARM-based 32-bit microcontroll	er							
Product type								
F = General-purpose								
Sub-family								
051 = STM32F051xx								
Pin count								
K = 32 pins								
T = 36 pins								
C = 48 pins								
R = 64 pins								
User code memory size								
4 = 16 Kbyte								
6 = 32 Kbyte								
8 = 64 Kbyte								
Package								
H = UFBGA								
T = LQFP								
U = UFQFPN								
Y = WLCSP								
Temperature range								
6 = -40 °C to +85 °C								
7 = -40 °C to +105 °C								
Options								
xxx = code ID of programmed parts (inclu	des nackin	n tvne)					

xxx = code ID of programmed parts (includes packing type) TR = tape and reel packing blank = tray packing



Date	Revision	Changes
28-Aug-2015	5 (continued)	 Table 31: Peripheral current consumption Addition of WLCSP36 package. Updates in: Section 2: Description Table 2: STM32F051xx family device features and peripheral count Section 4: Pinouts and pin descriptions with the addition of Figure 7: WLCSP36 package pinout Table 13: Pin definitions Table 20: General operating conditions Section 7: Package information with the addition of Section 7.5: WLCSP36 package information Table 74: Package thermal characteristics Section 8: Part numbering Update of the device marking examples in Section 7: Package information.
16-Dec-2015	6	 Section 2: Description: Table 2: STM32F051xx family device features and peripheral count - number of SPIs corrected for 64-pin packages Figure 1: Block diagram modified Section 3: Functional overview: Figure 2: Clock tree modified; divider for CEC corrected Table 8: Comparison of I²C analog and digital filters - adding 20 mA information for FastPlus mode Section 4: Pinouts and pin descriptions: Package pinout figures updated (look and feel) Figure 7: WLCSP36 package pinout - now presented in top view Table 13: Pin definitions - notes added (VSSA corrected to pin 16 on LQFP32); note 5 added Section 6: Electrical characteristics: Table 24: Embedded internal reference voltage - removed - 40°C-85°C temperature range line and the associated note Table 48: I/O static characteristics - removed note Section 6.3.16: 12-bit ADC characteristics - changed introductory sentence Table 52: ADC characteristics updated and table footnotes 3 and 4 added Table 59: TIMx characteristics reorganized Figure 52: UFQFPN32 package outline - figure footnotes added

Table 76. Document revision history (continued)

