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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051k8u7tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14), DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 55 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 3 internal (temperature



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can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision



The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I²C)

Up to two I²C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) and Fast mode (up to 400 kbit/s) and, I2C1 also supports Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	 Extra filtering capability vs. standard requirements Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

Table 8. C	Comparison	of I ² C analog	and digital filters
		•••••••••••••••••••••••••••••••••••••••	

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripherals can be served by the DMA controller.

Refer to Table 9 for the differences between I2C1 and I2C2.

Table 9. STM32F051xx I ² C in	nplementation
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I ² C features ⁽¹⁾	I2C1	I2C2
7-bit addressing mode	Х	Х
10-bit addressing mode	Х	Х
Standard mode (up to 100 kbit/s)	Х	Х
Fast mode (up to 400 kbit/s)	Х	Х
Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive I/Os	Х	-
Independent clock	Х	-



3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I²S)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in fullduplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I²S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

SPI features ⁽¹⁾	SPI1	SPI2
Hardware CRC calculation	Х	Х
Rx/Tx FIFO	Х	Х
NSS pulse mode	Х	Х
I ² S mode	х	-
TI mode	Х	Х

Table 44	OTM00F0F4	001/120 :	
Table 11.	SIM32F051XX	SPI/I-S Ir	nplementation

1. X = supported.

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.20 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.





Figure 8. LQFP32 package pinout







	Ρ	'in ni	umbe	er						Pin functions	
LQFP64	UFBGA64	LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	Pin name (function upon reset)	Pin type	I/O structure Notes		Alternate functions	Additional functions
22	G4	16	E3	12	12	PA6	I/O	ТТа	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT	ADC_IN6
23	H4	17	F4	13	13	PA7	I/O	ТТа	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
24	H5	-	-	-	-	PC4	I/O	TTa	-	EVENTOUT	ADC_IN14
25	H6	-	-	-	-	PC5	I/O	TTa	-	TSC_G3_IO1	ADC_IN15
26	F5	18	F3	14	14	PB0	I/O	ТТа	-	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	ADC_IN8
27	G5	19	F2	15	15	PB1	I/O	ТТа	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
28	G6	20	D2	-	16	PB2	I/O	FT	(4)	TSC_G3_IO4	-
29	G7	21	-	-	-	PB10	I/O	FT	(5)	I2C2_SCL, CEC, TIM2_CH3, TSC_SYNC	-
30	H7	22	-	-	-	PB11	I/O	FT	(5)	I2C2_SDA, TIM2_CH4, TSC_G6_IO1, EVENTOUT	-
31	D4	23	F1	16	0	VSS	S	-	-	Gro	und
32	E4	24	E1	17	17	VDD	S	-	-	Digital power supply	

Table 13. Pin definitions (continued)



	P	Pin nu	umbe	er						Pin functions	
LQFP64	UFBGA64	LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
33	H8	25	-	-	-	PB12	I/O	FT	(5)	SPI2_NSS, TIM1_BKIN, TSC_G6_IO2, EVENTOUT	-
34	G8	26	-	-	-	PB13	I/O	FT	(5)	SPI2_SCK, TIM1_CH1N, TSC_G6_IO3	-
35	F8	27	-	-	-	PB14	I/O	FT	(5)	SPI2_MISO, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	-
36	F7	28	-	-	-	PB15	I/O	FT	(5)	SPI2_MOSI, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	RTC_REFIN
37	F6	-	-	-	-	PC6	I/O	FT	-	TIM3_CH1	-
38	E7	-	-	-	-	PC7	I/O	FT	-	TIM3_CH2	-
39	E8	-	-	-	-	PC8	I/O	FT	-	TIM3_CH3	-
40	D8	-	-	-	-	PC9	I/O	FT	-	TIM3_CH4	-
41	D7	29	E2	18	18	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	C7	30	D1	19	19	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1	-
43	C6	31	C1	20	20	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2	-
44	C8	32	C2	21	21	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	-

Table 13. Pin definitions (continued)



Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
ANDZ	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
AHB1	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
APB	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 16. STM32F051xx peripheral register boundary addresses

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6.1.7 Current consumption measurement



Figure 14. Current consumption measurement scheme



Symbol	Ratings	Max.	Unit
ΣI _{VDD}	Total current into sum of all VDD power lines (source) ⁽¹⁾	120	
ΣI _{VSS}	Total current out of sum of all VSS ground lines (sink) ⁽¹⁾	-120	
I _{VDD(PIN)}	Maximum current into each VDD power pin (source) ⁽¹⁾	100	
I _{VSS(PIN)}	Maximum current out of each VSS ground pin (sink) ⁽¹⁾	-100	
	Output current sunk by any I/O and control pin	25	
IO(PIN)	Output current source by any I/O and control pin	-25	
ΣL	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	80	
∠IO(PIN)	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	-80	mA
	Injected current on B, FT and FTf pins	-5/+0 ⁽⁴⁾	
I _{INJ(PIN)} ⁽³⁾	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins ⁽⁵⁾	± 5	
ΣI _{INJ(PIN)}	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	± 25	1

Table 18. Current characteristics

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.

3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 17: Voltage characteristics* for the maximum allowed input voltage values.

4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

On these I/Os, a positive injection is induced by V_{IN} > V_{DDA}. Negative injection disturbs the analog performance of the device. See note ⁽²⁾ below *Table 54: ADC accuracy*.

6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 19. Thermal characteristics

Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	–65 to +150	°C
TJ	Maximum junction temperature	150	°C



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 35*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Тур	Max ⁽²⁾	Unit
f _{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R _F	Feedback resistor	-	-	200	-	kΩ
		During startup ⁽³⁾	-	-	8.5	
IDD	HSE current consumption	V _{DD} = 3.3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.4	-	
		V _{DD} = 3.3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V _{DD} = 3.3 V, Rm = 30 Ω, CL = 5 pF@32 MHz	-	0.8	-	mA
		V _{DD} = 3.3 V, Rm = 30 Ω, CL = 10 pF@32 MHz	-	1	-	
		V _{DD} = 3.3 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
9 _m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

Table 35.	HSE	oscillator	characteristics
	-		

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by design, not tested in production.

3. This consumption level occurs during the first 2/3 of the $t_{SU(\text{HSE})}$ startup time

4. t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.



High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
f _{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1 ⁽²⁾	%
DuCy _(HSI14)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
	Accuracy of the HSI14 oscillator (factory calibrated)	T _A = -40 to 105 °C	-4.2 ⁽³⁾	-	5.1 ⁽³⁾	%
100		T _A = −10 to 85 °C	-3.2 ⁽³⁾	-	3.1 ⁽³⁾	%
ACC _{HSI14}		T _A = 0 to 70 °C	-2.5 ⁽³⁾	-	2.3 ⁽³⁾	%
		T _A = 25 °C	-1	-	1	%
t _{su(HSI14)}	HSI14 oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs
I _{DDA(HSI14)}	HSI14 oscillator power consumption	-	_	100	150 ⁽²⁾	μA

Table 38. HSI14 oscillator characteristics⁽¹⁾

1. V_{DDA} = 3.3 V, T_A = -40 to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

3. Data based on characterization results, not tested in production.



Figure 20. HSI14 oscillator accuracy characterization results



Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
		TC, FT and FTf I/O TTa in digital mode V _{SS} ≤ V _{IN} ≤ V _{DDIOx}	-	-	± 0.1	
Input leakage I _{lkg} current ⁽²⁾	Input leakage	TTa in digital mode V _{DDIOx} ≤ V _{IN} ≤ V _{DDA}	-	-	1	μA
		TTa in analog mode V _{SS} ≤ V _{IN} ≤ V _{DDA}	-	-	± 0.2	
	FT and FTf I/O V _{DDIOx} ≤ V _{IN} ≤ 5 V	-	-	10		
R _{PU}	Weak pull-up equivalent resistor (3)	V _{IN} = V _{SS}	25	40	55	kΩ
R _{PD}	Weak pull-down equivalent resistor ⁽³⁾	V _{IN} = - V _{DDIOx}	25	40	55	kΩ
C _{IO}	I/O pin capacitance	-	-	5	-	pF

Table 48. I/O static characteristics (continued)

1. Data based on design simulation only. Not tested in production.

2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 47: I/O current injection susceptibility*.

 Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 21* for standard I/Os, and in *Figure 22* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.



6.3.17 DAC electrical specifications

Symbol	Parameter	Min	Тур	Max	Unit	Comments
V _{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	V	-
D (1)	Resistive load with buffer	5	-	-	kΩ	Load connected to V _{SSA}
►LOAD` ′	ON	25	-	-	kΩ	Load connected to V _{DDA}
R ₀ ⁽¹⁾	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
C _{LOAD} ⁽¹⁾	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xE1C) at
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer ON	-	-	V _{DDA} – 0.2	V	$V_{DDA} = 3.6 V \text{ and } (0x155) \text{ and}$ (0xEAB) at $V_{DDA} = 2.4 V$
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer OFF	-	-	V _{DDA} – 1LSB	V	excursion of the DAC.
lpo (¹)	DAC DC current	-	-	600	μA	With no load, middle code (0x800) on the input
'DDA	mode ⁽²⁾	-	-	700	μA	With no load, worst code (0xF1C) on the input
DNL ⁽³⁾	Differential non linearity Difference between two	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
	consecutive code-1LSB)	-	-	±2	LSB	Given for the DAC in 12-bit configuration
	Integral non linearity (difference between	-	-	±1	LSB	Given for the DAC in 10-bit configuration
INL ⁽³⁾ measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)		-	-	±4	LSB	Given for the DAC in 12-bit configuration
	Offset error	-	-	±10	mV	-
Offset ⁽³⁾	(difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$)	-	-	±3	LSB	Given for the DAC in 10-bit at V _{DDA} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at $V_{DDA} = 3.6 V$

Table	55.	DAC	charac	teristics
Table	55.	DAO	charac	



Symbol	Parameter	Min	Тур	Мах	Unit	Comments
Gain error ⁽³⁾	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
t _{SETTLING} ⁽³⁾	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	μs	C _{LOAD} ≤ 50 pF, R _{LOAD} ≥ 5 kΩ
Update rate ⁽³⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	C _{LOAD} ≤ 50 pF, R _{LOAD} ≥ 5 kΩ
t _{WAKEUP} ⁽³⁾	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	μs	$C_{LOAD} \le 50 \text{ pF}, R_{LOAD} \ge 5 \text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR+ ⁽¹⁾	Power supply rejection ratio (to V _{DDA}) (static DC measurement	-	-67	-40	dB	No R _{LOAD} , C _{LOAD} = 50 pF

Table 55. DAC characteristics (continued)

1. Guaranteed by design, not tested in production.

2. The DAC is in "quiescent mode" when it keeps the value steady on the output so no dynamic consumption is involved.

3. Data based on characterization results, not tested in production.



Figure 27. 12-bit buffered / non-buffered DAC

The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register. 1.





Figure 33. I²S master timing diagram (Philips protocol)

- 1. Data based on characterization results, not tested in production.
- 2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.



9 Revision history

Date	Revision	Changes
05-Apr-2012	1	Initial release
25-Apr-2012	2	Updated Table: STM32F051xx family device features and peripheral counts for SPI and I ² C in 32-pin package. Corrected Group 3 pin order in Table: Capacitive sensing GPIOs available on STM32F051xx devices. Updated the current consumption values in Section: Electrical characteristics. Updated Table: HSI14 oscillator characteristics
23-Jul-2012	3	Features reorganized and <i>Figure: Block diagram</i> structure changed. Added LQFP32 package. Updated <i>Section: Cyclic redundancy check calculation unit</i> (<i>CRC</i>). Modified the number of priority levels in <i>Section: Nested</i> <i>vectored interrupt controller (NVIC)</i> . Added note 3. for PB2 and PB8, changed TIM2_CH_ETR into TIM2_CH1_ETR in <i>Table: Pin definitions</i> and <i>Table: Alternate</i> <i>functions selected through GPIOA_AFR registers for port A</i> . Added <i>Table: Alternate functions selected through GPIOB_AFR</i> <i>registers for port B</i> . Updated I _{VDD} , I _{VSS} , and I _{INJ(PIN)} in <i>Table: Current</i> <i>characteristics</i> . Updated ACC _{HSI} in <i>Table: HSI oscillator characteristics</i> and <i>Table: HS114 oscillator characteristics</i> . Updated Table: <i>I/O current injection susceptibility</i> . Added BOOT0 input low and high level voltage in <i>Table: I/O</i> <i>static characteristics</i> . Modified number of pins in V _{OL} and V _{OH} description, and changed condition for V _{OLFM+} in <i>Table: Output voltage</i> <i>characteristics</i> . Changed V _{DD} to V _{DDA} in <i>Figure: Typical connection diagram</i> <i>using the ADC</i> . Updated Figure: <i>I/O AC characteristics definition</i> .

Table 76. Document revision history



Date	Revision	Changes
		Added "Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection" in Section Functional susceptibility to I/O current injection. Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in Table : ESD absolute maximum ratings.
		and Standby modes and Table: Typical and maximum VDD consumption in Stop and Standby modes and Table: Typical and maximum VDDA consumption in Stop and Standby modes into Table: Typical and maximum current consumption in Stop and Standby modes.
		- Table: Temperature sensor calibration values
		- Table: Internal voltage reference calibration values.
		– Table: Current characteristics,
	4	 Table: General operating conditions,
		 Table: Typical and maximum current consumption from the VDDA supply,
		 Table: Low-power mode wakeup timings,
		 Table: I/O current injection susceptibility,
		 Table: I/O static characteristics,
13-Jan-2014		 Table: Output voltage characteristics,
	(continued)	– Table: NRST pin characteristics,
		 Table: I²C analog filter characteristics,
		 Figure: Power supply scheme,
		 Figure: TC and TTa I/O input characteristics,
		 Figure: Five volt tolerant (FT and FTf) I/O input characteristics,
		 Figure: I/O AC characteristics definition,
		 Figure: ADC accuracy characteristics,
		 Figure: Typical connection diagram using the ADC,
		 Figure: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline,
		 Figure: LQFP64 recommended footprint,
		 Figure: LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline,
		– Figure: LQFP48 recommended footprint,
		 Figure: LQFP32 – 7 x 7 mm 32-pin low-profile quad flat package outline,
		– Figure: LQFP32 recommended footprint,
		 Figure: UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package outline.

Table 76. Document revision history (continued)



Date	Revision	Changes
28-Aug-2015	5 (continued)	 Table 31: Peripheral current consumption Addition of WLCSP36 package. Updates in: Section 2: Description Table 2: STM32F051xx family device features and peripheral count Section 4: Pinouts and pin descriptions with the addition of Figure 7: WLCSP36 package pinout Table 13: Pin definitions Table 20: General operating conditions Section 7: Package information with the addition of Section 7.5: WLCSP36 package information Table 74: Package thermal characteristics Section 8: Part numbering Update of the device marking examples in Section 7: Package information.
16-Dec-2015	6	 Section 2: Description: Table 2: STM32F051xx family device features and peripheral count - number of SPIs corrected for 64-pin packages Figure 1: Block diagram modified Section 3: Functional overview: Figure 2: Clock tree modified; divider for CEC corrected Table 8: Comparison of I²C analog and digital filters - adding 20 mA information for FastPlus mode Section 4: Pinouts and pin descriptions: Package pinout figures updated (look and feel) Figure 7: WLCSP36 package pinout - now presented in top view Table 13: Pin definitions - notes added (VSSA corrected to pin 16 on LQFP32); note 5 added Section 6: Electrical characteristics: Table 24: Embedded internal reference voltage - removed - 40°C-85°C temperature range line and the associated note Table 48: I/O static characteristics - removed note Section 6.3.16: 12-bit ADC characteristics - changed introductory sentence Table 52: ADC characteristics updated and table footnotes 3 and 4 added Table 59: TIMx characteristics reorganized Figure 52: UFQFPN32 package outline - figure footnotes added

Table 76. Document revision history (continued)



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