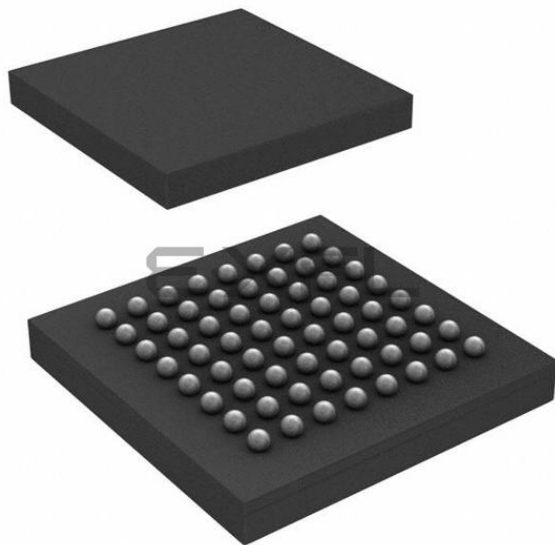




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	55
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051r8h6tr

Contents

1	Introduction	9
2	Description	10
3	Functional overview	13
3.1	ARM [®] -Cortex [®] -M0 core	13
3.2	Memories	13
3.3	Boot modes	13
3.4	Cyclic redundancy check calculation unit (CRC)	14
3.5	Power management	14
3.5.1	Power supply schemes	14
3.5.2	Power supply supervisors	14
3.5.3	Voltage regulator	14
3.5.4	Low-power modes	15
3.6	Clocks and startup	15
3.7	General-purpose inputs/outputs (GPIOs)	16
3.8	Direct memory access controller (DMA)	17
3.9	Interrupts and events	17
3.9.1	Nested vectored interrupt controller (NVIC)	17
3.9.2	Extended interrupt/event controller (EXTI)	17
3.10	Analog-to-digital converter (ADC)	17
3.10.1	Temperature sensor	18
3.10.2	Internal voltage reference (V_{REFINT})	18
3.10.3	V_{BAT} battery voltage monitoring	19
3.11	Digital-to-analog converter (DAC)	19
3.12	Comparators (COMP)	19
3.13	Touch sensing controller (TSC)	19
3.14	Timers and watchdogs	21
3.14.1	Advanced-control timer (TIM1)	21
3.14.2	General-purpose timers (TIM2, 3, 14, 15, 16, 17)	22
3.14.3	Basic timer TIM6	22
3.14.4	Independent watchdog (IWDG)	22
3.14.5	System window watchdog (WWDG)	23

3.14.6	SysTick timer	23
3.15	Real-time clock (RTC) and backup registers	23
3.16	Inter-integrated circuit interface (I ² C)	24
3.17	Universal synchronous/asynchronous receiver/transmitter (USART)	25
3.18	Serial peripheral interface (SPI) / Inter-integrated sound interface (I ² S)	26
3.19	High-definition multimedia interface (HDMI) - consumer electronics control (CEC)	26
3.20	Serial wire debug port (SW-DP)	26
4	Pinouts and pin descriptions	27
5	Memory mapping	39
6	Electrical characteristics	42
6.1	Parameter conditions	42
6.1.1	Minimum and maximum values	42
6.1.2	Typical values	42
6.1.3	Typical curves	42
6.1.4	Loading capacitor	42
6.1.5	Pin input voltage	42
6.1.6	Power supply scheme	43
6.1.7	Current consumption measurement	44
6.2	Absolute maximum ratings	45
6.3	Operating conditions	47
6.3.1	General operating conditions	47
6.3.2	Operating conditions at power-up / power-down	47
6.3.3	Embedded reset and power control block characteristics	48
6.3.4	Embedded reference voltage	49
6.3.5	Supply current characteristics	49
6.3.6	Wakeup time from low-power mode	59
6.3.7	External clock source characteristics	59
6.3.8	Internal clock source characteristics	63
6.3.9	PLL characteristics	66
6.3.10	Memory characteristics	66
6.3.11	EMC characteristics	67
6.3.12	Electrical sensitivity characteristics	68
6.3.13	I/O current injection characteristics	69

2 Description

The STM32F051xx microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 64 Kbytes of Flash memory and 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I²Cs, up to two SPIs, one I²S, one HDMI CEC and up to two USARTs), one 12-bit ADC, one 12-bit DAC, six 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F051xx microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F051xx microcontrollers include devices in seven different packages ranging from 32 pins to 64 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F051xx microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{\text{DDA}} = 3.3$ V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{\text{DDA}} = 3.3$ V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{\text{DDA}} = 3.3$ V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

Figure 8. LQFP32 package pinout

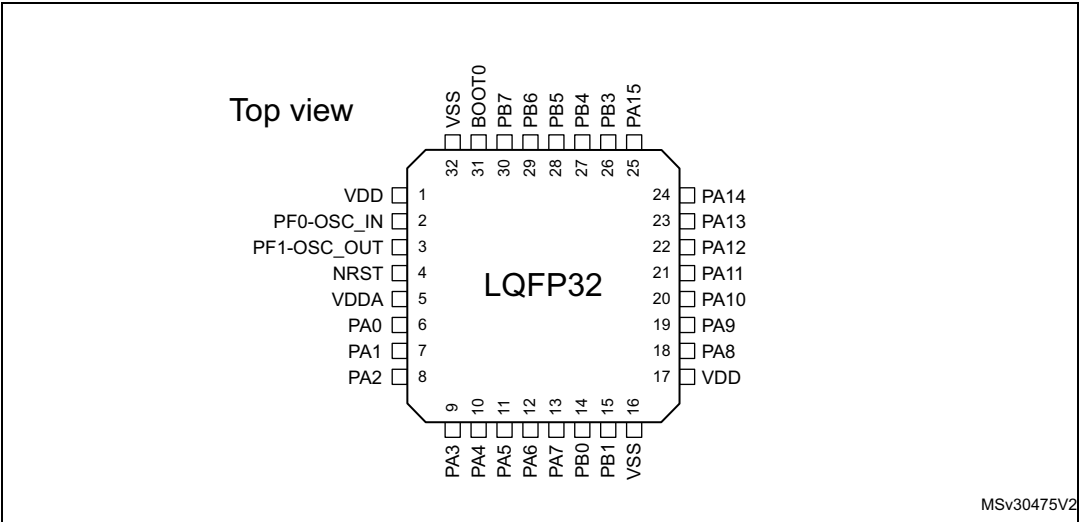
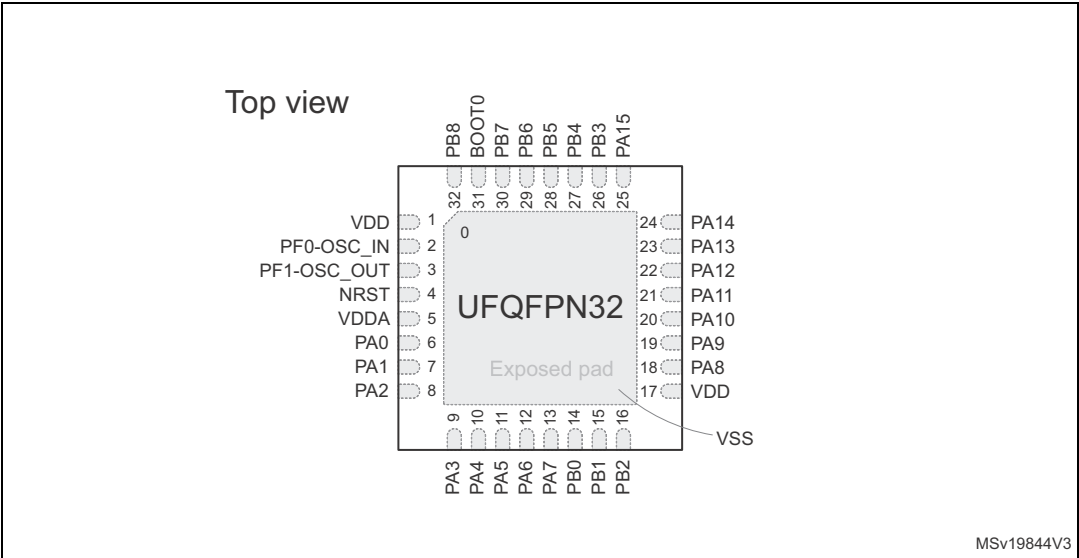


Figure 9. UFQFPN32 package pinout



**Table 15. Alternate functions selected through GPIOB_AFR registers for port B**

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3
PB2				TSC_G3_IO4
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1
PB12	SPI2_NSS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2
PB13	SPI2_SCK		TIM1_CH1N	TSC_G6_IO3
PB14	SPI2_MISO	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4
PB15	SPI2_MOSI	TIM15_CH2	TIM1_CH3N	TIM15_CH1N

Table 21. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	$\mu\text{s/V}$
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 22](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 22. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}^{(1)}$	Power on/power down reset threshold	Falling edge ⁽²⁾	1.80	1.88	1.96 ⁽³⁾	V
		Rising edge	1.84 ⁽³⁾	1.92	2.00	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}^{(4)}$	Reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD} .
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

Table 23. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V

Table 25. Typical and maximum current consumption from V_{DD} at 3.6 V (continued)

Symbol	Parameter	Conditions	f _{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T _A ⁽¹⁾			Typ	Max @ T _A ⁽¹⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DD}	Supply current in Sleep mode	HSE bypass, PLL on	48 MHz	14.0	15.3 ⁽²⁾	15.3	16.0 ⁽²⁾	2.8	3.0 ⁽²⁾	3.0	3.2 ⁽²⁾	mA
			32 MHz	9.5	10.2	10.2	10.7	2.0	2.1	2.1	2.3	
			24 MHz	7.3	7.8	7.8	8.3	1.5	1.7	1.7	1.9	
		HSE bypass, PLL off	8 MHz	2.6	2.9	2.9	3.0	0.6	0.8	0.8	0.8	
			1 MHz	0.4	0.6	0.6	0.6	0.2	0.4	0.4	0.4	
		HSI clock, PLL on	48 MHz	14.0	15.3	15.3	16.0	3.8	4.0	4.1	4.2	
			32 MHz	9.5	10.2	10.2	10.7	2.6	2.7	2.8	2.8	
			24 MHz	7.3	7.8	7.8	8.3	2.0	2.1	2.1	2.1	
		HSI clock, PLL off	8 MHz	2.6	2.9	2.9	3.0	0.6	0.8	0.8	0.8	

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 26. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f _{HCLK}	V _{DDA} = 2.4 V				V _{DDA} = 3.6 V				Unit
				Typ	Max @ T _A ⁽²⁾			Typ	Max @ T _A ⁽²⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSE bypass, PLL on	48 MHz	150	170 ⁽³⁾	178	182 ⁽³⁾	164	183 ⁽³⁾	195	198 ⁽³⁾	μA
			32 MHz	104	121	126	128	113	129	135	138	
			24 MHz	82	96	100	103	88	102	106	108	
		HSE bypass, PLL off	8 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
			1 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
		HSI clock, PLL on	48 MHz	220	240	248	252	244	263	275	278	
			32 MHz	174	191	196	198	193	209	215	218	
			24 MHz	152	167	173	174	168	183	190	192	
		HSI clock, PLL off	8 MHz	72	79	82	83	83.5	91	94	95	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent of clock frequencies.

2. Data based on characterization results, not tested in production unless otherwise specified.

3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 28. Typical and maximum current consumption from the V_{BAT} supply

Symbol	Parameter	Conditions	Typ @ V _{BAT}						Max ⁽¹⁾			Unit
			1.65 V	1.8 V	2.4 V	2.7 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD-VBAT}	RTC domain supply current	LSE & RTC ON; "Xtal mode": lower driving capability; LSEDRV[1:0] = '00'	0.5	0.5	0.6	0.7	0.8	0.9	1.0	1.3	1.7	μA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.8	0.8	0.9	1.0	1.1	1.2	1.3	1.6	2.1	

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = V_{DDA} = 3.3 V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to f_{HCLK} frequency:
 - 0 wait state and Prefetch OFF from 0 to 24 MHz
 - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Table 47. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on PA10, PA12, PB4, PB5, PB10, PB15 and PD2 pins with induced leakage current on adjacent pins less than –10 μ A	–5	NA	
	Injected current on all other FT and FTf pins	–5	NA	
	Injected current on PA6 and PC0	–0	+5	
	Injected current on all other TTa, TC and RST pins	–5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 48](#) are derived from tests performed under the conditions summarized in [Table 20: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 48. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3 V_{DDIOx} + 0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475 V_{DDIOx} - 0.2^{(1)}$	
		BOOT0	-	-	$0.3 V_{DDIOx} - 0.3^{(1)}$	
		All I/Os except BOOT0 pin	-	-	$0.3 V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445 V_{DDIOx} + 0.398^{(1)}$	-	-	V
		FT and FTf I/O	$0.5 V_{DDIOx} + 0.2^{(1)}$	-	-	
		BOOT0	$0.2 V_{DDIOx} + 0.95^{(1)}$	-	-	
		All I/Os except BOOT0 pin	$0.7 V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200 ⁽¹⁾	-	mV
		FT and FTf I/O	-	100 ⁽¹⁾	-	
		BOOT0	-	300 ⁽¹⁾	-	

Table 48. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current ⁽²⁾	TC, FT and FTf I/O TTa in digital mode $V_{SS} \leq V_{IN} \leq V_{DDIOx}$	-	-	± 0.1	μA
		TTa in digital mode $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O $V_{DDIOx} \leq V_{IN} \leq 5 V$	-	-	10	
R_{PU}	Weak pull-up equivalent resistor ⁽³⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
R_{PD}	Weak pull-down equivalent resistor ⁽³⁾	$V_{IN} = -V_{DDIOx}$	25	40	55	k Ω
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 47: I/O current injection susceptibility](#).
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 21](#) for standard I/Os, and in [Figure 22](#) for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

6.3.19 Temperature sensor characteristics

Table 57. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
V_{30}	Voltage at 30 $^{\circ}\text{C}$ (± 5 $^{\circ}\text{C}$) ⁽²⁾	1.34	1.43	1.52	V
$t_{START}^{(1)}$	ADC_IN16 buffer startup time	-	-	10	μs
$t_{S_temp}^{(1)}$	ADC sampling time when reading the temperature	4	-	-	μs

1. Guaranteed by design, not tested in production.
2. Measured at $V_{DDA} = 3.3 \text{ V} \pm 10 \text{ mV}$. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to [Table 3: Temperature sensor calibration values](#).

6.3.20 V_{BAT} monitoring characteristics

Table 58. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	2 x 50	-	k Ω
Q	Ratio on V_{BAT} measurement	-	2	-	-
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$t_{S_vbat}^{(1)}$	ADC sampling time when reading the V_{BAT}	4	-	-	μs

1. Guaranteed by design, not tested in production.

6.3.21 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to [Section 6.3.14: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 59. TIMx characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	24	-	MHz
t_{MAX_COUNT}	16-bit timer maximum period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	1365	-	μs
	32-bit counter maximum period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	89.48	-	s

Table 60. IWDG min/max timeout period at 40 kHz (LSI)⁽¹⁾

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 61. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.22 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to [Section 6.3.14: I/O port characteristics](#) for the I²C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 62. I²C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in [Table 63](#) for SPI or in [Table 64](#) for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 63. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, $f_{PCLK} = 36$ MHz, presc = 4	Tpclk/2 - 2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	4	-	
		Slave mode	5	-	
$t_{a(SO)}^{(2)}$	Data output access time	Slave mode, $f_{PCLK} = 20$ MHz	0	3Tpclk	
$t_{dis(SO)}^{(3)}$	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$ $t_{h(MO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 29. SPI timing diagram - slave mode and CPHA = 0

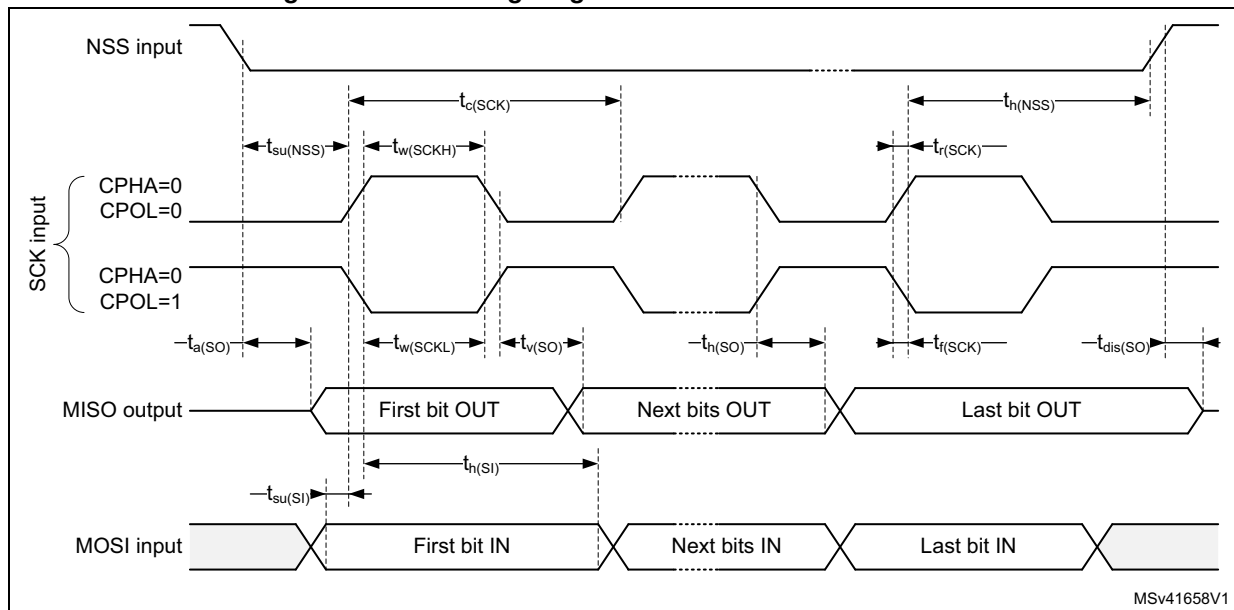
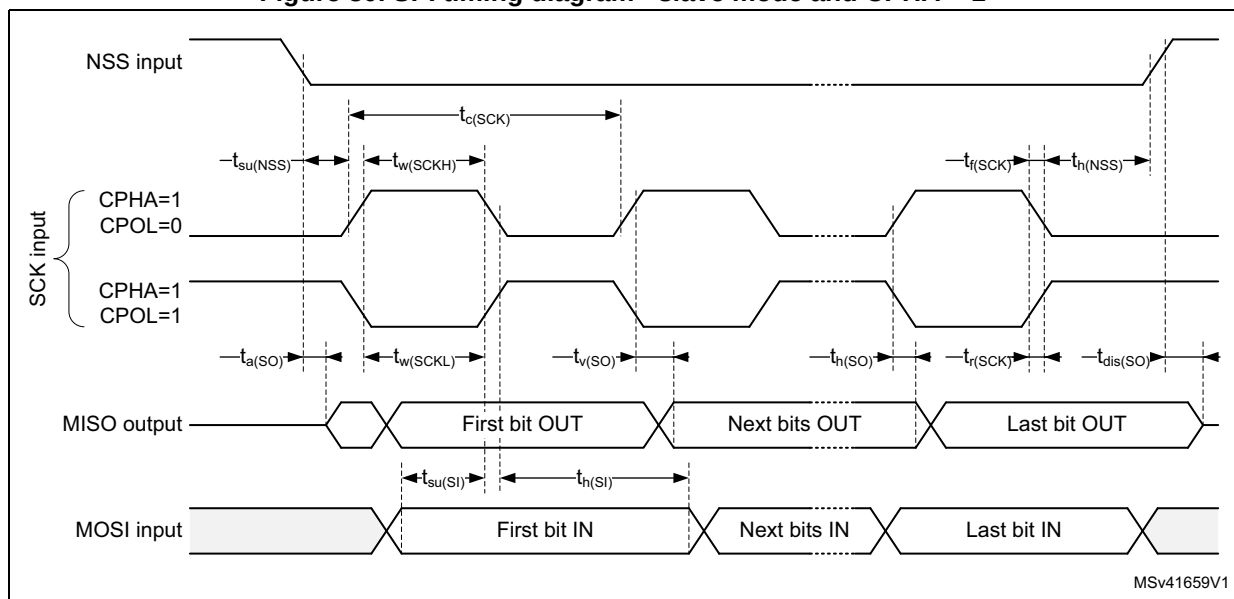


Figure 30. SPI timing diagram - slave mode and CPHA = 1

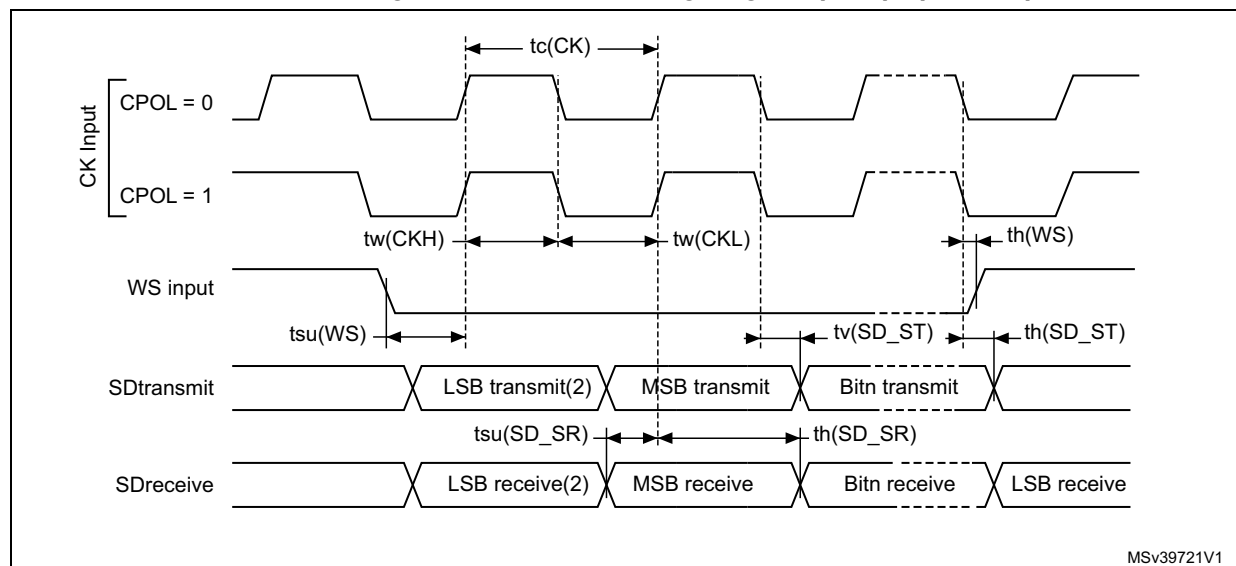


1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

Table 64. I²S characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su}(SD_MR)$	Data input setup time	Master receiver	6	-	ns
$t_{su}(SD_SR)$		Slave receiver	2	-	
$t_h(SD_MR)^{(2)}$	Data input hold time	Master receiver	4	-	
$t_h(SD_SR)^{(2)}$		Slave receiver	0.5	-	
$t_v(SD_MT)^{(2)}$	Data output valid time	Master transmitter	-	4	
$t_v(SD_ST)^{(2)}$		Slave transmitter	-	20	
$t_h(SD_MT)$	Data output hold time	Master transmitter	0	-	
$t_h(SD_ST)$		Slave transmitter	13	-	

1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK} . For example, if $f_{PCLK} = 8$ MHz, then $T_{PCLK} = 1/f_{PCLK} = 125$ ns.

Figure 32. I²S slave timing diagram (Philips protocol)

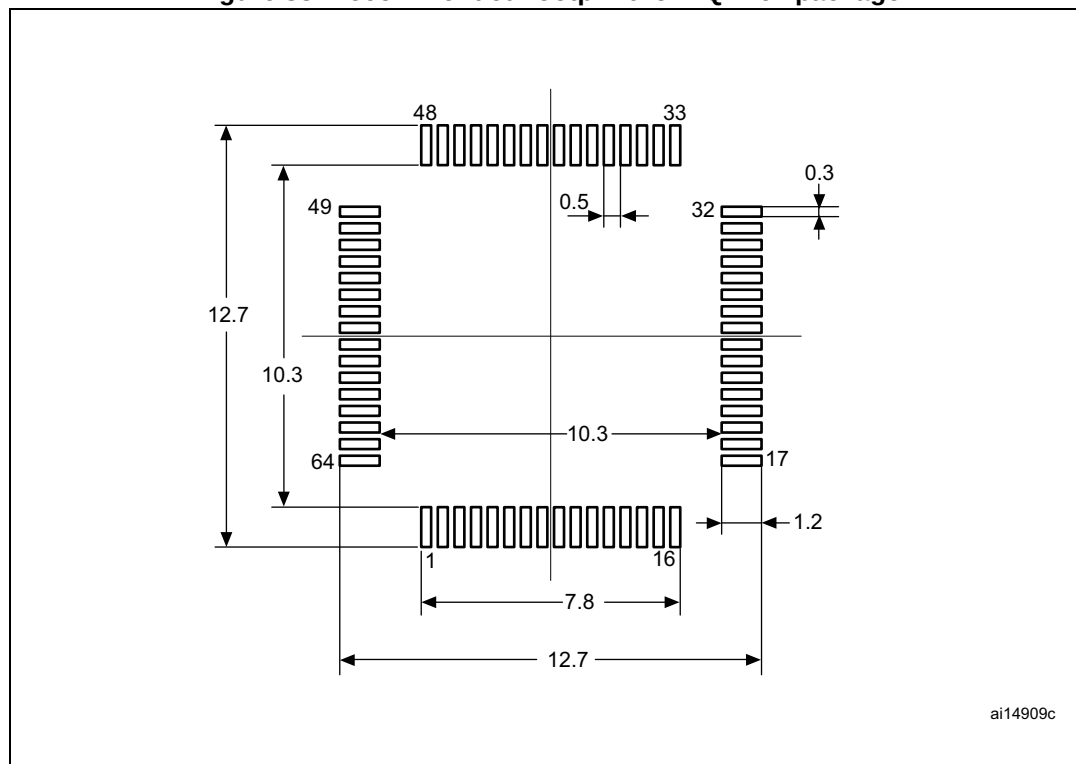
1. Measurement points are done at CMOS levels: $0.3 \times V_{DDIOx}$ and $0.7 \times V_{DDIOx}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 67. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. Recommended footprint for LQFP64 package



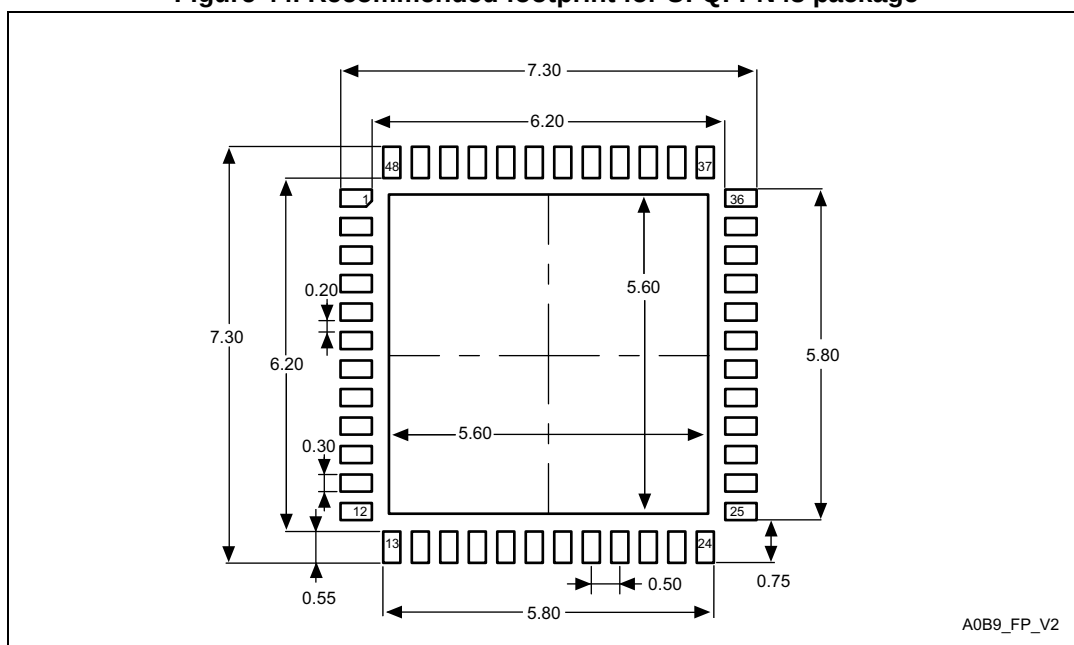
1. Dimensions are expressed in millimeters.

Table 69. UFQFPN48 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. Recommended footprint for UFQFPN48 package



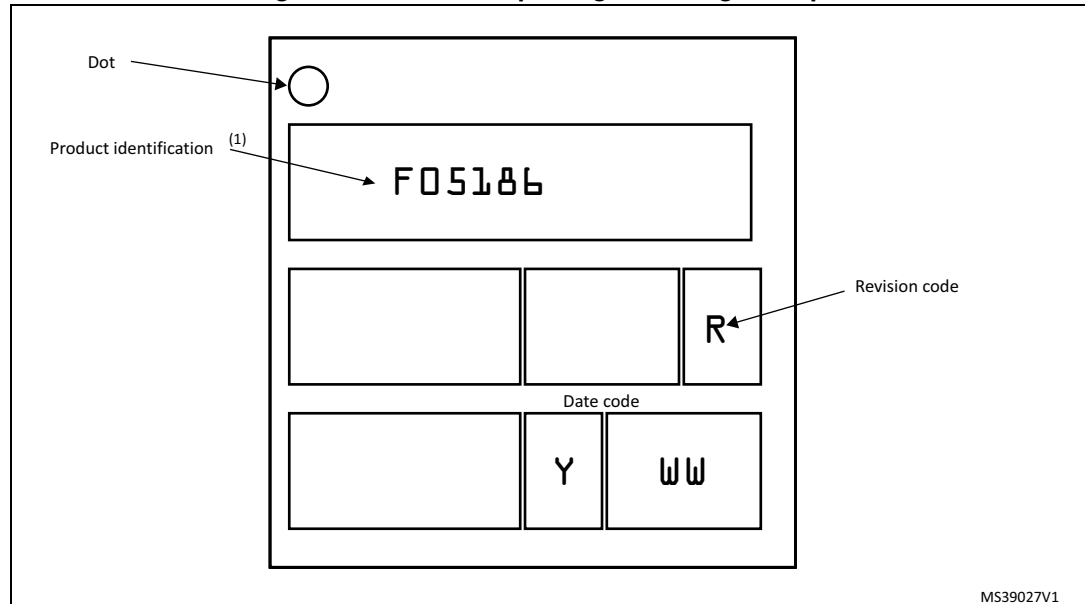
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 48. WLCSP36 package marking example



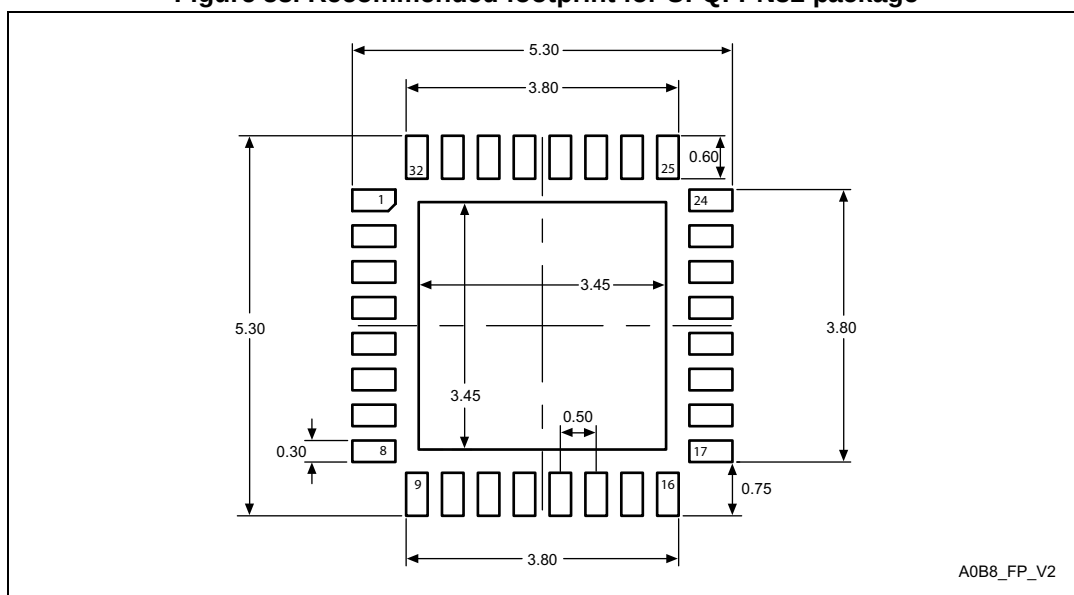
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 73. UFQFPN32 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 53. Recommended footprint for UFQFPN32 package



1. Dimensions are expressed in millimeters.