STMicroelectronics - STM32F051R8T6 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	55
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f051r8t6

Contents

Table 2. STM32F051xx family device features and peripheral count

Peripheral		STM32F051Kx			STM32F051T8	STM32F051Cx			STM32F051Rx		
Flash memory (Kbyte)		16	32	64	64	16	32	64	16	32	64
SRAM (Kbyte)		8									
Timers	Advanced control	1 (16-bit)									
	General purpose	5 (16-bit) 1 (32-bit)									
	Basic	1 (16-bit)									
Comm. interfaces	SPI [I^2S](1)	1 [1](2)			1 [1](2)	1 [1](2)		2 [1]	2 [1]		
	I^2C	1(3)			1(3)	1(3)		2	1(3)		2
	USART	1(4)	2		2	1(4)	2		1(4)	2	
	CEC	1									
12-bit ADC (number of channels)		1 (10 ext. + 3 int.)							1 (16 ext. + 3 int.)		
12-bit DAC (number of channels)		1 (1)									
Analog comparator		2									
GPIOs		25 (on LQFP32) 27 (on UFQFPN32)			29	39			55		
Capacitive sensing channels		13 (on LQFP32) 14 (on UFQFPN32)			14	17			18		
Max. CPU frequency		48 MHz									
Operating voltage		2.0 to 3.6 V									
Operating temperature		Ambient operating temperature: -40°C to 85°C / -40°C to 105°C Junction temperature: -40°C to 105°C / -40°C to 125°C									
Packages		LQFP32 UFQFPN32			WLCSP36	LQFP48 UFQFPN48			LQFP64 UFBGA64		

1. The SPI1 interface can be used either in SPI mode or in I^2S audio mode.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART2 is not present.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F051xx microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1,, COMPx or the CEC.

  The CEC, USART1 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

Table 13. Pin definitions (continued)

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	UFBGA64	LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32					Alternate functions	Additional functions
33	H8	25	-	-	-	PB12	I/O	FT	(5)	SPI2_NSS, TIM1_BKIN, TSC_G6_IO2, EVENTOUT	-
34	G8	26	-	-	-	PB13	I/O	FT	(5)	SPI2_SCK, TIM1_CH1N, TSC_G6_IO3	-
35	F8	27	-	-	-	PB14	I/O	FT	(5)	SPI2_MISO, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	-
36	F7	28	-	-	-	PB15	I/O	FT	(5)	SPI2_MOSI, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	RTC_REFIN
37	F6	-	-	-	-	PC6	I/O	FT	-	TIM3_CH1	-
38	E7	-	-	-	-	PC7	I/O	FT	-	TIM3_CH2	-
39	E8	-	-	-	-	PC8	I/O	FT	-	TIM3_CH3	-
40	D8	-	-	-	-	PC9	I/O	FT	-	TIM3_CH4	-
41	D7	29	E2	18	18	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	C7	30	D1	19	19	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1	-
43	C6	31	C1	20	20	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2	-
44	C8	32	C2	21	21	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	-

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 31*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 17: Voltage characteristics*

Table 31. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB	BusMatrix(1)	5	µA/MHz
	DMA1	7	
	SRAM	1	
	Flash memory interface	14	
	CRC	2	
	GPIOA	9	
	GPIOB	12	
	GPIOC	2	
	GPIOD	1	
	GPIOF	1	
	TSC	6	
	All AHB peripherals	**55**	

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 32* are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop or Standby mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode. The wakeup source from Standby mode is the WKUP1 pin (PA0).

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 32. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @$V_{DD} = V_{DDA}$					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	3.2	3.1	2.9	2.9	2.8	5	µs
		Regulator in low power mode	7.0	5.8	5.2	4.9	4.6	9	
$t_{WUSTANDBY}$	Wakeup from Standby mode	-	60.4	55.6	53.5	52	51	-	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4 SYSCLK cycles					-	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

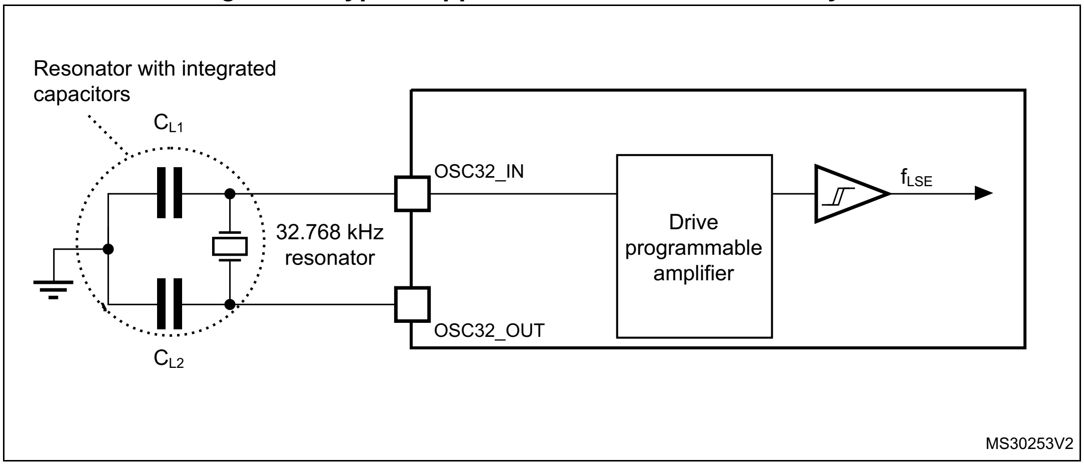
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15: High-speed external clock source AC timing diagram*.

Table 33. High-speed external user clock characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI) RC oscillator

Table 37. HSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1[2]	%
$DuCy_{(HSI)}$	Duty cycle	-	45[2]	-	55[2]	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8[3]	-	3.8[3]	%
		T_A = -10 to 85°C	-1.9[3]	-	2.3[3]	
		T_A = 0 to 85°C	-1.9[3]	-	2[3]	
		T_A = 0 to 70°C	-1.3[3]	-	2[3]	
		T_A = 0 to 55°C	-1[3]	-	2[3]	
		T_A = 25°C[4]	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1[2]	-	2[2]	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100[2]	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 19. HSI oscillator accuracy characterization results for soldered parts

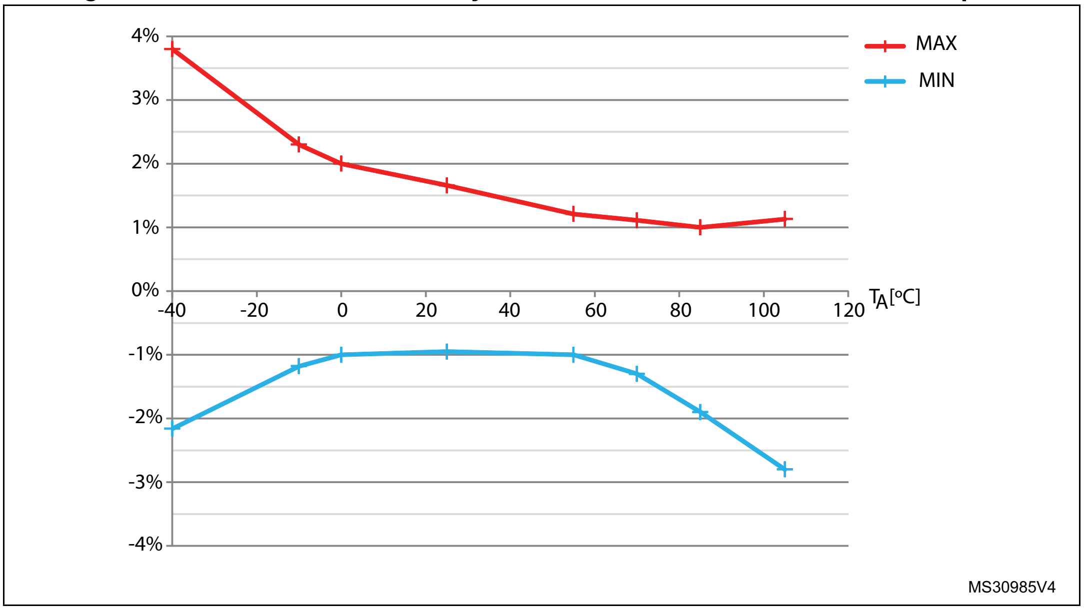


Table 47. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on PA10, PA12, PB4, PB5, PB10, PB15 and PD2 pins with induced leakage current on adjacent pins less than –10 µA	–5	NA	
	Injected current on all other FT and FTf pins	–5	NA	
	Injected current on PA6 and PC0	–0	+5	
	Injected current on all other TTa, TC and RST pins	–5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 20: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 48. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	0.3 V_{DDIOx}+0.07(1)	V
		FT and FTf I/O	-	-	0.475 V_{DDIOx}–0.2(1)	
		BOOT0	-	-	0.3 V_{DDIOx}–0.3(1)	
		All I/Os except BOOT0 pin	-	-	0.3 V_{DDIOx}	
V_{IH}	High level input voltage	TC and TTa I/O	0.445 V_{DDIOx}+0.398(1)	-	-	V
		FT and FTf I/O	0.5 V_{DDIOx}+0.2(1)	-	-	
		BOOT0	0.2 V_{DDIOx}+0.95(1)	-	-	
		All I/Os except BOOT0 pin	0.7 V_{DDIOx}	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(1)	-	mV
		FT and FTf I/O	-	100(1)	-	
		BOOT0	-	300(1)	-	

Table 48. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current(2)	TC, FT and FTf I/O TTa in digital mode $V_{SS} \leq V_{IN} \leq V_{DDIOx}$	-	-	± 0.1	µA
		TTa in digital mode $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O $V_{DDIOx} \leq V_{IN} \leq 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	$V_{IN} = - V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 47: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 21* for standard I/Os, and in *Figure 22* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 21. TC and TTa I/O input characteristics

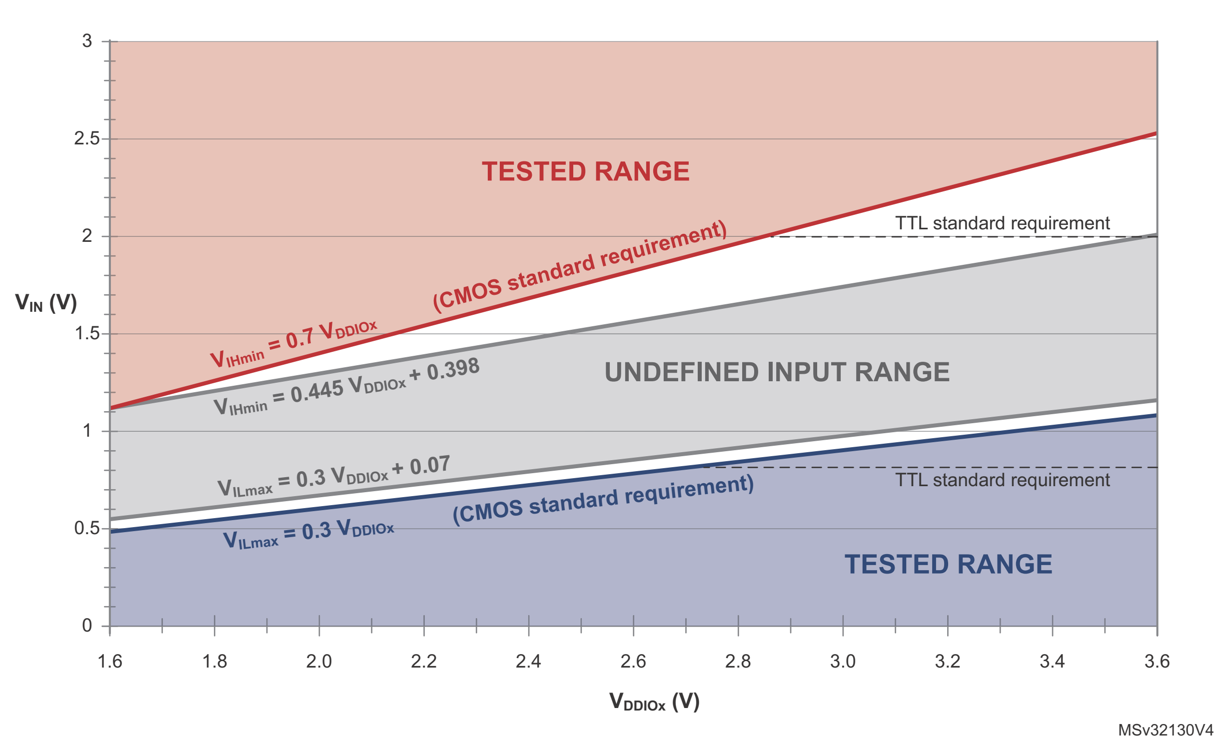


Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics

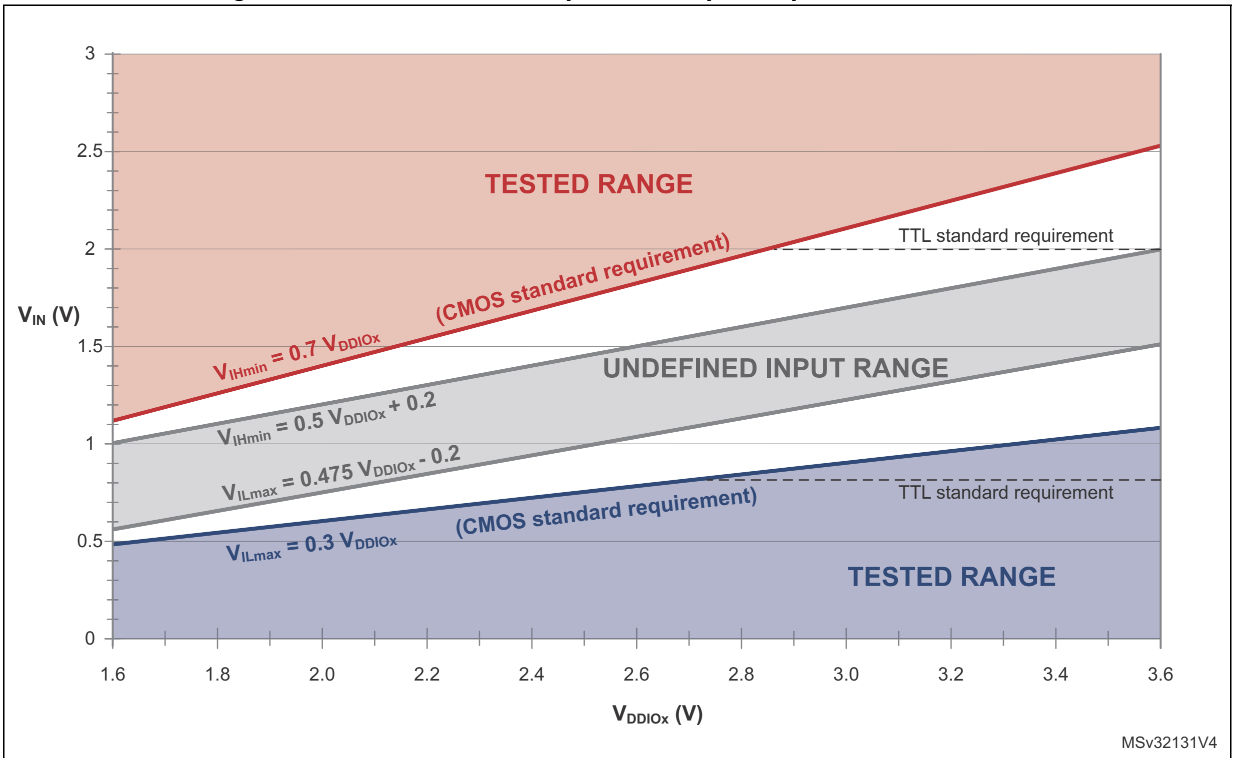
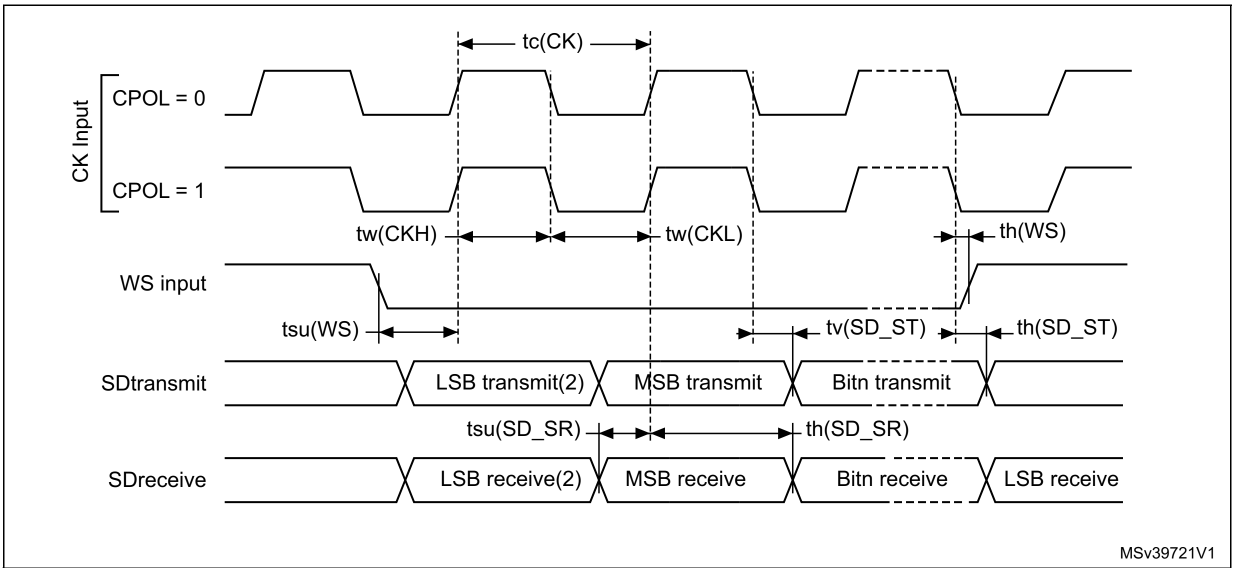


Table 64. I²S characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$(2)	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$(2)		Slave receiver	0.5	-	
$t_{v(SD\_MT)}$(2)	Data output valid time	Master transmitter	-	4	
$t_{v(SD\_ST)}$(2)		Slave transmitter	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter	0	-	
$t_{h(SD\_ST)}$		Slave transmitter	13	-	

1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then T_{PCLK} = 1/f_{PLCLK} = 125 ns.

Figure 32. I²S slave timing diagram (Philips protocol)



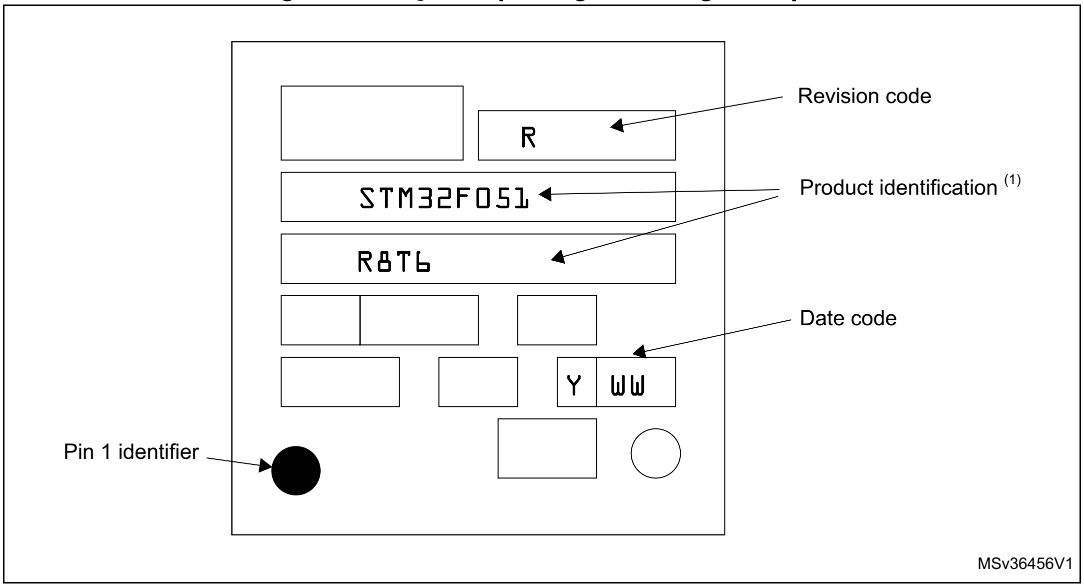
1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 39. LQFP64 package marking example



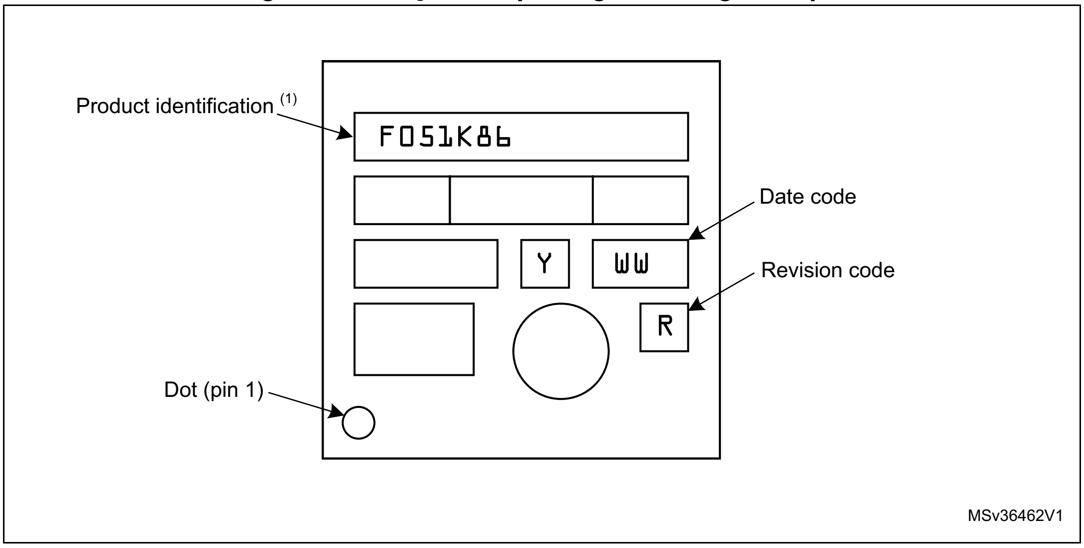
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 54. UFQFPN32 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.8 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 20: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 74. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP32 - 7 × 7 mm	56	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm	65	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	
	Thermal resistance junction-ambient UFQFPN32 - 5 × 5 mm	38	
	Thermal resistance junction-ambient WLCSP36 - 2.6 × 2.7 mm	60	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 75. Ordering information scheme

Example: STM32 F 051 R 8 T 6 x

Device family
STM32 = ARM-based 32-bit microcontroller

Product type
F = General-purpose

Sub-family
051 = STM32F051xx

Pin count
K = 32 pins
T = 36 pins
C = 48 pins
R = 64 pins

User code memory size
4 = 16 Kbyte
6 = 32 Kbyte
8 = 64 Kbyte

Package
H = UFBGA
T = LQFP
U = UFQFPN
Y = WLCSP

Temperature range
6 = –40 °C to +85 °C
7 = –40 °C to +105 °C

Options
xxx = code ID of programmed parts (includes packing type)
TR = tape and reel packing
blank = tray packing