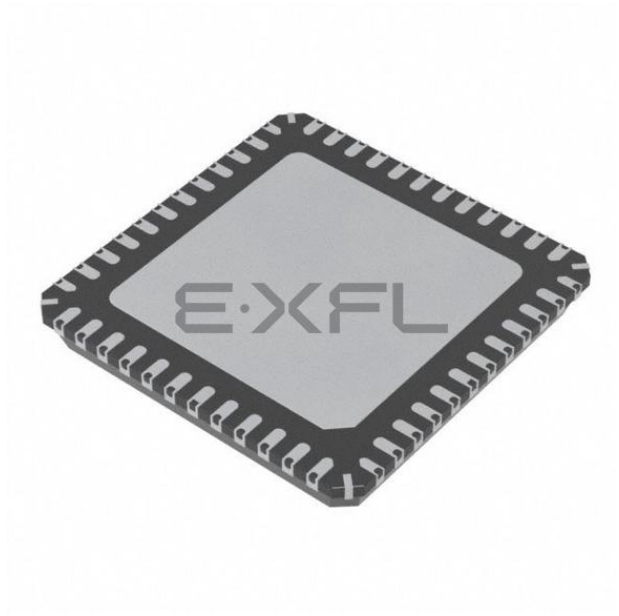

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Not For New Designs
Applications	Automotive
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (48kB)
Controller Series	-
RAM Size	4K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	3V ~ 28V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9845qxxuma1

Table of Contents

4 Modes of Operation

This highly integrated circuit contains analog and digital functional blocks. For system and interface control an embedded 32-Bit Cortex-M0 microcontroller is included. For internal and external power supply purposes, on-chip low drop-out regulators are existent. An internal oscillator (no external components necessary) provides a cost effective and suitable clock in particular for LIN slave nodes. As communication interface, a LIN transceiver and several High Voltage Monitor Inputs with adjustable threshold and filters are available. Furthermore two High-Sides Switches (e.g. for driving LEDs or powering of switches), two low-side switches (e.g. for relays) and several general purpose input/outputs (GPIO) with pulse-width modulation (PWM) capabilities are available.

The Micro Controller Unit supervision and system protection including reset feature is controlled by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support terminal 30 connected automotive applications. A wake-up from the power saving mode is possible via a LIN bus message, via the monitoring inputs or repetitive with a programmable time period (cyclic wake-up).

The integrated circuit is available in a package with 0.5 mm pitch and is designed to withstand the challenging conditions of automotive applications.

The TLE9845QX has several operational modes mainly to support low power consumption requirements. The low power modes and state transitions are depicted in **Figure 3** below.

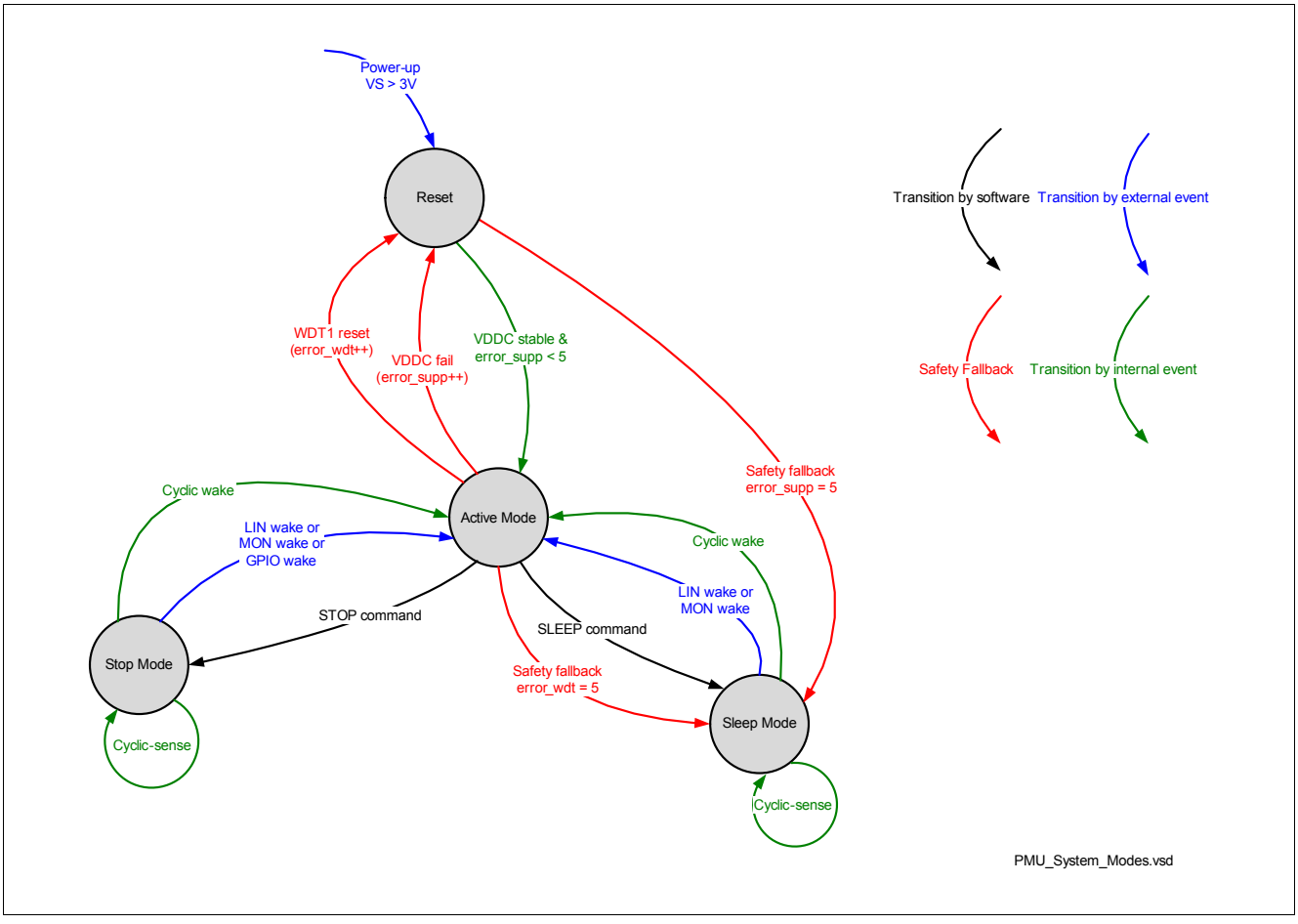

Figure 3 Power Control State Diagram

ICU (Interrupt Control Unit)

- PREWARN_SUP_NMI = generation of Prewarn-Supply NMI
- PREWARN_CLK_INT = generation of Prewarn-Clock Watchdog NMI
- INT = generation of MISC interrupts

The on-chip memory modules available in the TLE9845QX are:

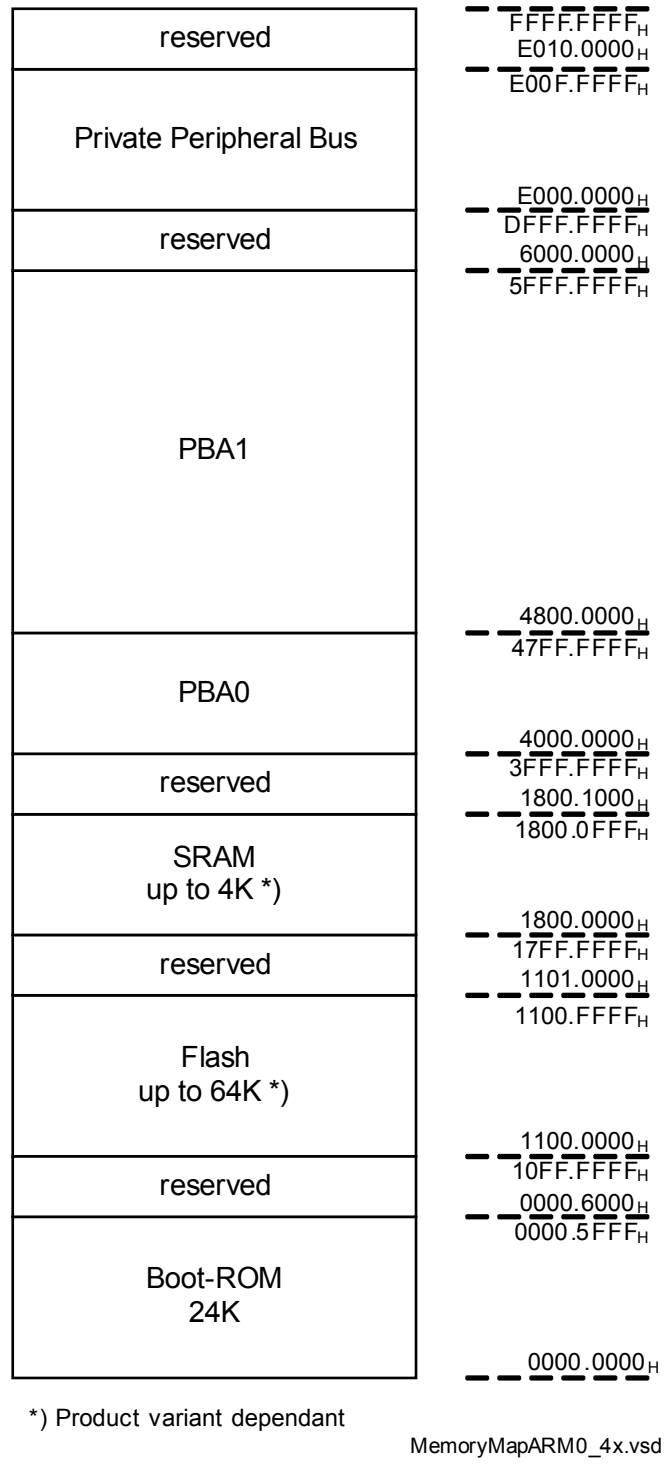

Figure 17 TLE9845QX Memory Map

Table 6 Interrupt Vector Table (cont'd)

Service Request	Node ID	Description
MONx	22	MONx Interrupt, wakeup
Port 2.x	23	Port 2.x - DPP1

Table 7 NMI Interrupt Table

Service Request	Node	Description
PLL NMI	NMI	PLL Loss-of-Lock
NVM Operation Complete NMI	NMI	NVM Operation Complete
Overtemperature NMI	NMI	System Overtemperature
Oscillator Watchdog NMI	NMI	Oscillator Watchdog and MI_CLK Watchdog Timer Overflow
NVM Map Error NMI	NMI	NVM Map Error
ECC Error NMI	NMI	RAM / NVM Uncorrectable ECC Error
Supply Prewarning NMI	NMI	Supply Prewarning

14.2.1 Port 0 and Port 1

Figure 21 shows the block diagram of an TLE9845QX bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin.

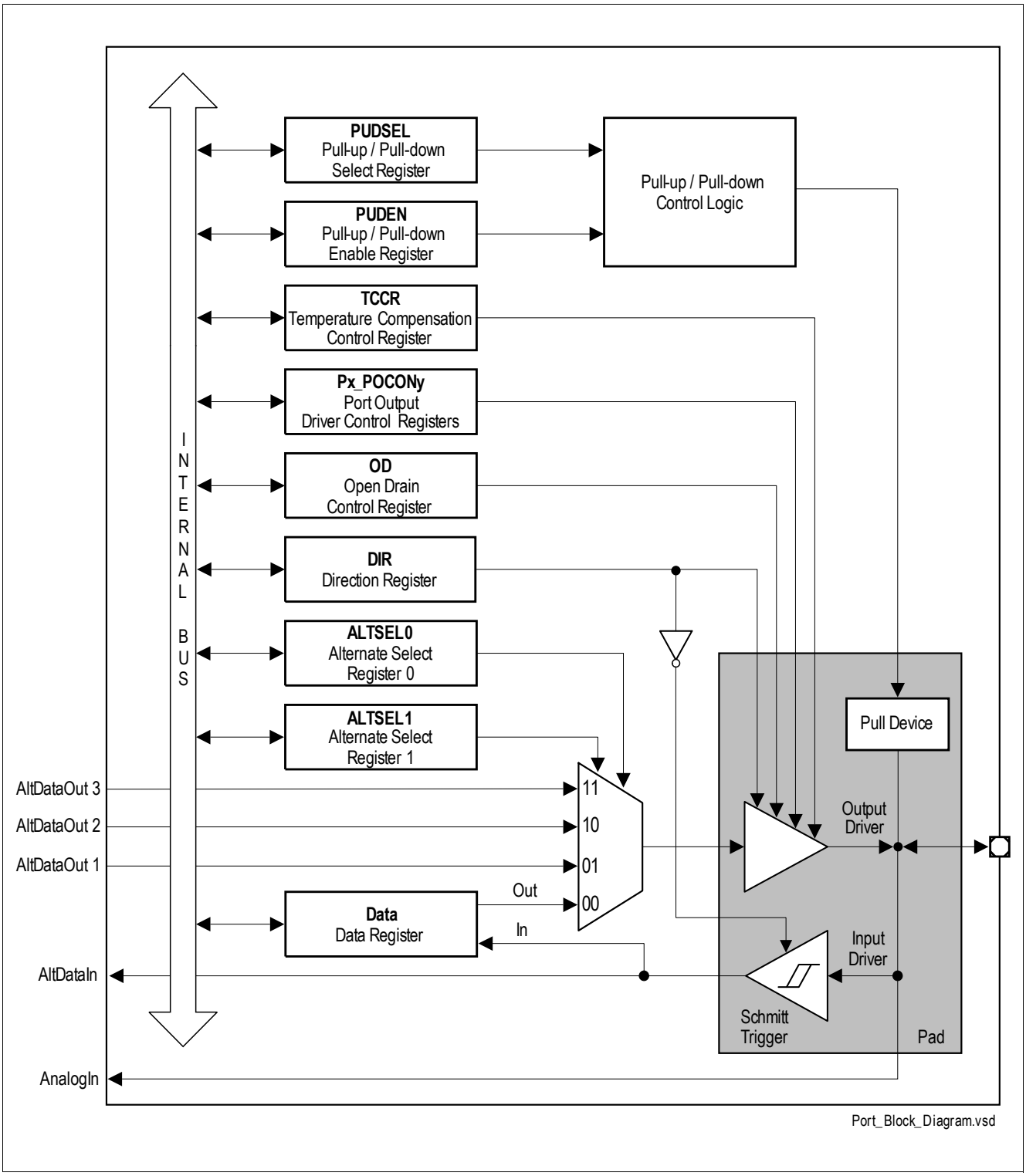

Figure 21 General Structure of Bidirectional Port

Table 8 Port 0 Input/Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.5	Input	GPI	P0_DATA.P5	
		INP1	SSC1_M_MRST	SSC1
		INP2	EXINT0_0	SCU
		INP3	T21EX_2	Timer 21
		INP4	T5INA	GPT12
		INP5	CCPOS2_1	CCU6
	Output	GPO	P0_DATA.P5	
		ALT1	SSC1_S_MRST	SSC1
		ALT2	COUT60_0	CCU6
		ALT3	LIN_RXD	LIN

14.3.2 Port 1

14.3.2.1 Port 1 Functions

Port 1alternate function mapping according **Table 9**

Table 9 Port 1 Input / Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.0	Input	GPI	P1_DATA.P0	
		INP1	T3INC	GPT12
		INP2	CC61_0	CCU6
		INP3	SSC2_S_SCK	SSC2
		INP4	T4EUDB	GPT12
	Output	GPO	P1_DATA.P0	
		ALT1	SSC2_M_SCK	SSC2
		ALT2	CC61_0	CCU6
		ALT3	UART2_TXD	UART2
P1.1	Input	GPI	P1_DATA.P1	
		INP1	T6EUDA	GPT12
		INP2	T5INB	GPT12
		INP3	T3EUDC	GPT12
		INP4	SSC2_S_MTSR	SSC2
		INP5	T21EX_3	Timer 21
		INP6	UART2_RXD	UART2
	Output	GPO	P1_DATA.P1	
		ALT1	SSC2_M_MTSR	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	EXF21_1	Timer 21
P1.2	Input	GPI	P1_DATA.P2	
		INP1	EXINT0_1	SCU
		INP2	T21_1	Timer 21
		INP3	T2INA	GPT12
		INP4	SSC2_M_MRST	SSC2
		INP5	CCPOS2_2	CCU6
	Output	GPO	P1_DATA.P2	
		ALT1	SSC2_S_MRST	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT_1	GPT12

21 Measurement Unit

21.1 Features

- 1 x 10 Bit ADC with 13 Inputs including attenuator allowing measurement of high voltage input signals
- Supply Voltage Attenuators with attenuation of **VBAT_SENSE, VS, MONx, P2.x**.
- 1 x 8 Bit ADC with 7 Inputs including attenuator allowing measurement of high voltage input signals
- Supply Voltage Attenuators with attenuation of **VS, VDDEXT, VDDP**, **VBG, VDDC, TSENSE_LS, TSENSE_CENTRAL**.
- VBG monitoring of 8 Bit ADC to support functional safety requirements.
- Temperature Sensor for monitoring the chip temperature and Low Side module temperature.
- Supplement Block with Reference Voltage Generation, Bias Current Generation, Voltage Buffer for NVM Reference Voltage, Voltage Buffer for Analog Module Reference Voltage and Test Interface.

21.2 Introduction

The measurement unit is a functional unit that comprises the following associated sub-modules:

Table 13 Measurement functions and associated modules

Module Name	Modules	Functions
Central Functions Unit	Bandgap reference circuit + current reference circuit	The bandgap-reference sub-module provides two reference voltages 1. an accurate reference voltage for the 10-bit and 8-bit ADCs. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the NVM module
10 Bit ADC (ADC1)	10-bit ADC module with 13 multiplexed analog inputs	VBAT_SENSE, VS and MONx measurement. Six (5V) analog inputs from Port 2.x
8 Bit ADC (ADC2)	8-bit ADC module with 7 multiplexed inputs	VS/VDDEXT/VDDP/VBG/VDDC/TSENSE_LS and TSENSE_CENTRAL measurement.
Temperature Sensor	Temperature sensor readout amplifier with two multiplexed ΔVbe-sensing elements	Generates outputs voltage which is a linear function of the local chip (Tj) temperature.
Measurement Core Module	Digital signal processing and ADC control unit	1. Generates the control signal for the 8-bit ADC 2 and the synchronous clock for the switched capacitor circuits (temperature sensor) 2. Performs digital signal processing functions and provides status outputs for interrupt generation.

21.2.1 Block Diagram

The Structure of the Measurement Functions Module is shown in the following figure.

23.2 Introduction

23.2.1 Block Diagram

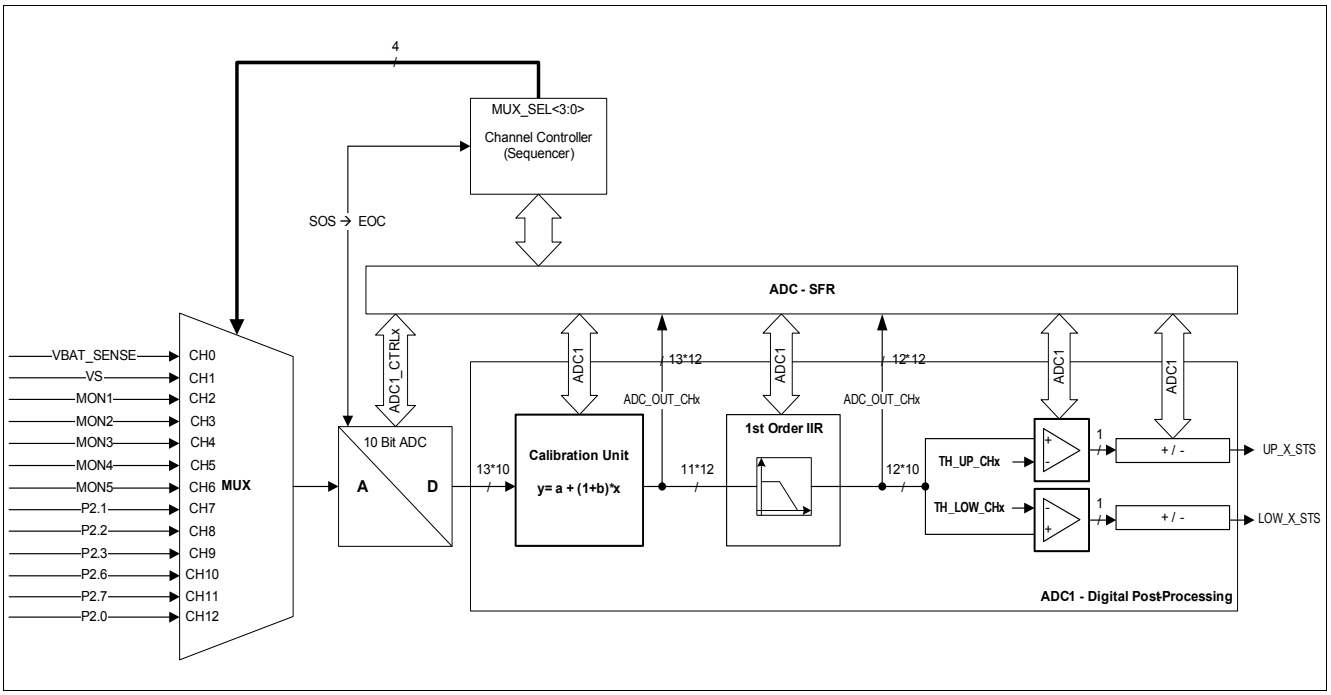

Figure 31 Module Block Diagram

27 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

27.1 Relay Window Lift Application diagram

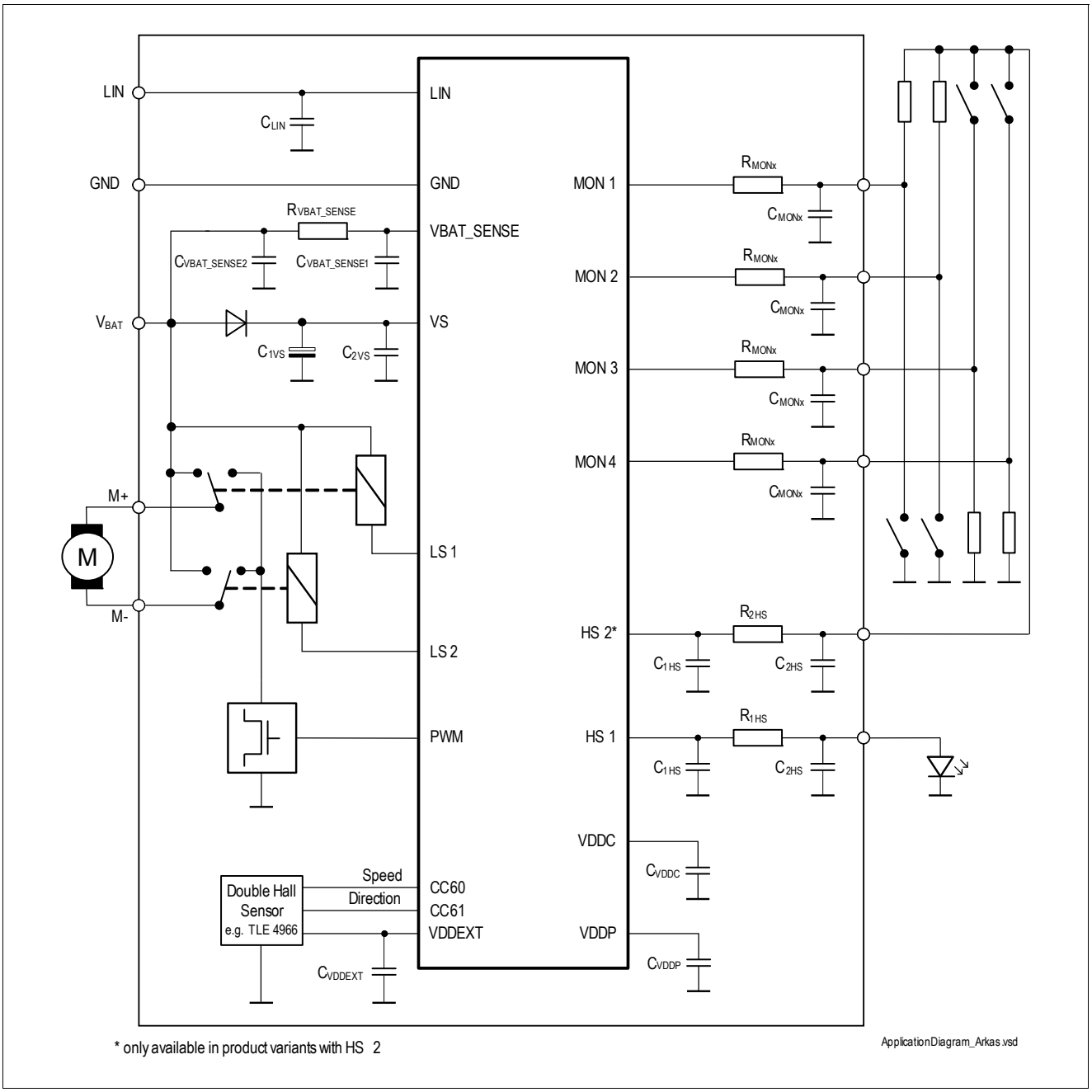

Figure 35 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the actual application.

For adjusting the required slope of the output voltage the resistors between the outputs HSx/LSx and the power MOSFET gate have to be dimensioned in a specific way according to the application requirements. It's further recommended to additionally connect the respective gate potentials to battery (P-channel) or ground (N-channel) by external resistors. This prevents the power half bridge from unwanted cross currents in case of a TLE9845QX reset condition (driver stage is high impedance).

27.2.2.2 PWM operation

TLE9845QX supports PWM controlled motor drive with active free-wheeling (i.e. synchronous switching of the half bridge MOSFETs to avoid body diode losses during PWM off phase) by using the CCU6 module.

The CCU6 can be configured to use the internal deadtime generation to control the switching delay between the external P-and N-channel MOSFETs of the half-bridge. In this case HSx and LSx are switched without any deadtime. The gate pre resistors has to be dimensioned expecting the max values.

27.2.2.3 MOSFET protection with integrated Differential Units for drain-source-monitoring

For emergency shut-off in case of short-to-GND or short-to-VBAT, the following protection scheme can be used.

For this feature, 3 of the MON inputs (e.g. MON1, MON2, MON4) are used in combination with 2 differential measurement units (MON1-MON2, MON2-MON4), that are located in ADC1.

The differential measurement units are sampled by the ADC1 and use the post processing for threshold supervision, interrupt generation and trap handling.

The ADC measurements are triggered from CCU6, i.e. aligned to the PWM signals.

27.3 Connection of N.C.

The device contains several N.C. (not connected, no bond wire).

Table 15 Recommendation for connecting N.C. / N.U. pins

type	pin number	recommendation 1	recommendation 2	comment
N.C.	27, 28, 29, 38, 40, 41	GND		
N.C.	10, 46	open	GND	neighboring high-voltage pins

27.4 Connection of unused pins

Table 16 shows recommendations how to connect pins, in case they are not needed by the application.

Table 16 Recommendation for connecting unused pins

type	pin number	recommendation 1 (if unused)	recommendation 2 (if unused)
LIN	1	open	
HS1, HS2	3, 4	VS	open
MON	5, 6, 7, 8, 9	GND	open + configure internal PU/PD
LS1, LS2	11, 12	GNDLS	open
GPIO	14, 15, 16, 17, 20, 22, 23, 24, 25, 26, 33, 34, 35, 36, 37, 39	GND	external PU/PD or open + configure internal PU/PD

Table 20 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in Sleep Mode (extended Voltage and Temperature Range 2)	$I_{Sleep(V\_T\_extend2)}$	–	–	40	µA	System in Sleep Mode, microcontroller not powered, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND: T_J = -40°C to 85°C; V_s = 3V to 28V	P_1.3.7
Current consumption in Sleep Mode with cyclic wake	I_{Cyclic}	–	–	15	µA	T_J = -40°C to 25°C; V_s = 13.5V during sleep period	P_1.3.5
Current consumption in Sleep Mode with cyclic wake (extended Temperature Range)	$I_{Cyclic(T\_extend)}$	–	–	30	µA	T_J = 25°C to 85°C; V_s = 13.5V; during sleep period	P_1.3.6
Current consumption in Stop Mode	I_{Stop}	–	65	115	µA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; T_J = -40°C to 85°C	P_1.3.19
Current consumption in Stop Mode	$I_{Stop\_V\_extend}$	–	3.5	4.0	mA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; T_J = -40°C to 85°C; V_s = 3V	P_1.3.21
Current consumption in Stop Mode with cyclic sense	I_{Stop_CS}	–	70	125	µA	System in Stop Mode (during stop period), microcontroller not clocked, Wake capable via LIN and MON; VDDEXT off; High Side off; GPIOs open (no loads) or connected to GND or VDDP; T_J = -40°C to 85°C; V_s = 5.5V to 28V	P_1.3.20

1) Not subject to production test, specified by design

28.1.4 Thermal Resistance

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Under Voltage Reset	V_{DDPUV}	2.55	2.7	2.8	V	–	P_2.1.10
Over Current Diagnostic	I_{VDDPOC}	90	–	200	mA	current including VDDC current consumption	P_2.1.11

1) currents used in this table are positive but flowing out the pin VDDP
2) Specified output current for port supply and additional other external loads connected to VDDP, excluding on-chip current consumption.
3) only min. value is tested.
4) the total capacitance on VDDP must not exceed 2,2 µF
5) Not subject to production test, specified by design.
6) Load current includes internal supply.
7) Output drop for I_{VDDP} plus internal supply

28.2.5 VPRE Voltage Regulator (PMU Subblock) Parameters

The PMU VPRE Regulator acts as a supply of VDDP and VDDC voltage regulators.

Table 27 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified Output Current	I_{VPRE}	–	–	90	mA	1)	P_2.4.1

1) Not subject to production test, specified by design.

28.2.5.1 Load Sharing of VPRE Regulator

The figure below shows the load sharing concept of VPRE regulator.

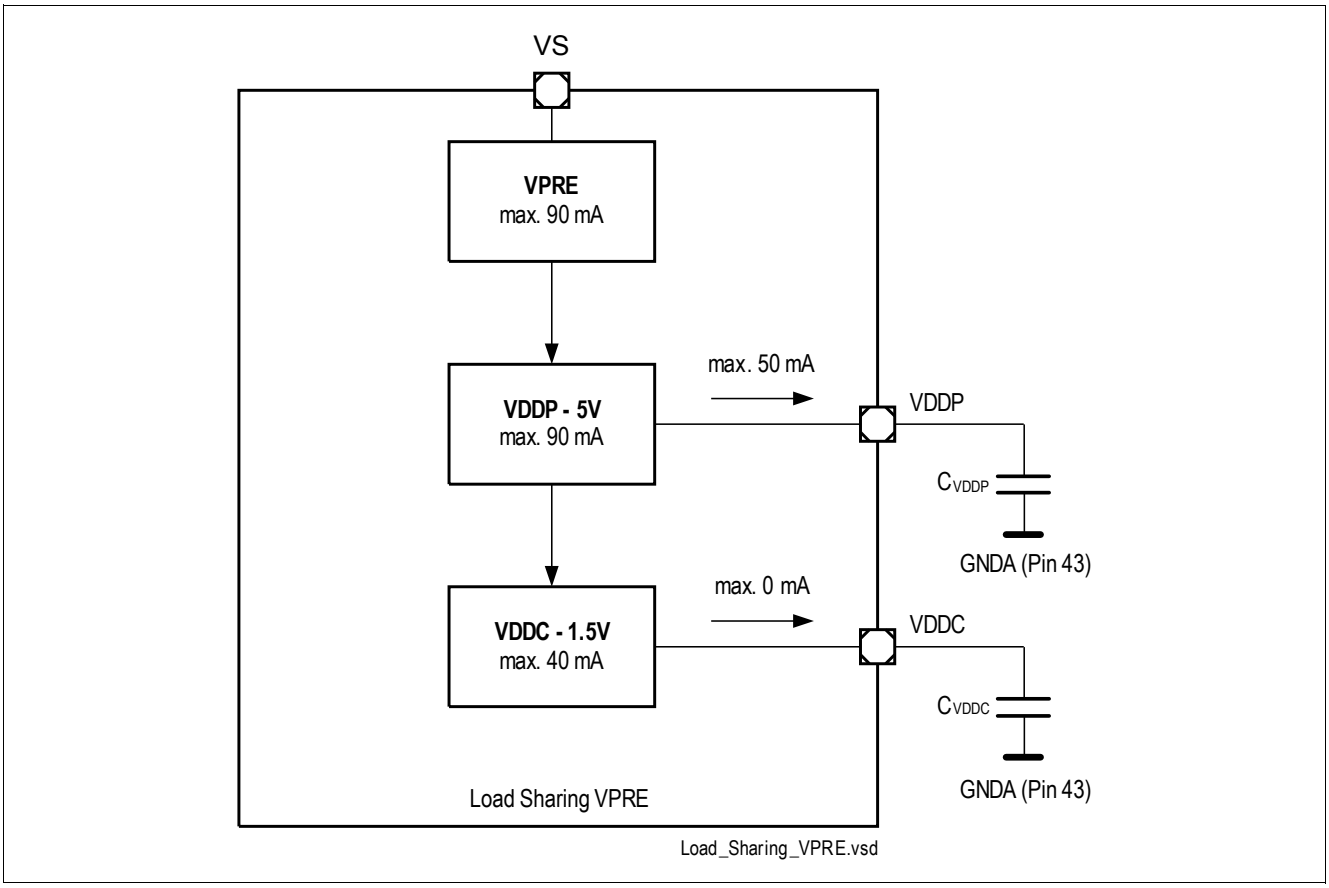

Figure 37 Load Sharing of VPRE Regulator

28.3 System Clocks

28.3.1 Electrical Characteristics Oscillators and PLL

Table 29 Electrical Characteristics System Clocks

V_S = 5.5 V to 28 V,, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
PMU Oscillators (Power Management Unit)							
Frequency of LP_CLK	f_{LP_CLK}	17	20	23	MHz	this clock is used at startup and can be used in case the PLL fails	P_3.1.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	this clock is used for cyclic wake	P_3.1.2
CGU Oscillator (Clock Generation Unit Microcontroller)							
Short term frequency deviation[1)]	f_{TRIMST}	-0.4%	–	+0.4%	MHz	within any 100 ms, e.g. after synchronization to a LIN frame (includes PLL accumulated jitter value).Assuption: T_j is varying < 30°C.	P_3.1.3
Absolute accuracy	$f_{TRIMABSA}$	-1.49%	–	+1.49%	MHz	Including temperature& lifetime drift and supply variation	P_3.1.4
CGU-OSC Start-up time	t_{OSC}	–	–	10	µs	[2)] startup time OSC from Sleep Mode, power supply stable	P_3.1.5
PLL (Clock Generation Unit Microcontroller) [2)]							
VCO reference frequency range	f_{REF}	0.8	1	1.25	MHz		P_3.1.25
VCO frequency (tuning) range	f_{VCO}	75	–	160	MHz		P_3.1.21
Input frequency range	f_{OSC}	4	–	6	MHz	see also specified limits for f_{VCO} and f_{REF} resulting in restrictions for possible N divider settings	P_3.1.6
XTAL1 input freq. range	f_{OSCHP}	4	–	6	MHz	see also specified limits for f_{VCO} and f_{REF} resulting in restrictions for possible N divider settings	P_3.1.23
Output freq. range	f_{PLL}	15	–	40	MHz	see also specified limits for f_{VCO} and f_{REF} resulting in restrictions for possible N divider settings	P_3.1.7
Free-running frequency	$f_{VCOfree}$	–	34	–	MHz		P_3.1.24

Table 29 Electrical Characteristics System Clocks (cont'd)

V_S = 5.5 V to 28 V,, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input clock high/low time	$t_{high/low}$	10	–	–	ns		P_3.1.8
Peak period jitter	t_{jp}	-500	–	500	ps	for K=2; this parameter value is only valid with the combination of an external quartz oscillator (e.g. 5 MHz)	P_3.1.9
Accumulated jitter with external oscillator	jacc_ext	–	–	5	ns	for K=2; this parameter value is only valid with the combination of an external quartz oscillator (e.g. 5 MHz).	P_3.1.10
Lock-in time	t_L	–	–	260	µs	this parameter represents the duration from module power-on to assertion of lock signal	P_3.1.11

1) The typical oscillator frequency is 40 MHz

2) Not subject to production test, specified by design.

28.3.2 External Clock Parameters XTAL1, XTAL2

Table 30 Functional Range

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range limits for signal on XTAL1	V_{IX1_SR}	-1.7 + V_{DDC}	–	1.7	V	2)	P_3.2.1
Input voltage (amplitude) on XTAL1	V_{AX1_SR}	0.3 x V_{DDC}	–	–	V	3) Peak-to-peak voltage	P_3.2.2
XTAL1 input current	I_{IL}	–	–	±20	µA	0 V < V_{IN} < V_{DDI}	P_3.2.3
Oscillator frequency	f_{OSC}	4	–	6	MHz	Clock signal	P_3.2.4
Oscillator frequency	f_{OSC}	4	–	6	MHz	Crystal or Resonator	P_3.2.5
High time	t_{1_VCOBYP}	6	–	–	ns	4)5)	P_3.2.6
Low time	t_{2_VCOBYP}	6	–	–	ns	4)5)–	P_3.2.7
Rise time	t_{3_VCOBYP}	–	8	8	ns	4)5)–	P_3.2.8
Fall time	t_{4_VCOBYP}	–	8	8	ns	4)5)–	P_3.2.9
High time	t_{1_PLLNM}	12	–	–	ns	5)6)–	P_3.2.10

Table 34 DC Characteristics Port 2 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pull level force current[4]	I_{PLF_P2}	±750	–	–	µA	[3] VPIN ≤ VIL (up) VPIN ≥ VIH (dn)	P_5.3.6
Pin capacitance (digital inputs/outputs)	C_{IO_P2}	–	–	10	pF	[2]	P_5.3.7

1) Tested at V_{DDP} = 5V, specified for 4.9V < V_{DDP} < 5.1V.

2) Not subject to production test, specified by design.

3) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.

4) Negative current is representing pullup; positive current is representing pulldown

28.5.4 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the TLE9845QX. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Table 35 Operating Condition Parameters

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Digital core supply voltage	V_{DDC}	1.35	–	1.6	V	Full active mode	P_5.4.1
Digital supply voltage for IO pads	V_{DDP}	2.55	5.0	5.5	V	[1]	P_5.4.2
Digital ground voltage	V_{SS}	0	–	0	V	Reference voltage	P_5.4.3
Overload current	I_{OV}	- 5.0	–	5.0	mA	Per IO pin[2)3)]	P_5.4.4
Overload current	I_{OV}	- 2.0	–	5.0	mA	Per analog input pin[2)3)]	P_5.4.5
Overload positive current coupling factor for analog inputs[4]	K_{OVA}	–	1.0×10^{-6}	1.0×10^{-4}	–	$I_{OV} > 0$[3]	P_5.4.6
Overload negative current coupling factor for analog inputs	K_{OVA}	–	2.5×10^{-4}	1.5×10^{-3}	–	$I_{OV} < 0$[3]	P_5.4.7
Overload positive current coupling factor for digital I/O pins	K_{OVD}	–	1.0×10^{-4}	5.0×10^{-3}	–	$I_{OV} > 0$[3]	P_5.4.8
Overload negative current coupling factor for digital I/O pins	K_{OVD}	–	1.0×10^{-2}	3.0×10^{-2}	–	$I_{OV} < 0$[3]	P_5.4.9
Absolute sum of overload currents	$\Sigma\lvert I_{OV}\rvert$	–	–	80	mA	[3]	P_5.4.10

Table 38 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ADC2 - Reference Voltage Measurement V_{BG}							
Input-to-output voltage attenuation: VBG	ATT_{VBG}	–	0.75	–		–	P_8.1.6
Nominal operating input voltage range VBG	$V_{BG,range}$	0.8	–	VDDC - 0.1V	V	2) Max. value corresponds to typ. ADC full scale input;	P_8.1.7
Value of ADC2-V_{BG} measurement after calibration	V_{BG_PMU}	0.90	1.0	1.1	V	–	P_8.1.39
ADC2 - Core supply Voltage Measurement V_{DDC}							
Input-to-output voltage attenuation: VDDC	ATT_{VDDC}	–	0.75	–		–	P_8.1.8
Nominal operating input voltage range VDDC	$V_{DDC,range}$	0.6	–	VDDC + 0.1V	V	2) Max. value corresponds to typ. ADC full scale input;	P_8.1.9

1) This typical theoretical full scale is not reached as the internal ESD Clamping Structure limits the voltage to max. 5.2V.

2) Not subject to production test, specified by design.

30 Revision History

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Rev. 1.0, 2016-05-06	
	Initial revision