# Infineon Technologies - C161OLM3VHABXUMA1 Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | EBI/EMI, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 63 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-QFP |
| Supplier Device Package | P-MQFP-80-1 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/c161olm3vhabxuma1 |

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Data Sheet, V2.0, Jan. 2001

# C161K
# C161O

## 16-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

**Revision History:** **2001-01** V2.0

Previous Version: 03.97 (Preliminary)
09.96 (Advance Information)

| Page | Subjects (major changes since last revision) |
|---|---|
| All | Converted to Infineon layout |
| All | C161V removed |
| 2 | Ordering Codes and Cross-Reference replaced with Derivative Synopsis |
| 5 - 8 | Open drain functionality described for P2, P3, P6 |
| 8 | Bidirectional reset introduced |
| 19 | Figure updated |
| 28, 29 | Revised description of Absolute Max. Ratings and Operating Conditions |
| 32 - 56 | Specifications for reduced supply voltage introduced |
| 35 | Reduced power consumption |
| 36, 37 | Clock Generation Modes added |
| 38, 39 | Description of External Clock Drive improved |
| 41 - 56 | Standard 25-MHz timing introduced (timing granularity 2 ns) |

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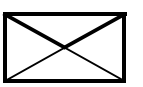
**mcdocu.comments@infineon.com**



## Pin Configuration MQFP Package
(top view)

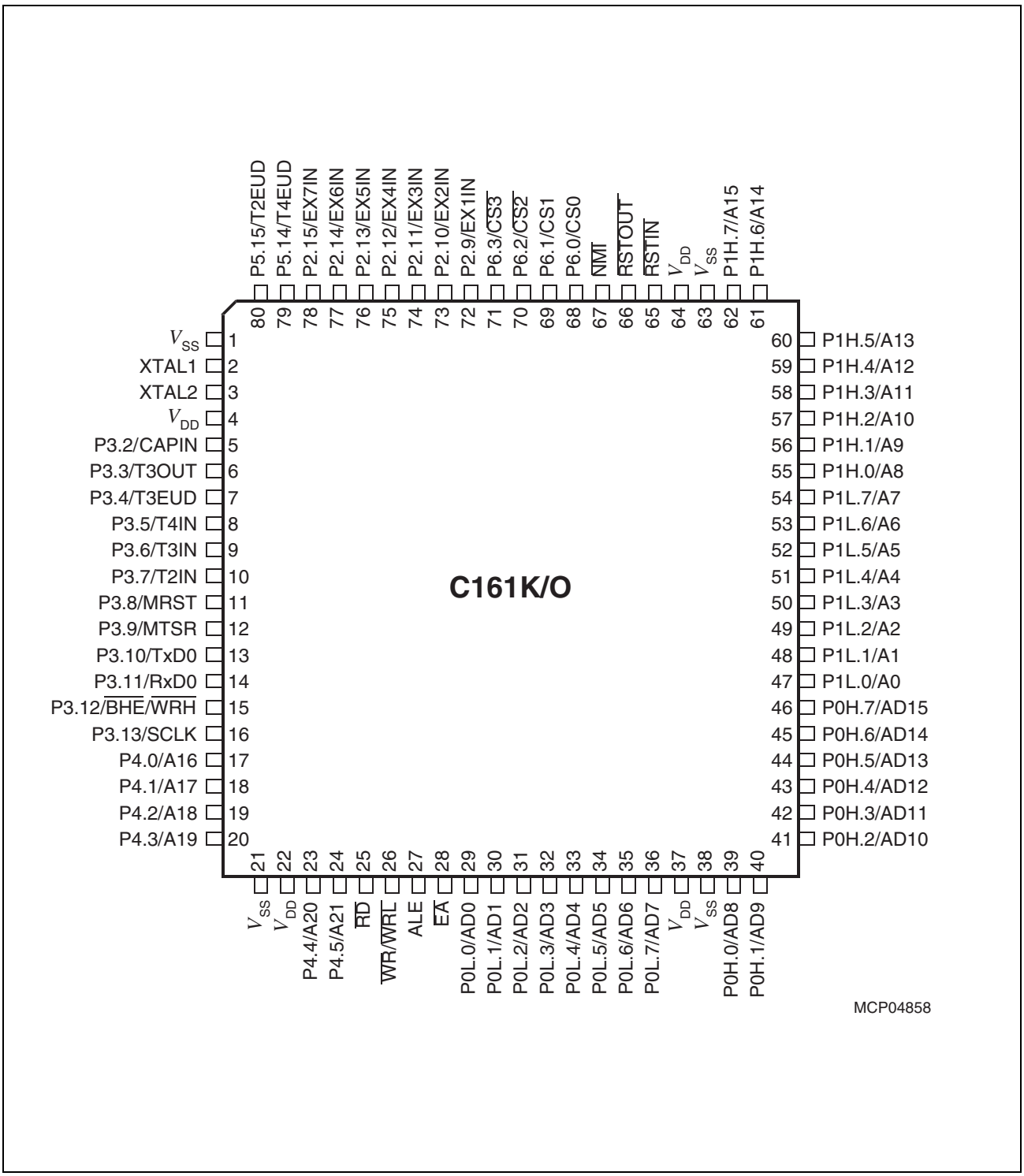



**Figure 2**

*Note: The **marked** signals are **only available in the C161O**.*
*Please also refer to the detailed description below (shaded lines).*

**Table 2 Pin Definitions and Functions**

| Symbol | Pin Num | Input Outp. | Function |
|---|---|---|---|
| XTAL1 | 2 | I | XTAL1: Input to the oscillator amplifier and input to the internal clock generator |
| XTAL2 | 3 | O | XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. |
| **P3** | | IO | Port 3 is a 12-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The Port 3 pins serve for following alternate functions: |
| P3.2 | 5 | I | CAPIN GPT2 Register CAPREL Capture Input<br>*This alternate input is **only available in the C161O**.* |
| P3.3 | 6 | O | T3OUT GPT1 Timer T3 Toggle Latch Output |
| P3.4 | 7 | I | T3EUD GPT1 Timer T3 External Up/Down Control Input |
| P3.5 | 8 | I | T4IN GPT1 Timer T4 Count/Gate/Reload/Capture Inp |
| P3.6 | 9 | I | T3IN GPT1 Timer T3 Count/Gate Input |
| P3.7 | 10 | I | T2IN GPT1 Timer T2 Count/Gate/Reload/Capture Inp |
| P3.8 | 11 | I/O | MRST SSC Master-Receive/Slave-Transmit Inp./Outp. |
| P3.9 | 12 | I/O | MTSR SSC Master-Transmit/Slave-Receive Outp./Inp. |
| P3.10 | 13 | O | TxD0 ASC0 Clock/Data Output (Async./Sync.) |
| P3.11 | 14 | I/O | RxD0 ASC0 Data Input (Async.) or Inp./Outp. (Sync.) |
| P3.12 | 15 | O | $\overline{\text{BHE}}$ External Memory High Byte Enable Signal, |
| | | O | $\overline{\text{WRH}}$ External Memory High Byte Write Strobe |
| P3.13 | 16 | I/O | SCLK SSC Master Clock Output / Slave Clock Input |
| **P4** | | IO | Port 4 is a 6-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines: |
| P4.0 | 17 | O | A16 Least Significant Segment Address Line |
| P4.1 | 18 | O | A17 Segment Address Line |
| P4.2 | 19 | O | A18 Segment Address Line |
| P4.3 | 20 | O | A19 Segment Address Line |
| P4.4 | 23 | O | A20 Segment Address Line |
| P4.5 | 24 | O | A21 Most Significant Segment Address Line |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num | Input Outp. | Function |
|---|---|---|---|
| $\overline{RD}$ | 25 | O | External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access. |
| $\overline{WR}$/ $\overline{WRL}$ | 26 | O | External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection. |
| ALE | 27 | O | Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes. |
| $\overline{EA}$ | 28 | I | External Access Enable pin. A low level at this pin during and after Reset forces the C161K/O to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'. |
| **PORT0**<br>P0L.0-7<br><br>P0H.0-7 | <br>29-36<br><br>39-46 | IO | PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes.<br>**Demultiplexed bus modes:**<br>Data Path Width: 8-bit 16-bit<br>P0L.0 – P0L.7: D0 – D7 D0 – D7<br>P0H.0 – P0H.7: I/O D8 – D15<br>**Multiplexed bus modes:**<br>Data Path Width: 8-bit 16-bit<br>P0L.0 – P0L.7: AD0 – AD7 AD0 – AD7<br>P0H.0 – P0H.7: A8 – A15 AD8 – AD15 |
| **PORT1**<br>P1L.0-7<br><br>P1H.0-7 | <br>47-54<br><br>55-62 | IO | PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num | Input Outp. | Function |
|---|---|---|---|
| $\overline{\text{RSTIN}}$ | 65 | I/O | Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C161K/O. An internal pullup resistor permits power-on reset using only a capacitor connected to $V_{SS}$. A spike filter suppresses input pulses < 10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles.<br>In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table.<br>*Note: To let the reset configuration of PORT0 settle a reset duration of ca. 1 ms is recommended.* |
| $\overline{\text{RST OUT}}$ | 66 | O | Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed. |
| $\overline{\text{NMI}}$ | 67 | I | Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C161K/O to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode.<br>If not used, pin $\overline{\text{NMI}}$ should be pulled high externally. |
| **P6** | | IO | Port 6 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers.<br>The Port 6 pins also serve for alternate functions: |
| P6.0 | 68 | O | $\overline{\text{CS0}}$ Chip Select 0 Output |
| P6.1 | 69 | O | $\overline{\text{CS1}}$ Chip Select 1 Output |
| P6.2 | 70 | O | $\overline{\text{CS2}}$ Chip Select 2 Output |
| P6.3 | 71 | O | $\overline{\text{CS3}}$ Chip Select 3 Output<br>*These chip select outputs are **only available in the C161O**.* |

**Table 3 C161K/O Interrupt Nodes**

| Source of Interrupt or PEC Service Request | Request Flag | Enable Flag | Interrupt Vector | Vector Location | Trap Number |
|---|---|---|---|---|---|
| External Interrupt 1 | CC9IR | CC9IE | CC9INT | $00'0064_H$ | $19_H$ |
| External Interrupt 2 | CC10IR | CC10IE | CC10INT | $00'0068_H$ | $1A_H$ |
| External Interrupt 3 | CC11IR | CC11IE | CC11INT | $00'006C_H$ | $1B_H$ |
| External Interrupt 4 | CC12IR | CC12IE | CC12INT | $00'0070_H$ | $1C_H$ |
| External Interrupt 5 | CC13IR | CC13IE | CC13INT | $00'0074_H$ | $1D_H$ |
| External Interrupt 6 | CC14IR | CC14IE | CC14INT | $00'0078_H$ | $1E_H$ |
| External Interrupt 7 | CC15IR | CC15IE | CC15INT | $00'007C_H$ | $1F_H$ |
| GPT1 Timer 2 | T2IR | T2IE | T2INT | $00'0088_H$ | $22_H$ |
| GPT1 Timer 3 | T3IR | T3IE | T3INT | $00'008C_H$ | $23_H$ |
| GPT1 Timer 4 | T4IR | T4IE | T4INT | $00'0090_H$ | $24_H$ |
| GPT2 Timer 5 | T5IR | T5IE | T5INT | $00'0094_H$ | $25_H$ |
| GPT2 Timer 6 | T6IR | T6IE | T6INT | $00'0098_H$ | $26_H$ |
| GPT2 CAPREL Reg. | CRIR | CRIE | CRINT | $00'009C_H$ | $27_H$ |
| ASC0 Transmit | S0TIR | S0TIE | S0TINT | $00'00A8_H$ | $2A_H$ |
| ASC0 Transmit Buffer | S0TBIR | S0TBIE | S0TBINT | $00'011C_H$ | $47_H$ |
| ASC0 Receive | S0RIR | S0RIE | S0RINT | $00'00AC_H$ | $2B_H$ |
| ASC0 Error | S0EIR | S0EIE | S0EINT | $00'00B0_H$ | $2C_H$ |
| SSC Transmit | SCTIR | SCTIE | SCTINT | $00'00B4_H$ | $2D_H$ |
| SSC Receive | SCRIR | SCRIE | SCRINT | $00'00B8_H$ | $2E_H$ |
| SSC Error | SCEIR | SCEIE | SCEINT | $00'00BC_H$ | $2F_H$ |

*Note: The shaded interrupt nodes are **only available in the C161O**, not in the C161K.*

### General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over-flow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

### Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 20 µs and 336 ms can be monitored (@ 25 MHz).
The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

### Parallel Ports

The C161K/O provides up to 63 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A21/19/17 … A16 in systems where segmentation is enabled to access more than 64 KBytes of memory.
Port 6 provides optional chip select signals.
Port 3 includes alternate functions of timers, serial interfaces, and the optional bus control signal $\overline{\text{BHE}}$/$\overline{\text{WRH}}$.
Port 5 is used for timer control signals.

**Table 5 Instruction Set Summary** (cont'd)

| Mnemonic | Description | Bytes |
|---|---|---|
| MOV(B) | Move word (byte) data | 2 / 4 |
| MOVBS | Move byte operand to word operand with sign extension | 2 / 4 |
| MOVBZ | Move byte operand to word operand. with zero extension | 2 / 4 |
| JMPA, JMPI, JMPR | Jump absolute/indirect/relative if condition is met | 4 |
| JMPS | Jump absolute to a code segment | 4 |
| J(N)B | Jump relative if direct bit is (not) set | 4 |
| JBC | Jump relative and clear bit if direct bit is set | 4 |
| JNBS | Jump relative and set bit if direct bit is not set | 4 |
| CALLA, CALLI, CALLR | Call absolute/indirect/relative subroutine if condition is met | 4 |
| CALLS | Call absolute subroutine in any code segment | 4 |
| PCALL | Push direct word register onto system stack and call absolute subroutine | 4 |
| TRAP | Call interrupt service routine via immediate trap number | 2 |
| PUSH, POP | Push/pop direct word register onto/from system stack | 2 |
| SCXT | Push direct word register onto system stack and update register with word operand | 4 |
| RET | Return from intra-segment subroutine | 2 |
| RETS | Return from inter-segment subroutine | 2 |
| RETP | Return from intra-segment subroutine and pop direct word register from system stack | 2 |
| RETI | Return from interrupt service subroutine | 2 |
| SRST | Software Reset | 4 |
| IDLE | Enter Idle Mode | 4 |
| PWRDN | Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low) | 4 |
| SRVWDT | Service Watchdog Timer | 4 |
| DISWDT | Disable Watchdog Timer | 4 |
| EINIT | Signify End-of-Initialization on RSTOUT-pin | 4 |
| ATOMIC | Begin ATOMIC sequence | 2 |
| EXTR | Begin EXTended Register sequence | 2 |
| EXTP(R) | Begin EXTended Page (and Register) sequence | 2 / 4 |
| EXTS(R) | Begin EXTended Segment (and Register) sequence | 2 / 4 |
| NOP | Null operation | 2 |

## Absolute Maximum Ratings

**Table 7 Absolute Maximum Rating Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Storage temperature | $T_{ST}$ | -65 | 150 | °C | – |
| Junction temperature | $T_J$ | -40 | 150 | °C | under bias |
| Voltage on $V_{DD}$ pins with respect to ground ($V_{SS}$) | $V_{DD}$ | -0.5 | 6.5 | V | – |
| Voltage on any pin with respect to ground ($V_{SS}$) | $V_{IN}$ | -0.5 | $V_{DD}$ + 0.5 | V | – |
| Input current on any pin during overload condition | – | -10 | 10 | mA | – |
| Absolute sum of all input currents during overload condition | – | – | \|100\| | mA | – |
| Power dissipation | $P_{DISS}$ | – | 1.5 | W | – |

*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
*During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on $V_{DD}$ pins with respect to ground ($V_{SS}$) must not exceed the values defined by the absolute maximum ratings.*

### Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C161K/O and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

**CC** (**C**ontroller **C**haracteristics):
The logic of the C161K/O will provide signals with the respective timing characteristics.

**SR** (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C161K/O.

### DC Characteristics (Standard Supply Voltage Range)

(Operating Conditions apply)[1)]

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Input low voltage (TTL, all except XTAL1) | $V_{IL}$ SR | -0.5 | 0.2 $V_{DD}$ - 0.1 | V | – |
| Input low voltage XTAL1 | $V_{IL2}$ SR | -0.5 | 0.3 $V_{DD}$ | V | – |
| Input high voltage (TTL, all except $\overline{\text{RSTIN}}$ and XTAL1) | $V_{IH}$ SR | 0.2 $V_{DD}$ + 0.9 | $V_{DD}$ + 0.5 | V | – |
| Input high voltage $\overline{\text{RSTIN}}$ (when operated as input) | $V_{IH1}$ SR | 0.6 $V_{DD}$ | $V_{DD}$ + 0.5 | V | – |
| Input high voltage XTAL1 | $V_{IH2}$ SR | 0.7 $V_{DD}$ | $V_{DD}$ + 0.5 | V | – |
| Output low voltage ($\overline{\text{PORT0}}$, $\overline{\text{PORT1}}$, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, $\overline{\text{RSTOUT}}$, $\overline{\text{RSTIN}}$[2)]) | $V_{OL}$ CC | – | 0.45 | V | $I_{OL}$ = 2.4 mA |
| Output low voltage (all other outputs) | $V_{OL1}$ CC | – | 0.45 | V | $I_{OL}$ = 1.6 mA |
| Output high voltage[3)] ($\overline{\text{PORT0}}$, $\overline{\text{PORT1}}$, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, $\overline{\text{RSTOUT}}$) | $V_{OH}$ CC | 2.4 | – | V | $I_{OH}$ = -2.4 mA |
| | | 0.9 $V_{DD}$ | – | V | $I_{OH}$ = -0.5 mA |
| Output high voltage[3)] (all other outputs) | $V_{OH1}$ CC | 2.4 | – | V | $I_{OH}$ = -1.6 mA |
| | | 0.9 $V_{DD}$ | – | V | $I_{OH}$ = -0.5 mA |
| Input leakage current (Port 5) | $I_{OZ1}$ CC | – | ±200 | nA | 0 V < $V_{IN}$ < $V_{DD}$ |
| Input leakage current (all other) | $I_{OZ2}$ CC | – | ±500 | nA | 0.45 V < $V_{IN}$ < $V_{DD}$ |
| $\overline{\text{RSTIN}}$ inactive current[4)] | $I_{RSTH}$[5)] | – | -10 | µA | $V_{IN}$ = $V_{IH1}$ |

**DC Characteristics (Standard Supply Voltage Range)** (cont'd)
(Operating Conditions apply)[1)]

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| $\overline{\text{RSTIN}}$ active current[4)] | $I_{RSTL}$[6)] | -100 | – | µA | $V_{IN} = V_{IL}$ |
| $\overline{\text{RD}}/\overline{\text{WR}}$ inact. current[7)] | $I_{RWH}$[5)] | – | -40 | µA | $V_{OUT}$ = 2.4 V |
| $\overline{\text{RD}}/\overline{\text{WR}}$ active current[7)] | $I_{RWL}$[6)] | -500 | – | µA | $V_{OUT} = V_{OLmax}$ |
| ALE inactive current[7)] | $I_{ALEL}$[5)] | – | 40 | µA | $V_{OUT} = V_{OLmax}$ |
| ALE active current[7)] | $I_{ALEH}$[6)] | 500 | – | µA | $V_{OUT}$ = 2.4 V |
| Port 6 inactive current[7)] | $I_{P6H}$[5)] | – | -40 | µA | $V_{OUT}$ = 2.4 V |
| Port 6 active current[7)] | $I_{P6L}$[6)] | -500 | – | µA | $V_{OUT} = V_{OL1max}$ |
| PORT0 configuration current[7)] | $I_{P0H}$[5)] | – | -10 | µA | $V_{IN} = V_{IHmin}$ |
| | $I_{P0L}$[6)] | -100 | – | µA | $V_{IN} = V_{ILmax}$ |
| XTAL1 input current | $I_{IL}$ CC | – | ±20 | µA | 0 V < $V_{IN}$ < $V_{DD}$ |
| Pin capacitance[8)] (digital inputs/outputs) | $C_{IO}$ CC | – | 10 | pF | $f$ = 1 MHz<br>$T_A$ = 25 °C |

1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current $I_{OV}$.

2) Valid in bidirectional reset mode only.

3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

4) These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 kΩ.

5) The maximum current may be drawn while the respective signal line remains inactive.

6) The minimum current must be drawn in order to drive the respective signal line active.

7) This specification is valid during Reset and during Adapt-mode.

8) Not 100% tested, guaranteed by design and characterization.

**DC Characteristics (Reduced Supply Voltage Range)** (cont'd)
(Operating Conditions apply)[1)]

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| PORT0 configuration current[7)] | $I_{P0H}$[5)] | – | -5 | µA | $V_{IN} = V_{IHmin}$ |
| | $I_{P0L}$[6)] | -100 | – | µA | $V_{IN} = V_{ILmax}$ |
| XTAL1 input current | $I_{IL}$ CC | – | ±20 | µA | 0 V < $V_{IN}$ < $V_{DD}$ |
| Pin capacitance[8)] (digital inputs/outputs) | $C_{IO}$ CC | – | 10 | pF | $f$ = 1 MHz<br>$T_A$ = 25 °C |

1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current $I_{OV}$.

2) Valid in bidirectional reset mode only.

3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

4) These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 kΩ.

5) The maximum current may be drawn while the respective signal line remains inactive.

6) The minimum current must be drawn in order to drive the respective signal line active.

7) This specification is valid during Reset and during Adapt-mode.

8) Not 100% tested, guaranteed by design and characterization.

**Multiplexed Bus (Reduced Supply Voltage Range)** (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A + t_C + t_F$ (150 ns at 20 MHz CPU clock without waitstates)

| Parameter | Symbol | | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1 / 2TCL = 1 to 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | |
| Data valid to $\overline{\text{WrCS}}$ | $t_{50}$ | CC | 28 + $t_C$ | – | 2TCL - 22 + $t_C$ | – | ns |
| Data hold after $\overline{\text{RdCS}}$ | $t_{51}$ | SR | 0 | – | 0 | – | ns |
| Data float after $\overline{\text{RdCS}}$ | $t_{52}$ | SR | – | 30 + $t_F$ | – | 2TCL - 20 + $t_F$ | ns |
| Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ | $t_{54}$ | CC | 30 + $t_F$ | – | 2TCL - 20 + $t_F$ | – | ns |
| Data hold after $\overline{\text{WrCS}}$ | $t_{56}$ | CC | 30 + $t_F$ | – | 2TCL - 20 + $t_F$ | – | ns |

1) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

**Demultiplexed Bus (Standard Supply Voltage Range)** (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2$t_A$ + $t_C$ + $t_F$ (80 ns at 25 MHz CPU clock without waitstates)

| Parameter | Symbol | | Max. CPU Clock = 25 MHz | | Variable CPU Clock 1 / 2TCL = 1 to 25 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | |
| Data float after $\overline{\text{RdCS}}$ (with RW-delay)[1] | $t_{53}$ | SR | – | 20 + $t_F$ | – | 2TCL - 20 + 2$t_A$ + $t_F$ [1] | ns |
| Data float after $\overline{\text{RdCS}}$ (no RW-delay)[1] | $t_{68}$ | SR | – | 0 + $t_F$ | – | TCL - 20 + 2$t_A$ + $t_F$ [1] | ns |
| Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ | $t_{55}$ | CC | -6 + $t_F$ | – | -6 + $t_F$ | – | ns |
| Data hold after $\overline{\text{WrCS}}$ | $t_{57}$ | CC | 6 + $t_F$ | – | TCL - 14 + $t_F$ | – | ns |

1) RW-delay and $t_A$ refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.

3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

## AC Characteristics

### Demultiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply)
ALE cycle time = 4 TCL + 2$t_A$ + $t_C$ + $t_F$ (100 ns at 20 MHz CPU clock without waitstates)

| Parameter | Symbol | | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1 / 2TCL = 1 to 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | |
| ALE high time | $t_5$ | CC | 11 + $t_A$ | – | TCL - 14 + $t_A$ | – | ns |
| Address setup to ALE | $t_6$ | CC | 5 + $t_A$ | – | TCL - 20 + $t_A$ | – | ns |
| ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay) | $t_8$ | CC | 15 + $t_A$ | – | TCL - 10 + $t_A$ | – | ns |
| ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay) | $t_9$ | CC | -10 + $t_A$ | – | -10 + $t_A$ | – | ns |
| $\overline{RD}$, $\overline{WR}$ low time (with RW-delay) | $t_{12}$ | CC | 34 + $t_C$ | – | 2TCL - 16 + $t_C$ | – | ns |
| $\overline{RD}$, $\overline{WR}$ low time (no RW-delay) | $t_{13}$ | CC | 59 + $t_C$ | – | 3TCL - 16 + $t_C$ | – | ns |
| $\overline{RD}$ to valid data in (with RW-delay) | $t_{14}$ | SR | – | 22 + $t_C$ | – | 2TCL - 28 + $t_C$ | ns |
| $\overline{RD}$ to valid data in (no RW-delay) | $t_{15}$ | SR | – | 47 + $t_C$ | – | 3TCL - 28 + $t_C$ | ns |
| ALE low to valid data in | $t_{16}$ | SR | – | 45 + $t_A$ + $t_C$ | – | 3TCL - 30 + $t_A$ + $t_C$ | ns |
| Address to valid data in | $t_{17}$ | SR | – | 57 + 2$t_A$ + $t_C$ | – | 4TCL - 43 + 2$t_A$ + $t_C$ | ns |
| Data hold after $\overline{RD}$ rising edge | $t_{18}$ | SR | 0 | – | 0 | – | ns |
| Data float after $\overline{RD}$ rising edge (with RW-delay[1)]) | $t_{20}$ | SR | – | 36 + 2$t_A$ + $t_F$[1)] | – | 2TCL - 14 + 22$t_A$ + $t_F$[1)] | ns |
| Data float after $\overline{RD}$ rising edge (no RW-delay[1)]) | $t_{21}$ | SR | – | 15 + 2$t_A$ + $t_F$[1)] | – | TCL - 10 + 22$t_A$ + $t_F$[1)] | ns |

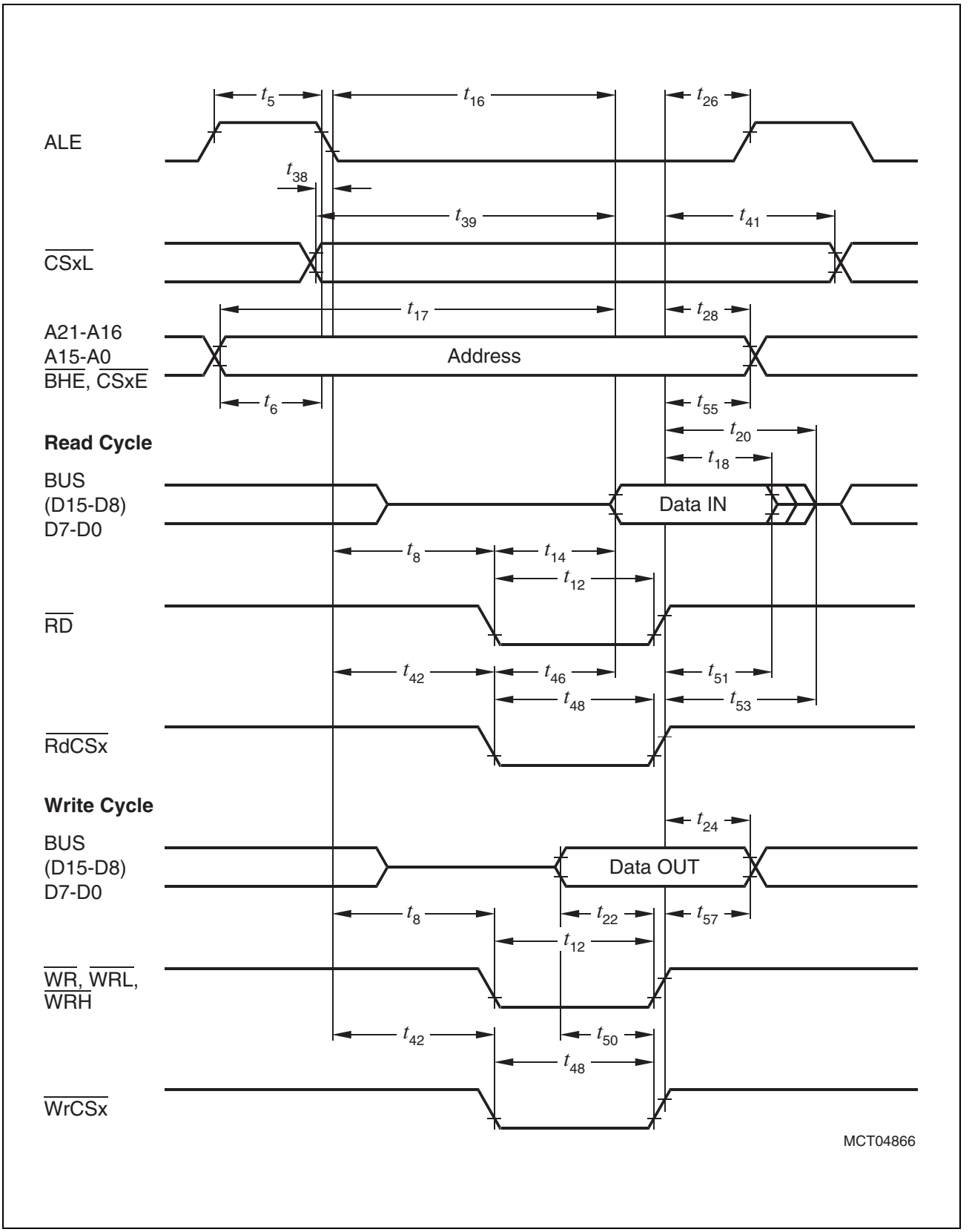



**Figure 17 External Memory Cycle:
Demultiplexed Bus, With Read/Write Delay, Extended ALE**

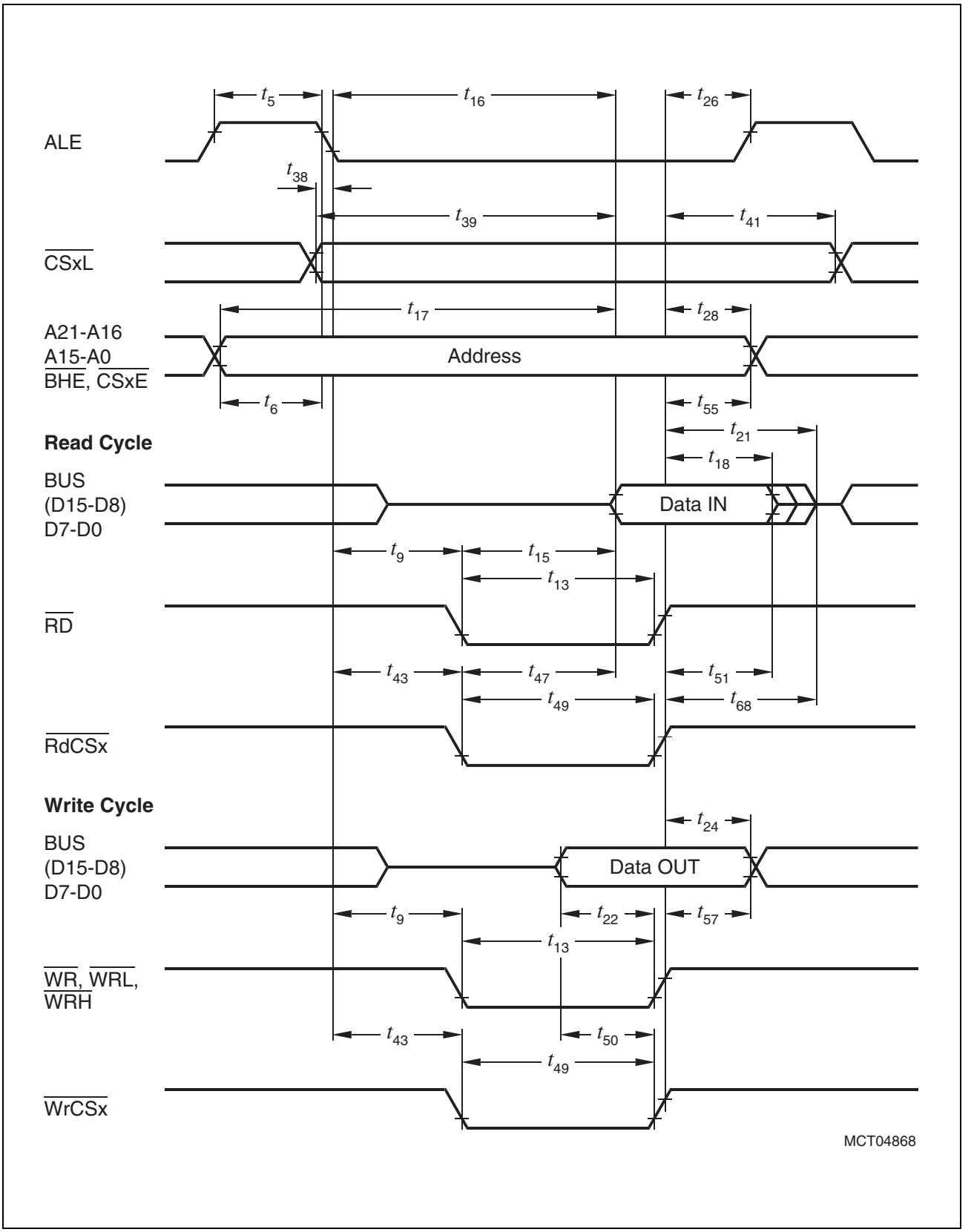



**Figure 19 External Memory Cycle:
Demultiplexed Bus, No Read/Write Delay, Extended ALE**