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Details

Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	63
Program Memory Size	•
Program Memory Type	ROMIess
EEPROM Size	•
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	•
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	P-MQFP-80-1
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c161olmhabxqma1

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C161K C161O

16-Bit Single-Chip Microcontroller

Microcontrollers



Never stop thinking.



Introduction

The C161K/O is a derivative of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. It combines high CPU performance (up to 12.5 million instructions per second) with peripheral functionality and enhanced IO-capabilities. The C161K/O is especially suited for cost sensitive applications.



Figure 1 Logic Symbol



Pin Configuration MQFP Package

(top view)



Figure 2

Note: The **marked** signals are **only available in the C1610**. Please also refer to the detailed description below (shaded lines).



Functional Description

The architecture of the C161K/O combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C161K/O.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).



Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resources, the X-Peripherals (see Figure 3).



Memory Organization

The memory space of the C161K/O is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C161K/O is prepared to incorporate on-chip program memory (not in the ROM-less derivatives, of course) for code or constant data. The internal ROM area can be mapped either to segment 0 or segment 1.

On-chip Internal RAM (IRAM) is provided (1 KByte in the C161K, 2 KBytes in the C161O) as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 4 MBytes of external RAM and/or ROM can be connected to the microcontroller.



Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C161K/O is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C161K/O supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C161K/O has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C161K/O interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).



The C161K/O also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during runtime:

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: – Hardware Reset – Software Reset – W-dog Timer Overflow	-	RESET RESET RESET	00'0000 _H 00'0000 _H 00'0000 _H	00 _H 00 _H 00 _H	
Class A Hardware Traps: – Non-Maskable Interrupt – Stack Overflow – Stack Underflow	NMI STKOF STKUF	NMITRAP STOTRAP STUTRAP	00'0008 _H 00'0010 _H 00'0018 _H	02 _H 04 _H 06 _H	
 Class B Hardware Traps: Undefined Opcode Protected Instruction Fault Illegal Word Operand Access 	UNDOPC PRTFLT ILLOPA	BTRAP BTRAP BTRAP	00'0028 _H 00'0028 _H 00'0028 _H	0A _H 0A _H 0A _H	1
 Illegal Instruction Access Illegal External Bus Access 	ILLINA ILLBUS	BTRAP BTRAP	00'0028 _H 00'0028 _H	0A _H 0A _H	1
Reserved	_	_	[2C _H – 3C _H]	[0B _H – 0F _H]	-
Software Traps – TRAP Instruction	-	-	Any [00'0000 _H 00'01FC _H] in steps of 4 _H	Any [00 _H – 7F _H]	Current CPU Priority

Table 4Hardware Trap Summary



General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.



Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the RSTOUT pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 20 μ s and 336 ms can be monitored (@ 25 MHz).

The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

Parallel Ports

The C161K/O provides up to 63 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A21/19/17 ... A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 6 provides optional chip select signals.

Port 3 includes alternate functions of timers, serial interfaces, and the optional bus control signal BHE/WRH.

Port 5 is used for timer control signals.



Table 6	C161K/O Registers, Ordered by Name (cont'd)
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Name		Physica Address	Physical 8-B Address Add		Description	Reset Value
DP0H	b	F102 _H	Ε	81 _H	P0H Direction Control Register	00 _H
DP0L	b	F100 _H	Ε	80 _H	P0L Direction Control Register	00 _H
DP1H	b	F106 _H	Ε	83 _H	P1H Direction Control Register	00 _H
DP1L	b	F104 _H	Ε	82 _H	P1L Direction Control Register	00 _H
DP2	b	FFC2 _H		E1 _H	Port 2 Direction Control Register	0000 _H
DP3	b	FFC6 _H		E3 _H	Port 3 Direction Control Register	0000 _H
DP4	b	FFCA _H		E5 _H	Port 4 Direction Control Register	00 _H
DP6	b	FFCE _H		E7 _H	Port 6 Direction Control Register	00 _H
DPP0		FE00 _H		00 _H	CPU Data Page Pointer 0 Reg. (10 bits)	0000 _H
DPP1		FE02 _H		01 _H	CPU Data Page Pointer 1 Reg. (10 bits)	0001 _H
DPP2		FE04 _H		02 _H	CPU Data Page Pointer 2 Reg. (10 bits)	0002 _H
DPP3		FE06 _H		03 _H	CPU Data Page Pointer 3 Reg. (10 bits)	0003 _H
EXICON	b	F1C0 _H	Ε	E0 _H	External Interrupt Control Register	0000 _H
IDCHIP		F07C _H	Ε	3E _H	Identifier	05XX _H
IDMANUF		F07E _H	Ε	3F _H	Identifier	1820 _H
IDMEM		F07A _H	Ε	3D _H	Identifier	0000 _H
IDMEM2		F076 _H	Ε	3B _H	Identifier	0000 _H
IDPROG		F078 _H	Ε	3C _H	Identifier	0000 _H
MDC	b	FF0E _H		87 _H	CPU Multiply Divide Control Register	0000 _H
MDH		FE0C _H		06 _H	CPU Multiply Divide Reg. – High Word	0000 _H
MDL		FE0E _H		07 _H	CPU Multiply Divide Reg. – Low Word	0000 _H
ODP2	b	F1C2 _H	Ε	E1 _H	Port 2 Open Drain Control Register	0000 _H
ODP3	b	F1C6 _H	Ε	E3 _H	Port 3 Open Drain Control Register	0000 _H
ODP6	b	F1CE _H	Ε	E7 _H	Port 6 Open Drain Control Register	00 _H
ONES	b	FF1E _H		8F _H	Constant Value 1's Register (read only)	FFFF _H
P0H	b	FF02 _H		81 _H	Port 0 High Reg. (Upper half of PORT0)	00 _H
POL	b	FF00 _H		80 _H	Port 0 Low Reg. (Lower half of PORT0)	00 _H
P1H	b	FF06 _H		83 _H	Port 1 High Reg. (Upper half of PORT1)	00 _H
P1L	b	FF04 _H		82 _H	Port 1 Low Reg.(Lower half of PORT1)	00 _H
P2	b	FFC0 _H		E0 _H	Port 2 Register	0000 _H



DC Characteristics (Reduced Supply Voltage Range) (cont'd)

(Operating Conditions apply)¹⁾

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
PORT0 configuration current ⁷⁾	I _{P0H} ⁵	5)	_	-5	μA	$V_{\rm IN} = V_{\rm IHmin}$
	I _{P0L} ⁶	5)	-100	-	μA	$V_{\rm IN} = V_{\rm ILmax}$
XTAL1 input current	I_{IL}	CC	-	±20	μA	$0 V < V_{IN} < V_{DD}$
Pin capacitance ⁸⁾ (digital inputs/outputs)	C _{IO}	CC	_	10	pF	f = 1 MHz T _A = 25 °C

¹⁾ Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV} .

²⁾ Valid in bidirectional reset mode only.

³⁾ This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

⁴⁾ These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 k Ω .

⁵⁾ The maximum current may be drawn while the respective signal line remains inactive.

⁶⁾ The minimum current must be drawn in order to drive the respective signal line active.

⁷⁾ This specification is valid during Reset and during Adapt-mode.

⁸⁾ Not 100% tested, guaranteed by design and characterization.



AC Characteristics

Table 10External Clock Drive XTAL1 (Standard Supply Voltage Range)
(Operating Conditions apply)

Parameter Sy		bol	Diı	rect Drive 1:1	P	Prescaler 2:1		
			min.	max.	min.	max.		
Oscillator period	t _{OSC}	SR	40	_	20	_	ns	
High time ¹⁾	<i>t</i> ₁	SR	20 ²⁾	_	6	_	ns	
Low time ¹⁾	<i>t</i> ₂	SR	20 ²⁾	_	6	_	ns	
Rise time ¹⁾	t ₃	SR	_	10	-	6	ns	
Fall time ¹⁾	<i>t</i> ₄	SR	_	10	-	6	ns	

¹⁾ The clock input signal must reach the defined levels V_{IL2} and V_{IH2} .

²⁾ The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

Table 11External Clock Drive XTAL1 (Reduced Supply Voltage Range)
(Operating Conditions apply)

Parameter	Symbol		Direc 1	t Drive 1:1	Pres 2	caler :1	Unit
			min.	max.	min.	max.	
Oscillator period	t _{OSC}	SR	50	-	25	-	ns
High time ¹⁾	t ₁	SR	25 ²⁾	-	8	-	ns
Low time ¹⁾	<i>t</i> ₂	SR	25 ²⁾	-	8	-	ns
Rise time ¹⁾	t ₃	SR	-	10	-	6	ns
Fall time ¹⁾	<i>t</i> ₄	SR	-	10	-	6	ns

¹⁾ The clock input signal must reach the defined levels V_{IL2} and V_{IH2} .

²⁾ The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.



Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 12 Memory Cycle Variables

Description	Symbol	Values
ALE Extension	t _A	TCL × <alectl></alectl>
Memory Cycle Time Waitstates	t _C	2TCL × (15 - <mctc>)</mctc>
Memory Tristate Time	t _F	2TCL × (1 - <mttc>)</mttc>

Note: Please respect the maximum operating frequency of the respective derivative.

AC Characteristics

Multiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter		nbol	Max. CF = 25	PU Clock MHz	Variable (1 / 2TCL =	Unit	
			min.	max.	min.	max.	
ALE high time	<i>t</i> ₅	CC	$10 + t_{A}$	_	TCL - 10 + <i>t</i> _A	-	ns
Address setup to ALE	<i>t</i> ₆	CC	$4 + t_A$	-	TCL - 16 + <i>t</i> _A	-	ns
Address hold after ALE	<i>t</i> ₇	CC	$10 + t_{A}$	_	TCL - 10 + <i>t</i> _A	_	ns
ALE falling edge to \overline{RD} , WR (with RW-delay)	<i>t</i> 8	CC	$10 + t_{A}$	_	TCL - 10 + <i>t</i> _A	-	ns
ALE falling edge to RD, WR (no RW-delay)	t ₉	CC	$-10 + t_{A}$	_	$-10 + t_{A}$	-	ns
Address float after RD, WR (with RW-delay)	<i>t</i> ₁₀	CC	_	6	-	6	ns
Address float after RD, WR (no RW-delay)	<i>t</i> ₁₁	CC	-	26	-	TCL + 6	ns
RD, WR low time (with RW-delay)	t ₁₂	CC	$30 + t_{\rm C}$	_	2TCL - 10 + <i>t</i> _C	-	ns



AC Characteristics

Demultiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. C = 25	PU Clock 5 MHz	Variable (1 / 2TCL = 1	Unit	
			min.	max.	min.	max.	
ALE high time	<i>t</i> ₅	CC	$10 + t_{A}$	-	TCL - 10 + <i>t</i> _A	_	ns
Address setup to ALE	<i>t</i> ₆	CC	$4 + t_A$	-	TCL - 16 + <i>t</i> _A	_	ns
ALE falling edge to \overline{RD} , WR (with RW-delay)	t ₈	CC	$10 + t_{A}$	_	TCL - 10 + <i>t</i> _A	_	ns
ALE falling edge to \overline{RD} , WR (no RW-delay)	t ₉	CC	$-10 + t_{A}$	-	-10 + <i>t</i> _A	_	ns
RD, WR low time (with RW-delay)	t ₁₂	CC	$30 + t_{\rm C}$	-	2TCL - 10 + <i>t</i> _C	_	ns
RD, WR low time (no RW-delay)	t ₁₃	CC	$50 + t_{\rm C}$	-	3TCL - 10 + <i>t</i> _C	-	ns
RD to valid data in (with RW-delay)	t ₁₄	SR	_	$20 + t_{\rm C}$	-	2TCL - 20 + <i>t</i> _C	ns
RD to valid data in (no RW-delay)	t ₁₅	SR	_	$40 + t_{\rm C}$	-	3TCL - 20 + <i>t</i> _C	ns
ALE low to valid data in	t ₁₆	SR	_	$40 + t_{A} + t_{C}$	_	3TCL - 20 + <i>t</i> _A + <i>t</i> _C	ns
Address to valid data in	t ₁₇	SR	_	$50 + 2t_A + t_C$	_	$4TCL - 30 + 2t_A + t_C$	ns
Data hold after RD rising edge	t ₁₈	SR	0	-	0	-	ns
Data float after RD rising edge (with RW-delay ¹⁾)	t ₂₀	SR	_	$26 + 2t_{A} + t_{F}^{1)}$	-	$2\text{TCL} - 14 + 22t_{\text{A}} + t_{\text{F}}^{1)}$	ns
Data float after RD rising edge (no RW-delay ¹⁾)	t ₂₁	SR	_	$10 + 2t_A + t_F^{(1)}$	-	TCL - 10 + $22t_A$ + $t_F^{(1)}$	ns



Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. C = 20	PU Clock) MHz	Variable (1 / 2TCL =	Unit	
			min.	max.	min.	max.	
Data valid to WR	t ₂₂	CC	$24 + t_{C}$	_	2TCL - 26	_	ns
					$+ t_{\rm C}$		
Data hold after \overline{WR}	t ₂₄	CC	15 + <i>t</i> _F	_	TCL - 10 + <i>t</i> _F	_	ns
ALE rising edge after RD, WR	t ₂₆	CC	-12 + <i>t</i> _F	-	-12 + <i>t</i> _F	_	ns
Address hold after WR ²⁾	t ₂₈	CC	$0 + t_{F}$	-	$0 + t_{F}$	-	ns
ALE falling edge to $\overline{CS}^{3)}$	t ₃₈	CC	-8 - t _A	10 - <i>t</i> _A	-8 - t _A	10 - <i>t</i> _A	ns
CS low to Valid Data In ³⁾	t ₃₉	SR	_	$47 + t_{C} + 2t_{A}$	_	3TCL - 28 + <i>t</i> _C + 2 <i>t</i> _A	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}^{3)}$	t ₄₁	CC	9 + <i>t</i> _F	-	TCL - 16 + <i>t</i> _F	_	ns
ALE falling edge to RdCS, WrCS (with RW- delay)	t ₄₂	CC	19 + <i>t</i> _A	-	TCL - 6 + <i>t</i> _A	-	ns
ALE falling edge to RdCS, WrCS (no RW- delay)	t ₄₃	CC	$-6 + t_{A}$	-	-6 + <i>t</i> _A	-	ns
RdCS to Valid Data In (with RW-delay)	t ₄₆	SR	_	$20 + t_{\rm C}$	-	2TCL - 30 + <i>t</i> _C	ns
RdCS to Valid Data In (no RW-delay)	t ₄₇	SR	_	$45 + t_{\rm C}$	_	3TCL - 30 + <i>t</i> _C	ns
RdCS, WrCS Low Time (with RW-delay)	t ₄₈	CC	$38 + t_{\rm C}$	-	2TCL - 12 + <i>t</i> _C	-	ns
RdCS, WrCS Low Time (no RW-delay)	t ₄₉	CC	$63 + t_{\rm C}$	-	3TCL - 12 + <i>t</i> _C	_	ns
Data valid to WrCS	<i>t</i> ₅₀	CC	$28 + t_{\rm C}$	-	2TCL - 22 + <i>t</i> _C	_	ns
Data hold after RdCS	<i>t</i> ₅₁	SR	0	-	0	-	ns



Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A + t_C + t_F$ (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CI = 20	PU Clock) MHz	Variable (1 / 2TCL = ⁻	Unit	
			min.	max.	min.	max.	
Data float after RdCS (with RW-delay) ¹⁾	t ₅₃	SR	_	30 + <i>t</i> _F	_	2TCL - 20 + 2 <i>t</i> _A + <i>t</i> _F 1)	ns
Data float after RdCS (no RW-delay) ¹⁾	t ₆₈	SR	_	5 + <i>t</i> _F	_	TCL - 20 + $2t_A + t_F$ 1)	ns
Address hold after RdCS, WrCS	t ₅₅	CC	-16 + <i>t</i> _F	-	-16 + <i>t</i> _F	-	ns
Data hold after WrCS	t ₅₇	CC	9 + $t_{\sf F}$	-	TCL - 16 + <i>t</i> _F	-	ns

¹⁾ RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

²⁾ Read data are latched with the same clock edge that triggers the address change and the rising RD edge. Therefore address changes before the end of RD have no impact on read cycles.

³⁾ These parameters refer to the latched chip select signals (CSxL). The early chip select signals (CSxE) are specified together with the address and signal BHE (see figures below).





Figure 18 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE





Figure 19 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

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"Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.

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Dr. Ulrich Schumacher

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