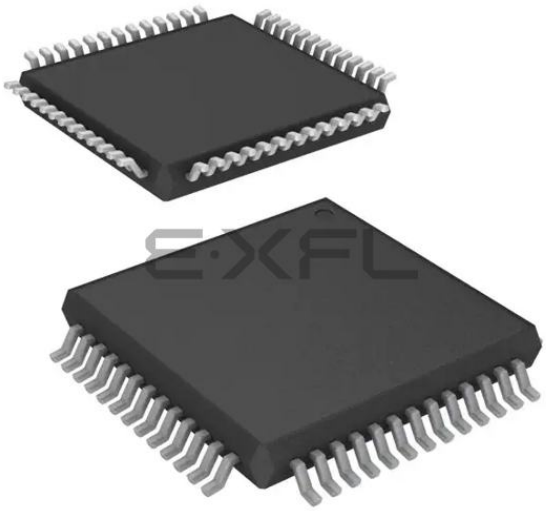


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21244snfp-x6

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and are packaged in a 52-pin molded-plastic LQFP or a 64-pin molded-plastic FLGA. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.
Furthermore, the R8C/25 Group has on-chip data flash (1 KB x 2 blocks).
The difference between the R8C/24 Group and R8C/25 Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, etc.

Table 1.2 Functions and Specifications for R8C/25 Group

Item			Specification
CPU	Number of fundamental instructions		89 instructions
	Minimum instruction execution time		50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)
	Operating mode		Single-chip
	Address space		1 Mbyte
	Memory capacity		Refer to **Table 1.4 Product Information for R8C/25 Group**
Peripheral Functions	Ports		I/O ports: 41 pins, Input port: 3 pins
	LED drive ports		I/O ports: 8 pins
	Timers		Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits × 2 channels (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function
	Serial interface		2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface		1 channel I2C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module		Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter		10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer		15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupts		Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels
	Clock	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz)
			Real-time clock (timer RE)
	Oscillation stop detection function		XIN clock oscillation stop detection function
	Voltage detection circuit		On-chip
	Power-on reset circuit		On-chip
Electrical Characteristics	Supply voltage		VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz)
	Current consumption		Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash memory	Programming and erasure voltage		VCC = 2.7 to 5.5 V
	Programming and erasure endurance		1,0000 times (data flash)
			1,000 times (program ROM)
Operating Ambient Temperature			-20 to 85°C (N version)
			-40 to 85°C (D version)(2)
			-20 to 105°C (Y version)(3)
Package			52-pin molded-plastic LQFP
			64-pin molded-plastic FLGA

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

Table 1.4 Product Information for R8C/25 Group Current of Feb. 2008

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21254SNFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21255SNFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Blank product
R5F21255SDFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Factory programming product(1)
R5F21255SNXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNXXXLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Factory programming product(1)
R5F21255SDXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	

NOTE:
1. The user ROM is programmed before shipment.

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C bus Interface	A/D Converter
2		P3_5				SSCK	SCL	
3		P3_3				SSI		
4		P3_4				$\overline{SCS}$	$\overline{SDA}$	
5	MODE							
6	XCIN	P4_3						
7	XCOUT	P4_4						
8	$\overline{RESET}$							
9	XOUT	P4_7						
10	VSS/AVSS							
11	XIN	P4_6						
12	VCC/AVCC							
13		P2_7		TRDIOD1				
14		P2_6		TRDIOC1				
15		P2_5		TRDIOB1				
16		P2_4		TRDIOA1				
17		P2_3		TRDIOD0				
18		P2_2		TRDIOC0				
19		P2_1		TRDIOB0				
20		P2_0		TRDIOA0/TRDCLK				
21		P1_7	$\overline{INT1}$	TRAIO				
22		P1_6			CLK0			
23		P1_5	$\overline{(INT1)}$(1)	(TRAIO)(1)	RXD0			
24		P1_4			TXD0			
25		P1_3	$\overline{KI3}$					AN11
27		P4_5	$\overline{INT0}$	$\overline{INT0}$				
28		P6_6	$\overline{INT2}$		TXD1			
29		P6_7	$\overline{INT3}$		RXD1			
30		P1_2	$\overline{KI2}$					AN10
31		P1_1	$\overline{KI1}$					AN9
32		P1_0	$\overline{KI0}$					AN8
33		P3_1		TRBO				
34		P3_0		TRAO				
35		P6_5			CLK1			
36		P6_4						
37		P6_3						
38		P0_7						AN0
41		P0_6						AN1
42		P0_5						AN2
43		P0_4						AN3
44	VREF	P4_2						
45		P6_0		TREO				
46		P6_2						
47		P6_1						
48		P0_3						AN4
49		P0_2						AN5
50		P0_1						AN6
51		P0_0						AN7
52		P3_7				SSO		

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

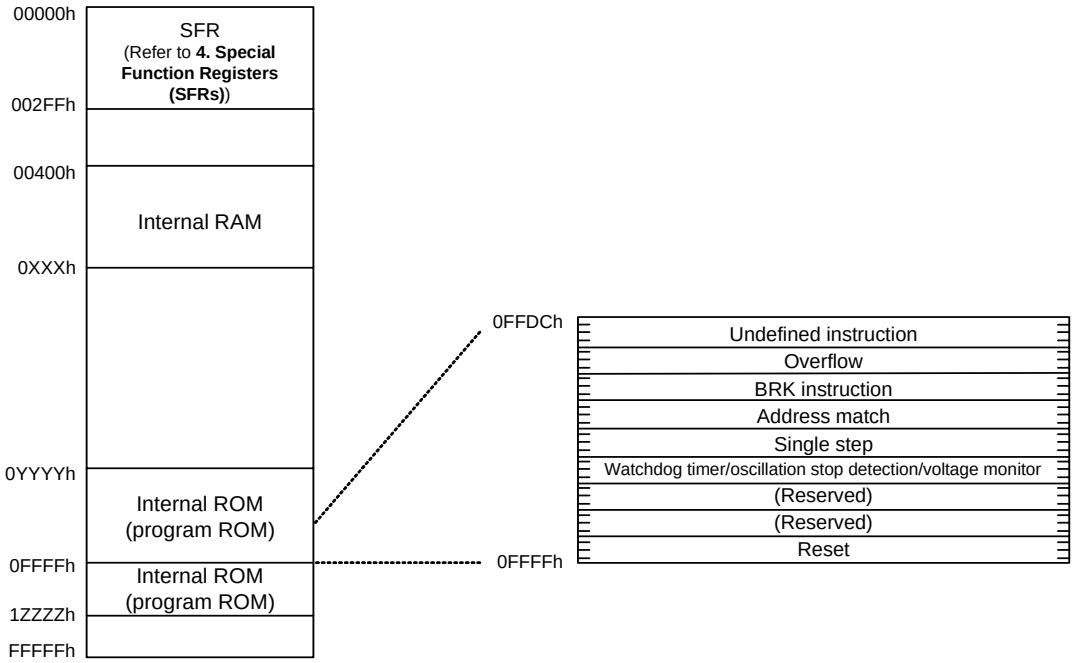
2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

3. Memory

3.1 R8C/24 Group

Figure 3.1 is a Memory Map of R8C/24 Group. The R8C/24 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM area is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address 1ZZZZh	Size	Address 0XXXXh
R5F21244SNFP, R5F21244SNXXXFP, R5F21244SDFP, R5F21244SDXXXFP, R5F21244SNLG, R5F21244SNXXXLG	16 Kbytes	0C000h	–	1 Kbyte	007FFh
R5F21245SNFP, R5F21245SNXXXFP, R5F21245SDFP, R5F21245SDXXXFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21246SNFP, R5F21246SNXXXFP, R5F21246SDFP, R5F21246SDXXXFP, R5F21246SNLG, R5F21246SNXXXLG	32 Kbytes	08000h	–	2 Kbytes	00BFFh
R5F21247SNFP, R5F21247SNXXXFP, R5F21247SDFP, R5F21247SDXXXFP	48 Kbytes	04000h	–	2.5 Kbytes	00DFFh
R5F21248SNFP, R5F21248SNXXXFP, R5F21248SDFP, R5F21248SDXXXFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh

Figure 3.1 Memory Map of R8C/24 Group

Table 4.2 SFR Information (2)[1]

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC Interrupt Control Register[2]	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P2 Drive Capacity Control Register	P2DRR	00h
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

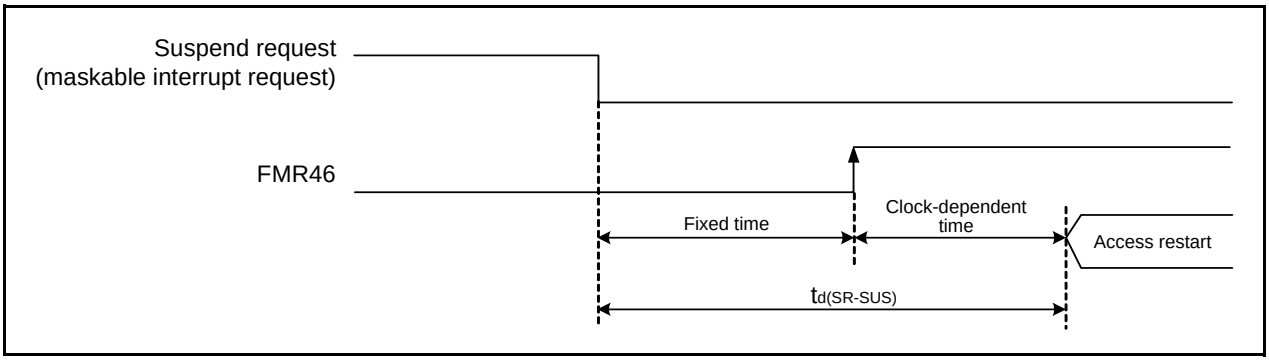


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level		2.2	2.3	2.4	V
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	0.9	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	300	µs
Vccmin	MCU operating voltage minimum value		2.2	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level		2.70	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 to 5.25 V 0°C ≤ T_{opr} ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	38.8	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C	38.4	40	40.8	MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 2.7 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38	40	42	MHz
		V_{CC} = 2.7 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	37.6	40	42.4	MHz
		V_{CC} = 2.2 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(3)	35.2	40	44.8	MHz
		V_{CC} = 2.2 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(3)	34	40	46	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4)	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864		MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	-3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

NOTES:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Standard values when the FRA1 register value after reset is assumed.
3. Standard values when the corrected value of the FRA6 register has been written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

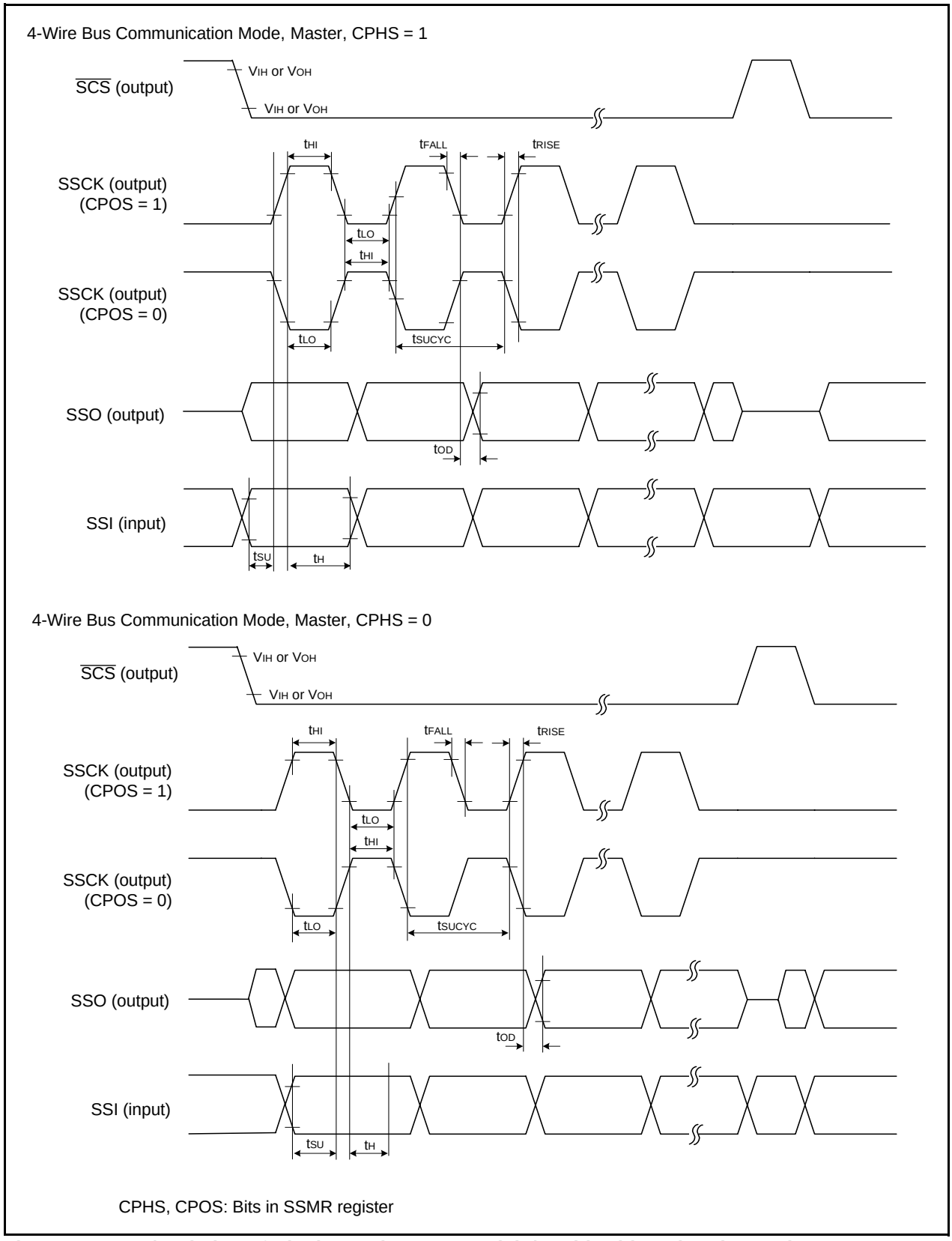


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

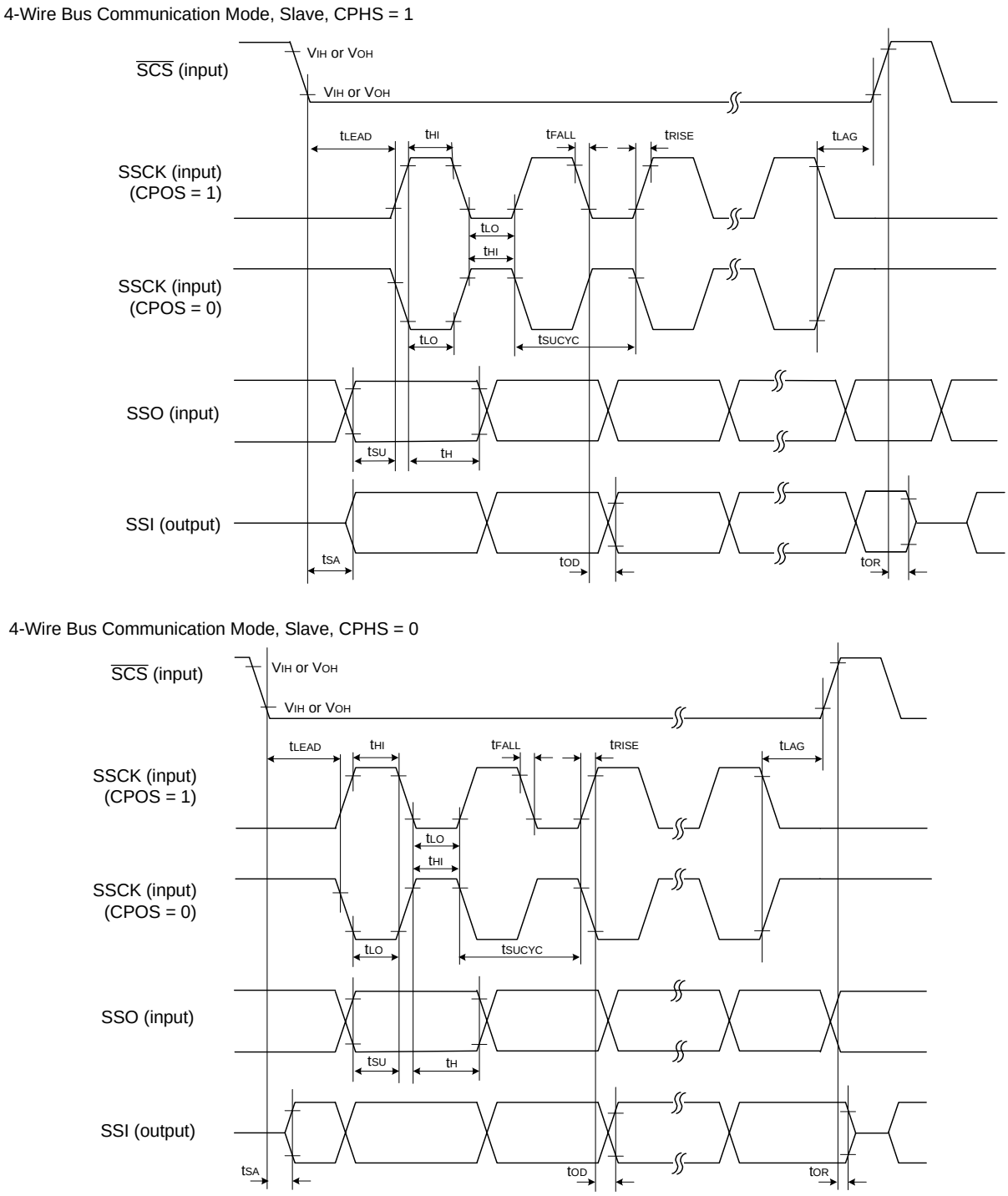


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.15 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200 µA		V_{CC} – 0.5	–	V_{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 µA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 µA		–	–	0.45	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 µA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, KI1, KI2, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, Vcc = 5V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 5V		–	–	-5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, Vcc = 5V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

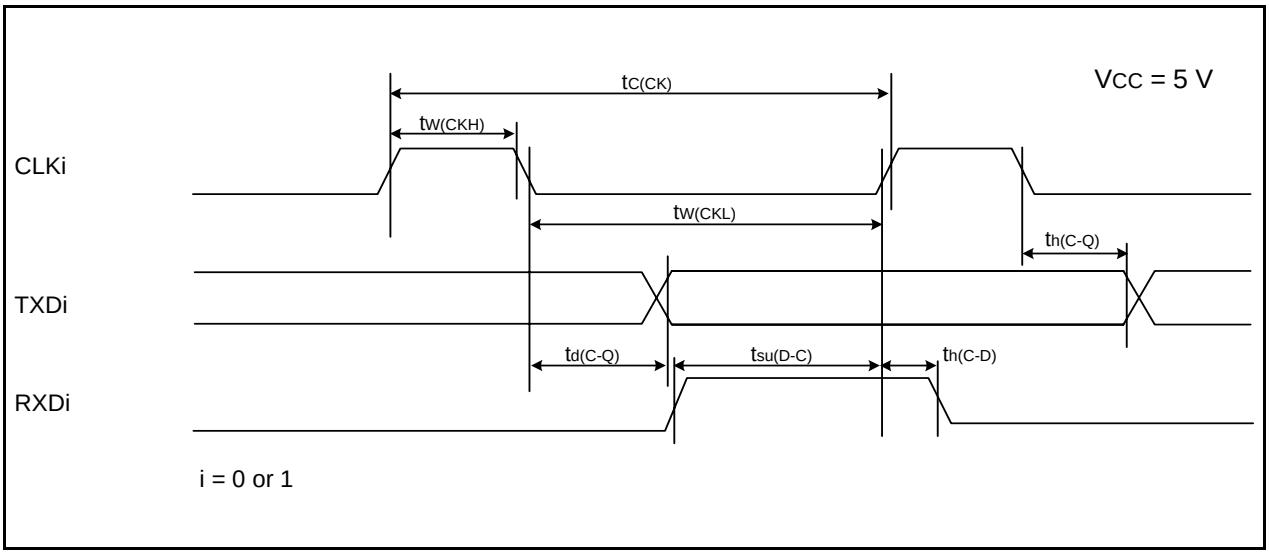


Figure 5.10 Serial Interface Timing Diagram when VCC = 5 V

Table 5.21 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

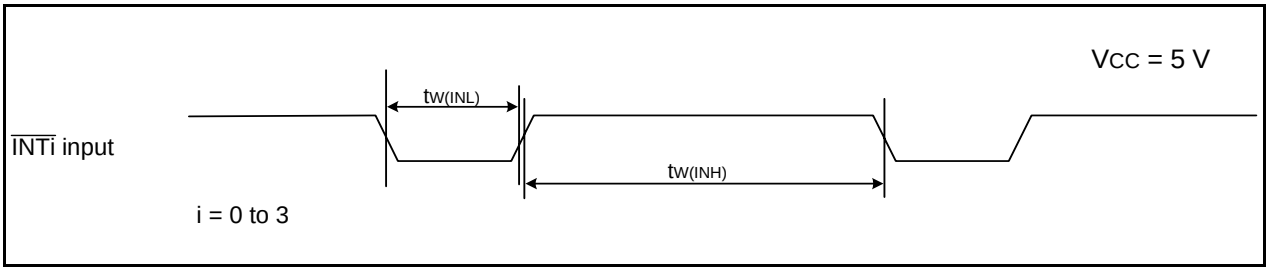


Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V

Table 5.22 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -1 mA		Vcc - 0.5	–	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -5 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -1 mA	Vcc - 0.5	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -50 µA	Vcc - 0.5	–	Vcc	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 5 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, Vcc = 3V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 3V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, Vcc = 3V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc =2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.28 Electrical Characteristics (5) [Vcc = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -1 mA		Vcc - 0.5	–	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -2 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -1 mA	Vcc - 0.5	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -50 µA	Vcc - 0.5	–	Vcc	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 2 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.05	0.3	–	V
		$\overline{RESET}$			0.05	0.15	–	V
I_{IH}	Input “H” current		VI = 2.2 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V		100	200	600	kΩ
R_{fXIN}	Feedback resistance	XIN			–	5	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	35	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	100	230	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	25	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.0	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	1.8	–	µA
		Increase during A/D converter operation	Without sample & hold	–	0.4	–	mA
			With sample & hold	–	0.3	–	mA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Feb 24, 2005	1 to 3 5, 6	Pin type changed: 48-pin(under consideration) → 52-pin.
		5 to 7	Package type revised: 48-pin LQFP(under consideration) → PLQP0052JA-A
		8	Table 1.5 TCLK added, VREF revised.
		9	Table 1.6 revised.
		13, 14	Figures 3.1 and 3.2 part number revised.
		15	Tabel 4.1 revised: - 000Fh: 000XXXXXb → 00011111b - 0023h: FR0 → FRA0 - 0024h: FR1 → FRA1 - 0025h: FR2 → FRA2 - 0031h: Voltage Detection A Register 1, VC1 → Voltage Detection Register 1, VCA1 - 0032h: Voltage Detection A Register 2, VC2 → Voltage Detection Register 2, VCA2
		17	Tabel 4.3 Register name and the value after reset at 00B8h to 00BFh revised; NOTE2 added.
		19	Tabel 4.5 revised: - 0107h: LINSR → LINST - 0137h to 013Fh: Register symbol revised
		20	Tabel 4.6 revised: - 0140h to 015Fh: Register symbol revised - 0158h, 0159h: Timer RD General Register → Timer RD General Register A1
0.20	Mar 8, 2005	2, 3 8	Tables 1.1, 1.2 and 1.5 revised: “main clock” → “XIN clock”; “sub clock” → “XCIN clock”
		15	- 0023h to 0025h: 40MHz On-Chip Oscillator Control Register → High-Speed On-Chip Oscillator Control Register
0.30	Sep 01, 2005	2, 3	Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance • Serial Interface revised: - Serial Interface: 2 channels Clock synchronous serial I/O, UART - Clock Synchronous Serial Interface: 1 channel I^2C bus Interface(1), Clock synchronous serial I/O with chip select
		4	Figure 1.1 Block Diagram • UART or Clock Synchronous Serial Interface: “(8 bits × 1 channel)” → “(8 bits × 2 channels)” revised • UART (8 bits × 1 channel) deleted
		5, 6	Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group “Flash Memory Version” → “N Version” revised

Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	19	Tabel 4.5 SFR Information(5) revised: • 0118h : Timer RE Second Data Register/Counter Register → Timer RE Second Data Register/Counter Data Register
		20	Tabel 4.6 SFR Information(6) revised: • 0145h POCR0 → TRDPOCR0 • 0146h, 0147h TRDCNT0 → TRD0 • 0148h, 0149h GRA0 → TRDGRA0 • 014Ah, 014Bh GRB0 → TRDGRB0 • 014Ch, 014Dh GRC0 → TRDGRC0 • 014Eh, 014Fh GRD0 → TRDGRD0 • 0155h POCR1 → TRDPOCR1 • 0156h, 0157h TRDCNT1 → TRD1 • 0158h, 0159h GRA1 → TRDGRA1 • 015Ah, 015Bh GRB1 → TRDGRB1 • 015Ch, 015Dh GRC1 → TRDGRC1 • 015Eh, 015Fh GRD1 → TRDGRD1
		21	Tabel 4.7 SFR Information(7) revised: • 01B5h: 01000101b → 1000000Xb • 01B7h: XX000001b → 00000001b • FFFFh: (Note 2) added
		22 to 44	5. Electrical Characteristics added
0.40	Jan 24, 2006	all pages	• “Preliminary” deleted • Symbol name “TRDMDR” → “TRDMR”, “SSUAIC” → “SSUIC”, and “IIC2AIC” → “IICIC” revised • Pin name “TCLK” → “TRDCLK” revised
		2	Table 1.1 Functions and Specifications for R8C/24 Group revised
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; “Peripheral Functions” added, “System Clock Generation” → “System Clock Generator” revised
		5	Table 1.3 Product Information for R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group revised
		7	Figure 1.4 Pin Assignments (Top View) “TCLK” → “TRDCLK” revised
		8	Table 1.5 Pin Functions “TCLK” → “TRDCLK” revised
		9	Table 1.6 Pin Name Information by Pin Number; “TCLK” → “TRDCLK” revised
		10	Figure 2.1 CPU Registers; “Reserved Area” → “Reserved Bit” revised
		12	2.8.10 Reserved Area; “Reserved Area” → “Reserved bit” revised
		13	Figure 3.1 Memory Map of R8C/24 Group; “Program area” → “program ROM” revised
		14	3.2 R8C/25 Group, Figure 3.2 Memory Map of R8C/25 Group; “Data area” → “data flash”, “Program area” → “program ROM” revised