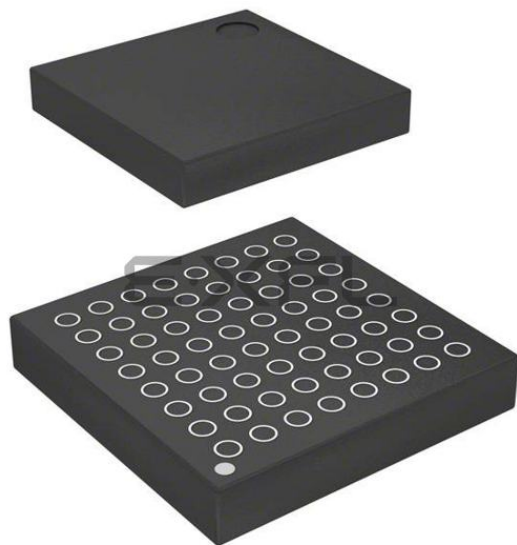




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFLGA
Supplier Device Package	64-TFLGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21244snlg-u0

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and are packaged in a 52-pin molded-plastic LQFP or a 64-pin molded-plastic FLGA. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/25 Group has on-chip data flash (1 KB x 2 blocks).

The difference between the R8C/24 Group and R8C/25 Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, etc.

Table 1.2 Functions and Specifications for R8C/25 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 2.2$ to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.4 Product Information for R8C/25 Group
Peripheral Functions	Ports	I/O ports: 41 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins
	Timers	Timer RA: 8 bits $\times$ 1 channel Timer RB: 8 bits $\times$ 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits $\times$ 2 channels (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function
	Serial interface	2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface	1 channel I ² C bus Interface ⁽¹⁾ Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits $\times$ 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels
	Clock	Clock generation circuits
		3 circuits - XIN clock generation circuit (with on-chip feedback resistor) - On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function - XCIN clock generation circuit (32 kHz)
		Real-time clock (timer RE)
	Oscillation stop detection function	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	$VCC = 3.0$ to 5.5 V ($f(XIN) = 20$ MHz) $VCC = 2.7$ to 5.5 V ($f(XIN) = 10$ MHz) $VCC = 2.2$ to 5.5 V ($f(XIN) = 5$ MHz)
	Current consumption	Typ. 10 mA ($VCC = 5.0$ V, $f(XIN) = 20$ MHz) Typ. 6 mA ($VCC = 3.0$ V, $f(XIN) = 10$ MHz) Typ. 2.0 μ A ($VCC = 3.0$ V, wait mode ($f(XCIN) = 32$ kHz)) Typ. 0.7 μ A ($VCC = 3.0$ V, stop mode)
Flash memory	Programming and erasure voltage	$VCC = 2.7$ to 5.5 V
	Programming and erasure endurance	1,000 times (data flash) 1,000 times (program ROM)
Operating Ambient Temperature		-20 to 85°C (N version)
		-40 to 85°C (D version) ⁽²⁾
		-20 to 105°C (Y version) ⁽³⁾
Package		52-pin molded-plastic LQFP
		64-pin molded-plastic FLGA

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

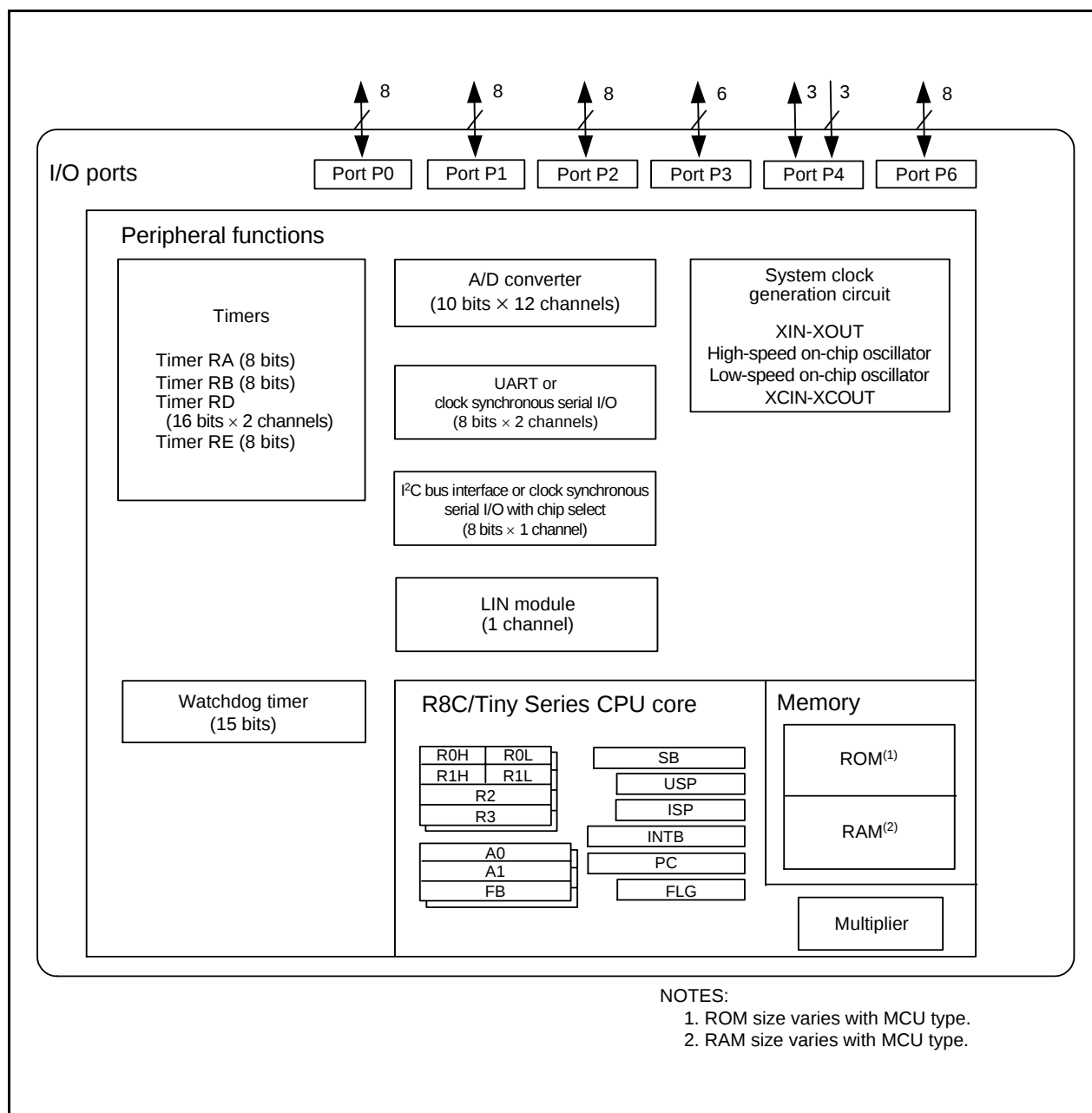


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information for R8C/24 Group and Table 1.4 lists the Product Information for R8C/25 Group.

Table 1.3 Product Information for R8C/24 Group

Current of Feb. 2008

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21244SNFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21245SNFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	D version Blank product
R5F21244SDFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	
R5F21245SDFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Factory programming product ⁽¹⁾
R5F21245SNXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNXXXLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	D version Factory programming product ⁽¹⁾
R5F21244SDXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	
R5F21245SDXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	

NOTE:

1. The user ROM is programmed before shipment.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽⁶⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾ 00100000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽⁵⁾	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register ⁽²⁾	VW0C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset or the LVD0ON bit in the OFS register is set to 0, and hardware reset.
5. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.2 SFR Information (2)⁽¹⁾

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC Interrupt Control Register ⁽²⁾	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage ⁽⁴⁾		–	–	0.1	V
V _{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V _{det0}	V
t _{rth}	External power V _{CC} rise gradient ⁽²⁾		20	–	–	mV/msec

NOTES:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if V_{CC} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD00N bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. t_{w(por1)} indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain t_{w(por1)} for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain t_{w(por1)} for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.

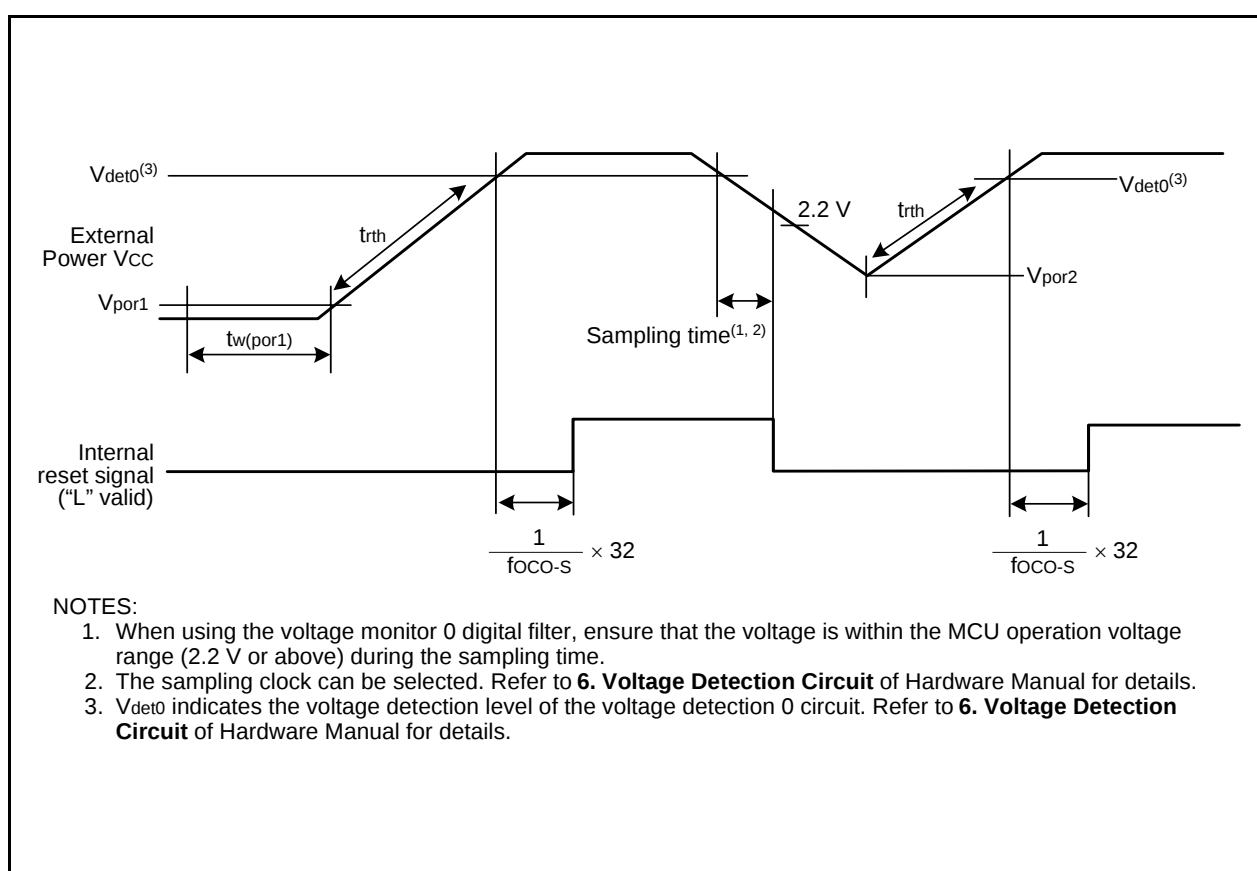
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
tsa	SSI slave access time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns
tor	SSI slave out open time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

Table 5.15 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
			I _{OH} = -200 μA	V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	Drive capacity HIGH I _{OH} = -1 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} = -500 μA	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 5 mA	—	—	2.0	V
			I _{OL} = 200 μA	—	—	0.45	V
		P2_0 to P2_7	Drive capacity HIGH I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity LOW I _{OL} = 5 mA	—	—	2.0	V
		XOUT	Drive capacity HIGH I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW I _{OL} = 500 μA	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}}, \overline{\text{INT3}}, \text{KI0}, \text{KI1}, \text{KI2}, \text{KI3}, \text{TRAIO}, \text{RXD0}, \text{RXD1}, \text{CLK0}, \text{CLK1}, \text{SSI}, \text{SCL}, \text{SDA}, \text{SSO}$		0.1	0.5	—	V
		$\overline{\text{RESET}}$		0.1	1.0	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5V	—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5V	—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5V	30	50	167	kΩ
R _{FXIN}	Feedback resistance	XIN		—	1.0	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN		—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

NOTE:

- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

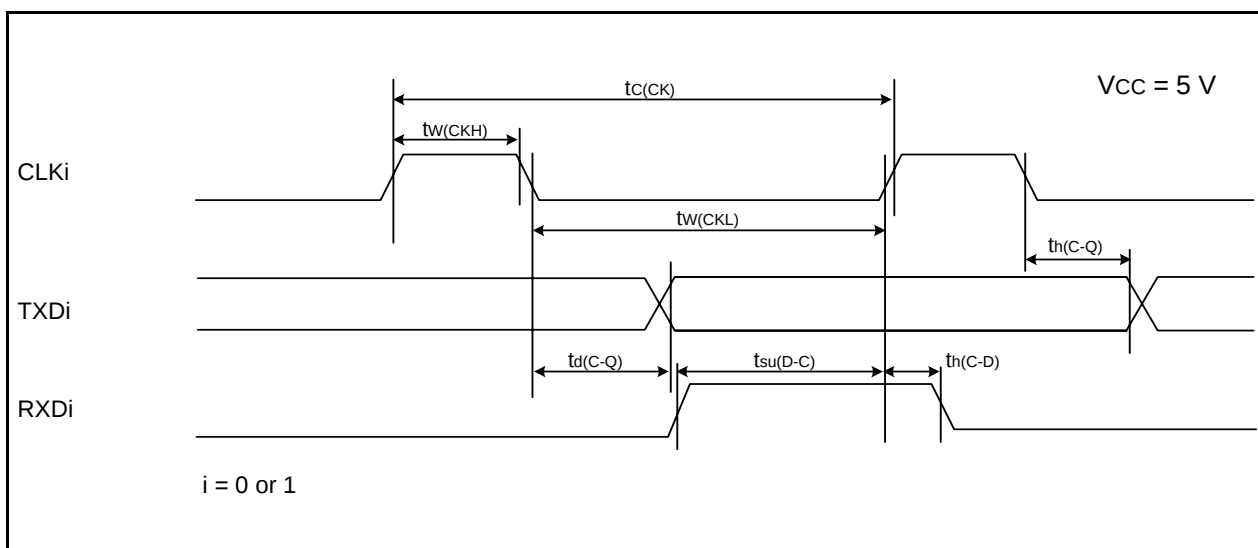
Table 5.16 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on FOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on FOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on FOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on FOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	μA

Table 5.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

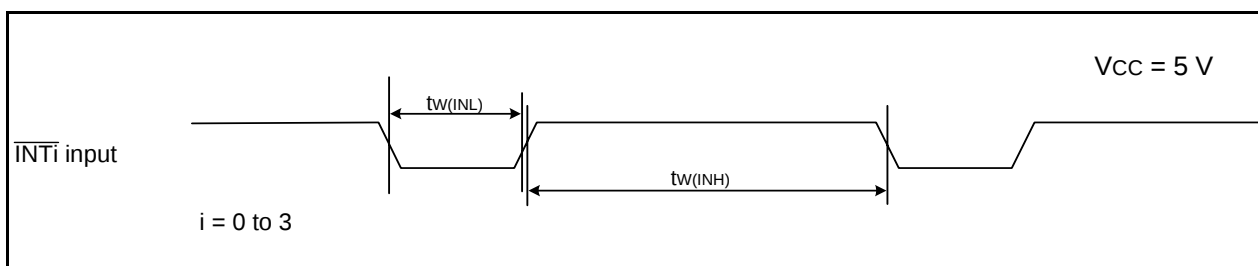
i = 0 or 1

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.21 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	250 ⁽²⁾	—	ns

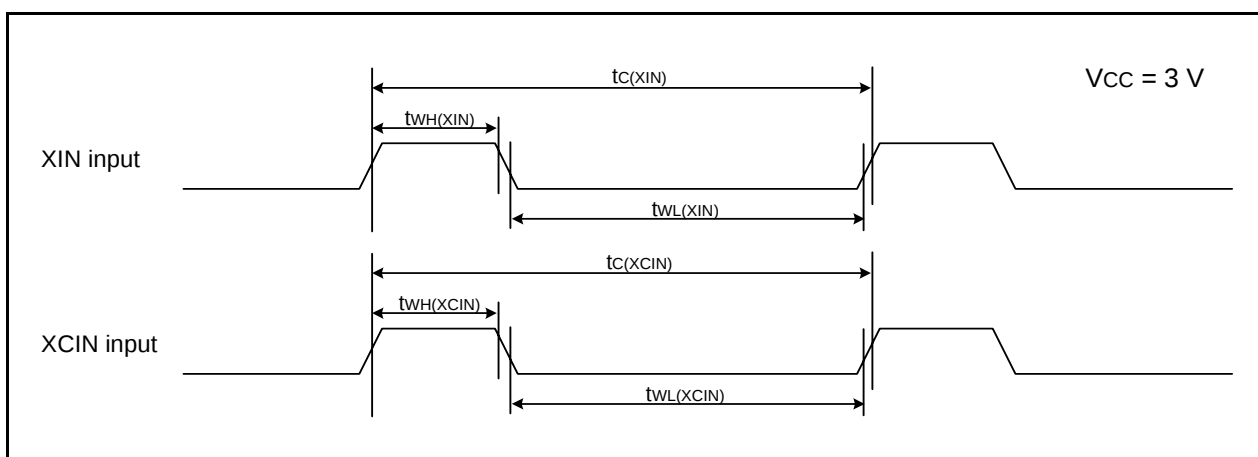
NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{op} = 25^\circ\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.24 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.12 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.25 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

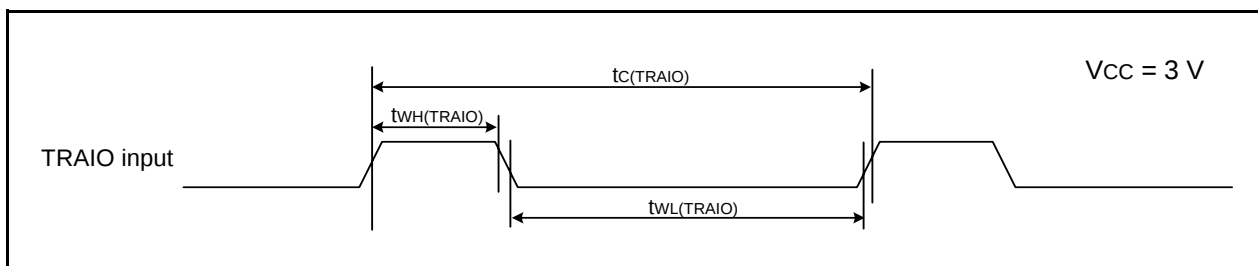
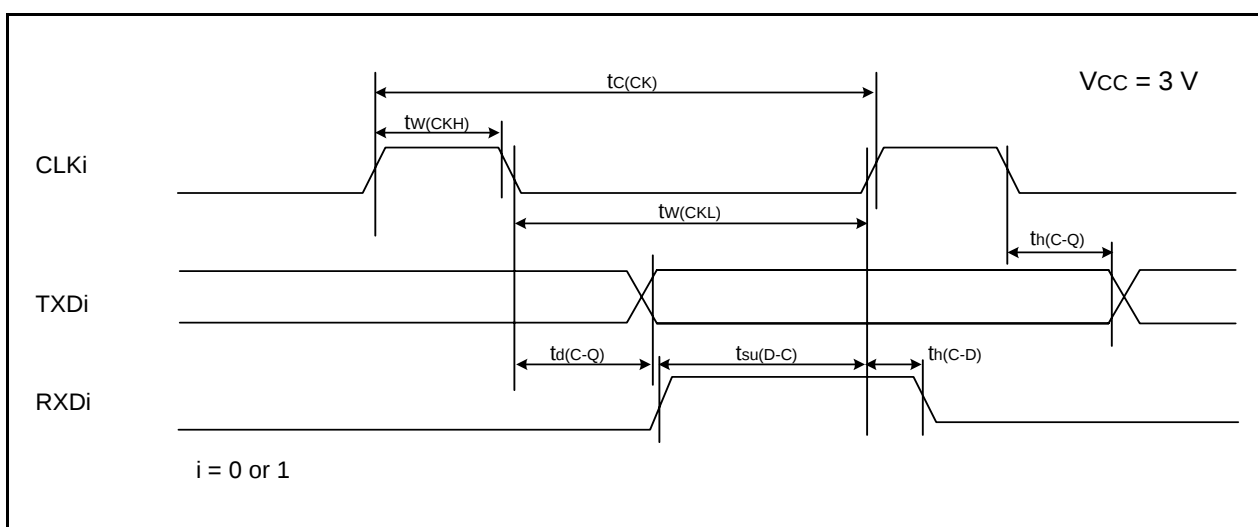
**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 1

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.27 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	380 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

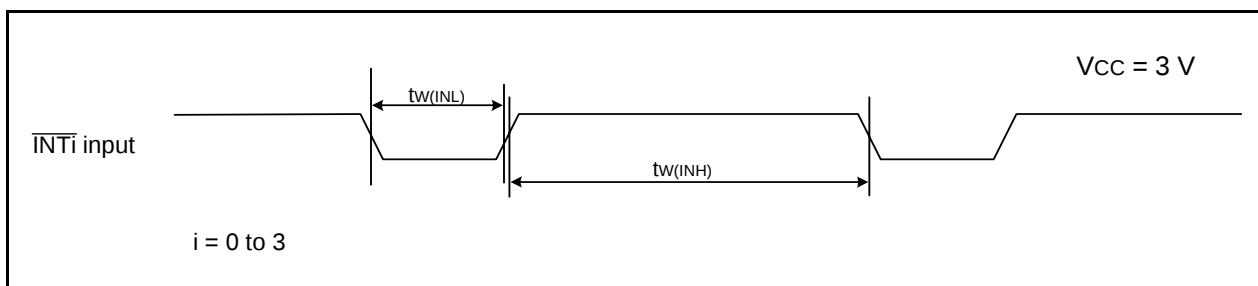
**Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V**

Table 5.28 Electrical Characteristics (5) [V_{CC} = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}}, \overline{\text{INT3}}, \text{KI0}, \text{KI1}, \text{KI2}, \text{KI3}, \text{TRAIO}, \text{RXD0}, \text{RXD1}, \text{CLK0}, \text{CLK1}, \text{SSI}, \text{SCL}, \text{SDA}, \text{SSO}$			0.05	0.3	—	V
		$\overline{\text{RESET}}$			0.05	0.15	—	V
I _{IH}	Input "H" current		V _I = 2.2 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		100	200	600	kΩ
R _{FXIN}	Feedback resistance	XIN			—	5	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	35	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

- V_{CC} = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

**Table 5.29 Electrical Characteristics (6) [V_{CC} = 2.2 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	–	3.5	–	mA
				1.5	–	mA
		High-speed on-chip oscillator mode	–	3.5	–	mA
				1.5	–	mA
		Low-speed on-chip oscillator mode	–	100	230	μA
				100	230	μA
		Low-speed clock mode	–	25	–	μA
				22	60	μA
		Wait mode	–	20	55	μA
				3.0	–	μA
				1.8	–	μA
				0.4	–	mA
		Increase during A/D converter operation	–	0.3	–	mA
				0.7	3.0	μA
		Stop mode	–	1.1	–	μA
				–	–	μA

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Sep 17, 2004	-	First Edition issued
0.02	Dec 10, 2004	All pages 2, 3 4 5, 6 7 8 9 15 16 19	Part Number revised. R8C/26 → R8C/24, R8C/27 → R8C/25 Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance - Serial Interface: I²C Bus Interface and Chip-select clock synchronous (SSU) added. - LIN Module added. - Interrupt: Internal factors revised; 10 → 11 - Note on Operating Ambient Temperature added. Figure 1.1 Block Diagram - LIN Module added. - Chip-select clock synchronous (SSU) is added to I²C Bus Interface. Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group Date and Development state revised. Figure 1.4 Pin Assignment P3_5/SCL → P3_5/SCL/SSCK, P3_3 → P3_3/SSI, P3_4/SDA → P3_4/SDA/SCS, P3_7 → P3_7/SSO, VSS/AVSS → VSS, XIN/P4_6 → P4_6/XIN, VCC/AVSS → VCC 12pin P1_7/TRAO/INT1 to 22pin P1_0/KIO/AN8 → 20pin P1_7/TRAO/INT1 to 30pin P1_0/KIO/AN8 Table 1.5 Pin Description - Analog Power Supply Input eliminated. - SSU added. Table 1.6 Pin Name Information by Pin Number added. Table 4.1 SFR Information (1) - 0031h: Voltage Detection Register 1 → Voltage Detection <u>A</u> Register 1 - 0032h: Voltage Detection Register 1 → Voltage Detection <u>A</u> Register 2 01000001b → 00100001b (Note 4) - 0036h: "(3), 01000001b (4)" eliminated. - 0038h: Voltage Monitor 0 Control Register (2), VW0C, 00001000b (3), 01000001b (4) added. Table 4.2 SFR Information (2) - 0048h: Timer RD0 Interrupt Control Register, RD0IC, XXXXX000b added. - 0049h: Timer RD Interrupt Control Register, RDIC → Timer RD1 Interrupt Control Register, RD1IC - 004Fh: IIC Interrupt Control Register, IIC → IIC/SSU Interrupt Control Register, IIC2IC Table 4.5 SFR Information (3) - 0106h: LIN Control Register, LINCR, 00h added. - 0107h: LIN Status Register, LINST, 00h added.

REVISION HISTORY

R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	7	Figure 1.4 Pin Assignment - Pin name revised; VSS → VSS/AVSS, VCC → VCC/AVCC, P1_5/RXD0/(TRAIO)/(INT1) → P1_5/RXD0/(TRAIO)/(INT1)⁽²⁾, P6_6/INT2/(TXD1) → P6_6/INT2/TXD1, P6_7/INT3/(RXD1) → P6_7/INT3/RXD1, P6_5 → P6_5/CLK1 - NOTE2 added
		8	Table 1.5 Pin Description - Analog Power Supply Input: line added - INT Interrupt Input: "INT0 Timer RD input pins. INT1 Timer RA input pins." added - Serial Interface: "CLK1" added "I²C Bus Interface (IIC)" → "I²C Bus Interface" "SSU" → "Clock Synchronous Serial I/O with Chip Select"
		9	Table 1.6 Pin Name Information by Pin Number revised - Pin Number 10: "VSS" → "VSS/AVSS" - Pin Number 12: "VCC" → "VCC/AVCC" - Pin Number 27: "INT0" added - Pin Number 28: "(TXD1)" → "TXD1" - Pin Number 29: "(RXD1)" → "RXD1" - Pin Number 35: "CLK1" added
		15	Tabel 4.1 SFR Information(1) revised: 0012h: X0h → 00h 0013h: XXXXX00b → 00h 0016h: X0h → 00h 0036h: Voltage Monitor 1 Control Register⁽²⁾ → Voltage Monitor 1 Control Register⁽⁵⁾ 0038h: 00001000b⁽³⁾, 01000001b⁽⁴⁾ → 0000X000b⁽³⁾, 0100X001b⁽⁴⁾ - NOTES2, 5: "the voltage monitor 1 reset" added - NOTE3: "voltage monitor 1 reset" → "voltage monitor 0 reset"
		16	Tabel 4.2 SFR Information(2) revised: 0048h: RD0IC → TRD0IC 0049h: RD1IC → TRD1IC 004Ah: REIC → TREIC 004Fh: SSU/IIC Interrupt Control Register, IIC2AIC → SSU/IIC Interrupt Control Register⁽²⁾, SSUAIC/IIC2AIC 0056h: RAIC → TRAIC 0058h: RBIC → TRBIC - NOTE2 added
		17	Tabel 4.3 SFR Information(3) revised: 00BCh: 00h → 00h/0000X000b
		18	Tabel 4.4 SFR Information(4) revised: 00D6h: 00000XXXb → 00h 00F5h: UART1 Function Select Register, U1SR, XXh added

REVISION HISTORY

R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.40	Jan 24, 2006	15	Table 4.1 SFR Information(1); 0024h: "TBD" → "When shipping" NOTES 3 and 4 revised
		19	Table 4.5 SFR Information (5); 0118h: "Timer RE Second Data Register" → "Timer RE Second Data Register / Counter Data Register" 0119h: "Timer RE Minute Data Register" → "Timer RE Minute Data Register / Compare Data Register" 0138h: "TRDMDR" → "TRDMR" 013Bh: "Timer RD Output Master Enable Register" → "Timer RD Output Master Enable Register 1"
		22	Table 5.1 Absolute Maximum Ratings; "Vcc" → "Vcc/AVcc" revised Table 5.2 Recommended Operating Conditions revised
		23	Table 5.3 A/D Converter Characteristics revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics revised
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical revised
		26	Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics revised Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics revised Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics revised
		28	Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.13 Power Supply Circuit Timing Characteristics revised
		29	Table 5.14 Timing Requirements of Clock Synchronous Serial I/O with Chip Select revised
		33	Table 5.15 Timing Requirements of I ² C bus Interface NOTE1 revised
		34	Table 5.16 Electrical Characteristics (1) [Vcc = 5 V] revised
		35	Table 5.17 Electrical Characteristics (2) [Vcc = 5 V] revised
		36	Table 5.18 XIN Input, XCIN Input revised
		37	Table 5.20 Serial Interface revised
		38	Table 5.22 Electrical Characteristics (3) [Vcc = 3 V] revised
		39	Table 5.23 Electrical Characteristics (4) [Vcc = 3 V] revised
		40	Table 5.24 XIN Input, XCIN Input revised
		41	Table 5.26 Serial Interface revised
		42	Table 5.28 Electrical Characteristics (5) [Vcc = 2.2 V] revised
		43	Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V] revised
		44	Table 5.30 XIN Input, XCIN Input revised Table 5.31 TRAIO Input, INT1 Input revised
		45	Table 5.32 Serial Interface revised Table 5.33 External Interrupt INTi (i = 0, 2, 3) Input

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
2.00	Jul 14, 2006	all pages	"PTLG0064JA-A (64F0G)" package added
		1	1. Overview; "... or a 64-pin molded-plastic FLGA." added
		2, 3	Table 1.1 Functions and Specifications for R8C/24 Group, Table 1.2 Functions and Specifications for R8C/25 Group; Package: "64-pin molded-plastic FLGA" added
		5	Table 1.3 Product Information for R8C/24 Group, Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group, Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group revised
		7	Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View); NOTE3 revised
		8	Figure 1.5 PTLG0064JA-A Package Pin Assignments added
		14	Figure 3.1 Memory Map of R8C/24 Group revised
		15	Figure 3.2 Memory Map of R8C/25 Group revised
		23	Table 5.1 Absolute Maximum Ratings; NOTE1 added
		47	Package Dimensions; "PTLG0064JA-A (64F0G)" added
3.00	Feb 29, 2008	all pages	Y version added Factory programming product added
		2, 3	Table 1.1, Table 1.2 Clock; "Real-time clock (timer RE)" added
		5, 7	Table 1.3, Table 1.4 revised
		6, 8	Figure 1.2, Figure 1.3; ROM number "XXX" added
		16, 17	Figure 3.1, Figure 3.2; "Expanded area" deleted
		18	Table 4.1 revised
		26	Table 5.2 NOTE2 revised
		32	Table 5.10; revised, NOTE4 added Table 5.11; Oscillation stability time: Condition "Vcc = 5.0 V, Topr = 25°C" deleted
		38	Table 5.15; I _{IH} , I _L , R _{PULLUP} Condition: "Vcc = 5V" added
		39	Table 5.16; Condition: High-speed on-chip oscillator mode revised
		40	Table 5.17 added
		41	Figure 5.8 revised
		43	Table 5.22; I _{IH} , I _L , R _{PULLUP} Condition: "Vcc = 3V" added
		44	Table 5.23; Condition "Increase during A/D converter operation" added
		45	Figure 5.12 revised
		48	Table 5.29; Condition "Increase during A/D converter operation" added
		49	Figure 5.16 revised