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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

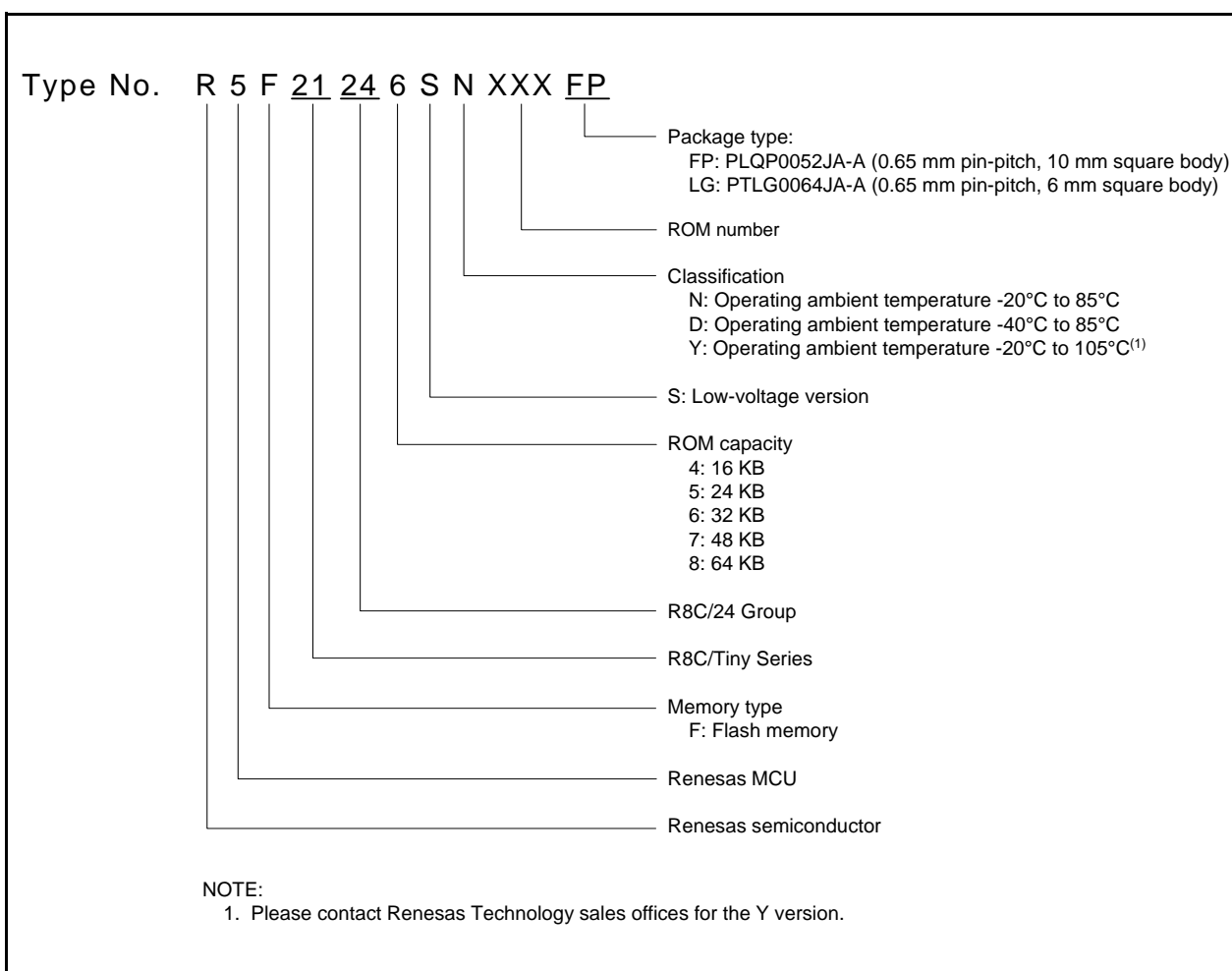
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21246sdfp-v2">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21246sdfp-v2</a>

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**Figure 1.2** Type Number, Memory Size, and Package of R8C/24 Group

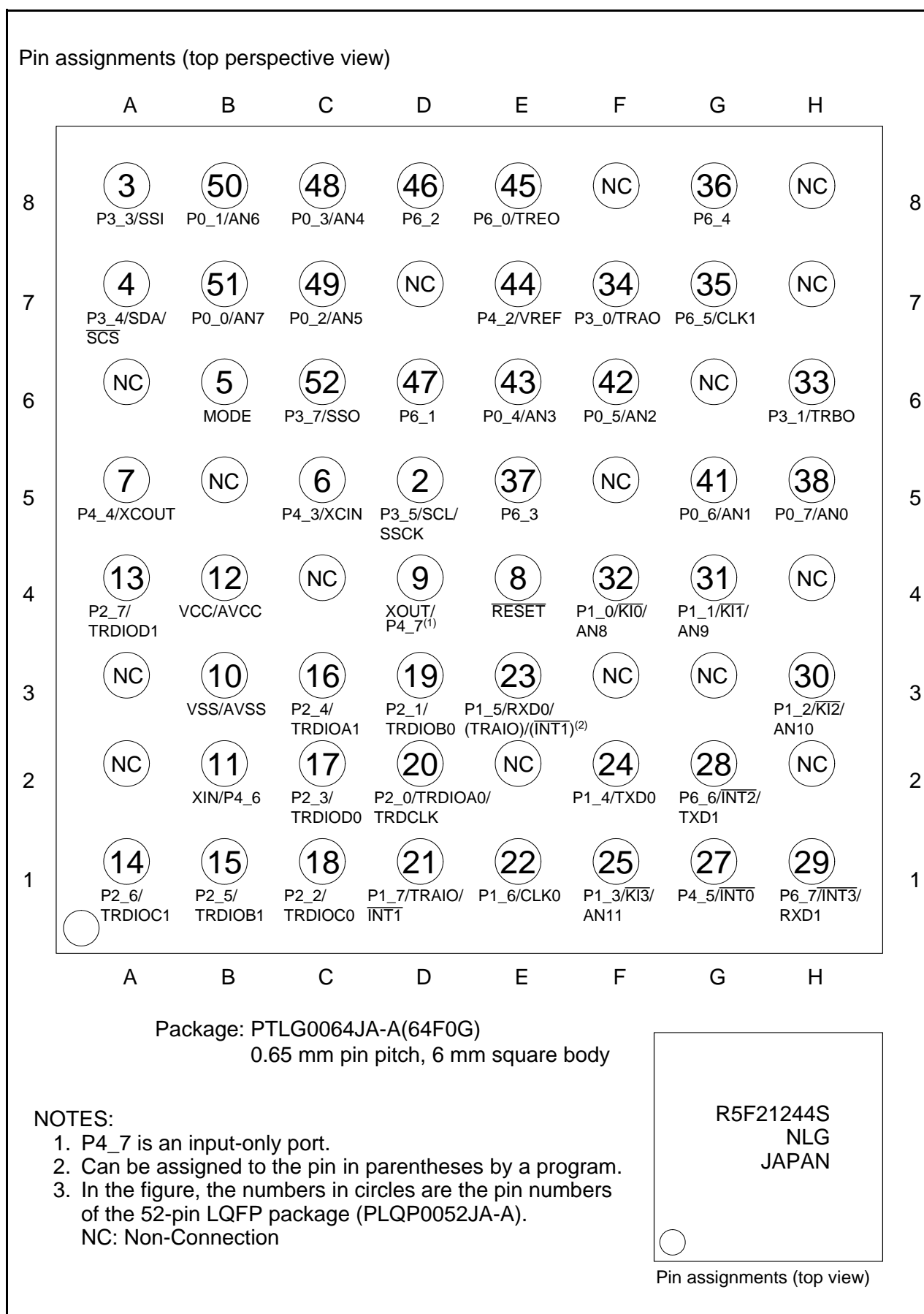


Figure 1.5 PTLG0064JA-A Package Pin Assignments

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

### **2.8.7 Interrupt Enable Flag (I)**

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### **2.8.8 Stack Pointer Select Flag (U)**

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### **2.8.9 Processor Interrupt Priority Level (IPL)**

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### **2.8.10 Reserved Bit**

If necessary, set to 0. When read, the content is undefined.

### 3. Memory

#### 3.1 R8C/24 Group

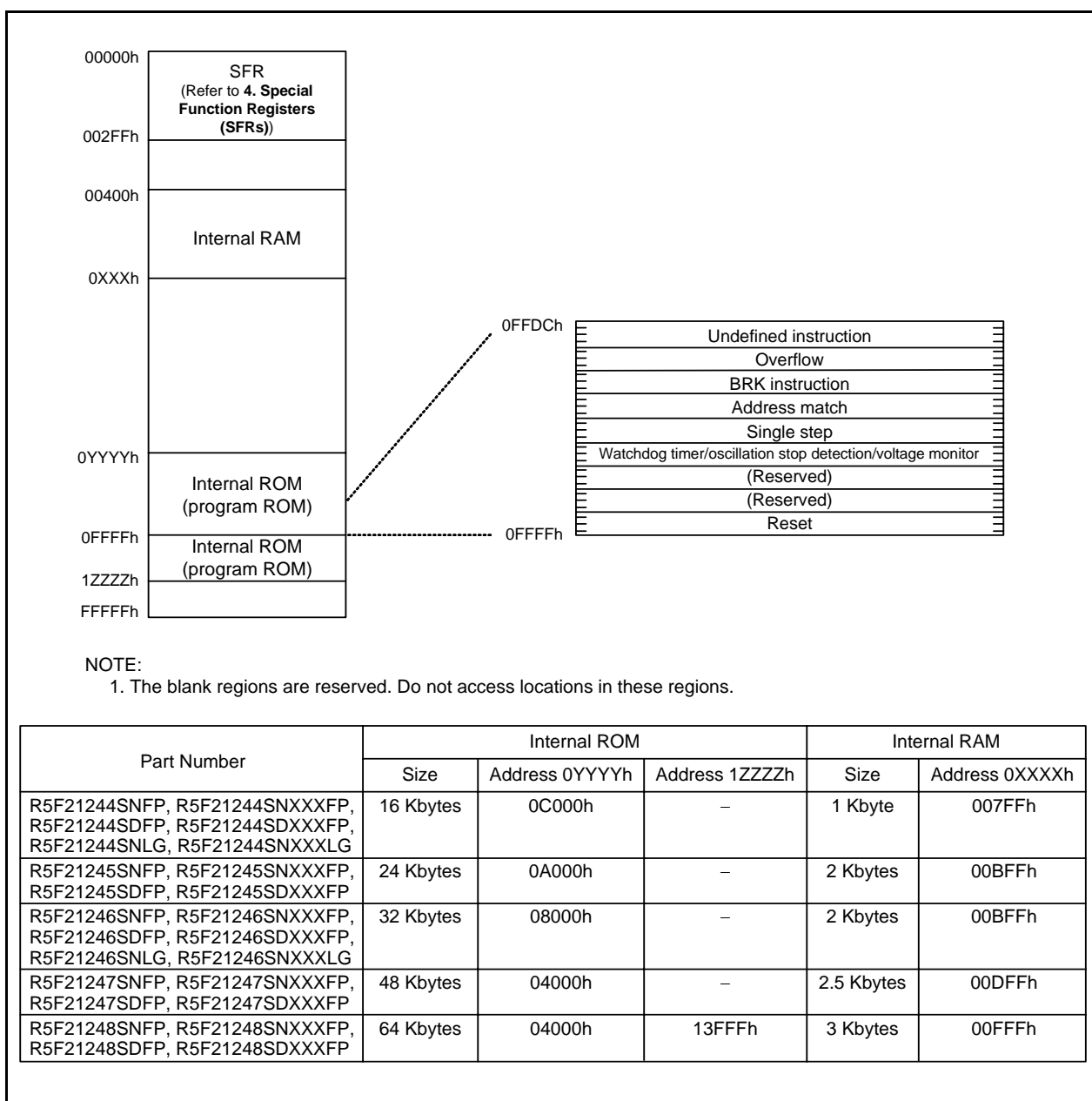
Figure 3.1 is a Memory Map of R8C/24 Group. The R8C/24 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM area is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



**Figure 3.1 Memory Map of R8C/24 Group**

### 3.2 R8C/25 Group

Figure 3.2 is a Memory Map of R8C/25 Group. The R8C/25 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

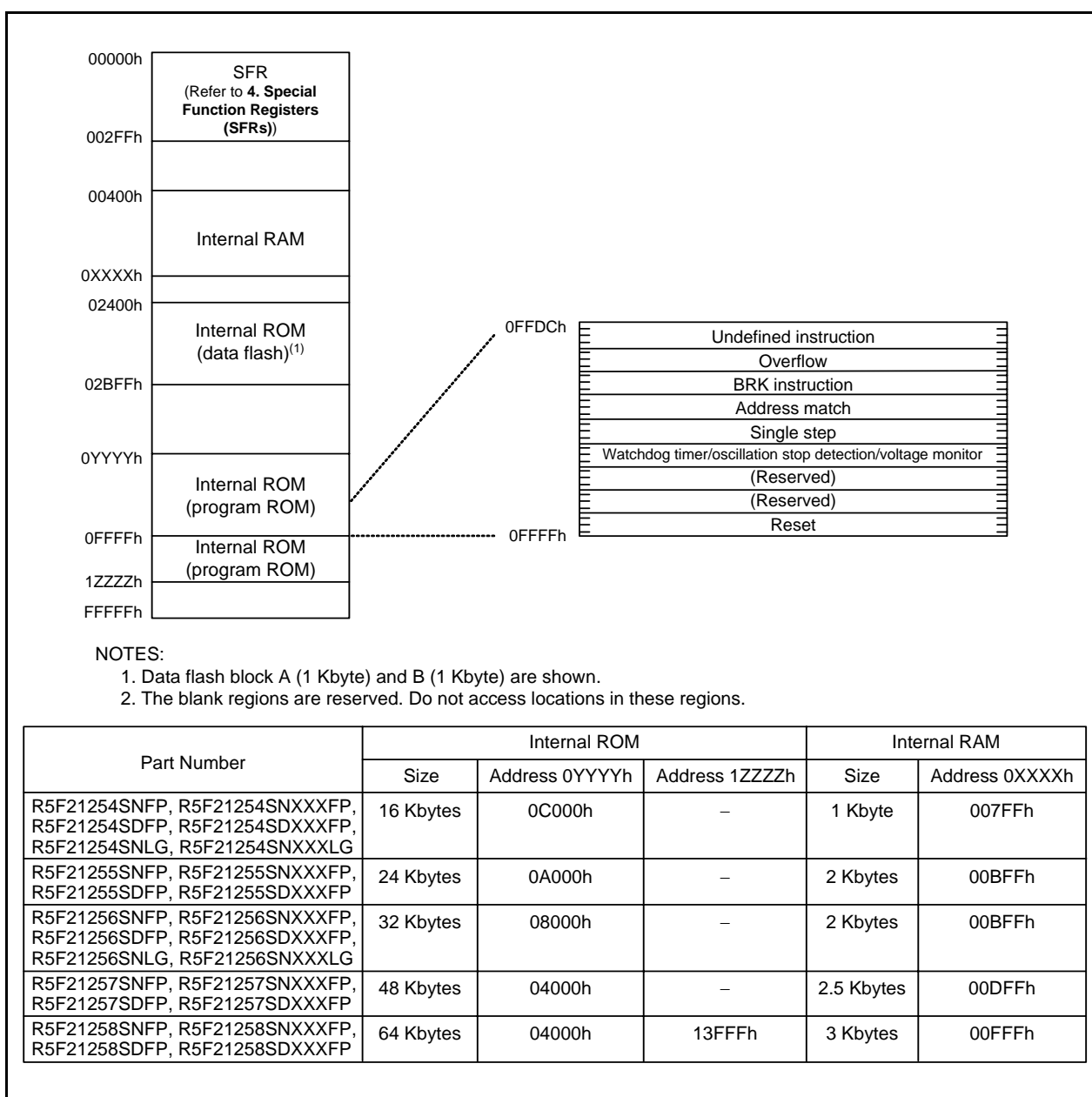


Figure 3.2 Memory Map of R8C/25 Group



## 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

**Table 4.1 SFR Information (1)(1)**

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b <sup>(6)</sup>
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0030h			
0031h	Voltage Detection Register 1 <sup>(2)</sup>	VCA1	00001000b
0032h	Voltage Detection Register 2 <sup>(2)</sup>	VCA2	00h <sup>(3)</sup> 00100000b <sup>(4)</sup>
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register <sup>(5)</sup>	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register <sup>(5)</sup>	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register <sup>(2)</sup>	VW0C	0000X000b <sup>(3)</sup> 0100X001b <sup>(4)</sup>
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

### NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset or the LVD0ON bit in the OFS register is set to 0, and hardware reset.
5. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

**Table 4.6 SFR Information (6)<sup>(1)</sup>**

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIOA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIOA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

**Table 5.2 Recommended Operating Conditions**

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V <sub>CC</sub> /AV <sub>CC</sub>	Supply voltage			2.2	—	5.5	V
V <sub>SS</sub> /AV <sub>SS</sub>	Supply voltage			—	0	—	V
V <sub>IH</sub>	Input "H" voltage			0.8 V <sub>CC</sub>	—	V <sub>CC</sub>	V
V <sub>IL</sub>	Input "L" voltage			0	—	0.2 V <sub>CC</sub>	V
I <sub>OH</sub> (sum)	Peak sum output "H" current	Sum of all pins I <sub>OH</sub> (peak)		—	—	-160	mA
I <sub>OH</sub> (sum)	Average sum output "H" current	Sum of all pins I <sub>OH</sub> (avg)		—	—	-80	mA
I <sub>OH</sub> (peak)	Peak output "H" current	Except P2_0 to P2_7		—	—	-10	mA
		P2_0 to P2_7		—	—	-40	mA
I <sub>OH</sub> (avg)	Average output "H" current	Except P2_0 to P2_7		—	—	-5	mA
		P2_0 to P2_7		—	—	-20	mA
I <sub>OL</sub> (sum)	Peak sum output "L" current	Sum of all pins I <sub>OL</sub> (peak)		—	—	160	mA
I <sub>OL</sub> (sum)	Average sum output "L" current	Sum of all pins I <sub>OL</sub> (avg)		—	—	80	mA
I <sub>OL</sub> (peak)	Peak output "L" current	Except P2_0 to P2_7		—	—	10	mA
		P2_0 to P2_7		—	—	40	mA
I <sub>OL</sub> (avg)	Average output "L" current	Except P2_0 to P2_7		—	—	5	mA
		P2_0 to P2_7		—	—	20	mA
f(XIN)	XIN clock input oscillation frequency		3.0 V ≤ V <sub>CC</sub> ≤ 5.5 V	0	—	20	MHz
			2.7 V ≤ V <sub>CC</sub> < 3.0 V	0	—	10	MHz
			2.2 V ≤ V <sub>CC</sub> < 2.7 V	0	—	5	MHz
f(XCIN)	XCIN clock input oscillation frequency		2.2 V ≤ V <sub>CC</sub> ≤ 5.5 V	0	—	70	kHz
—	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V <sub>CC</sub> ≤ 5.5 V	0	—	20	MHz
			2.7 V ≤ V <sub>CC</sub> < 3.0 V	0	—	10	MHz
			2.2 V ≤ V <sub>CC</sub> < 2.7 V	0	—	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	—	125	—	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V <sub>CC</sub> ≤ 5.5 V	—	—	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V	—	—	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V <sub>CC</sub> ≤ 5.5 V	—	—	5	MHz

## NOTES:

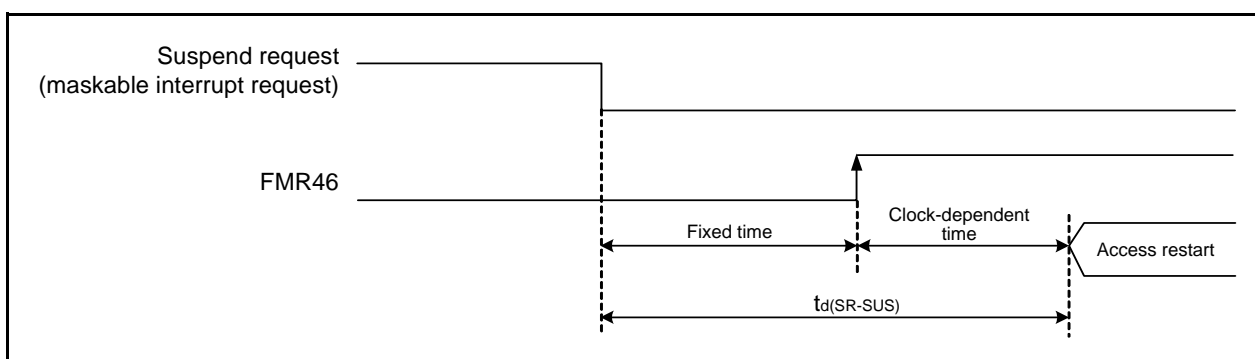
1. V<sub>CC</sub> = 2.2 to 5.5 V at T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

**Table 5.4 Flash Memory (Program ROM) Electrical Characteristics**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance <sup>(2)</sup>	R8C/24 Group	100 <sup>(3)</sup>	–	–	times
		R8C/25 Group	1,000 <sup>(3)</sup>	–	–	times
–	Byte program time		–	50	400	μs
–	Block erase time		–	0.4	9	s
t <sub>d</sub> (SR-SUS)	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time <sup>(7)</sup>	Ambient temperature = 55°C	20	–	–	year

**NOTES:**

1. V<sub>CC</sub> = 2.7 to 5.5 V at T<sub>opr</sub> = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance  
The programming and erasure endurance is defined on a per-block basis.  
If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

**Figure 5.2 Time delay until Suspend****Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det0</sub>	Voltage detection level		2.2	2.3	2.4	V
—	Voltage detection circuit self power consumption	VCA25 = 1, V <sub>CC</sub> = 5.0 V	—	0.9	—	μA
t <sub>d(E-A)</sub>	Waiting time until voltage detection circuit operation starts <sup>(2)</sup>		—	—	300	μs
V <sub>ccmin</sub>	MCU operating voltage minimum value		2.2	—	—	V

**NOTES:**

1. The measurement condition is V<sub>CC</sub> = 2.2 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

**Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det1</sub>	Voltage detection level		2.70	2.85	3.00	V
—	Voltage monitor 1 interrupt request generation time <sup>(2)</sup>		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V <sub>CC</sub> = 5.0 V	—	0.6	—	μA
t <sub>d(E-A)</sub>	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>		—	—	100	μs

**NOTES:**

1. The measurement condition is V<sub>CC</sub> = 2.2 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V<sub>det1</sub>.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det2</sub>	Voltage detection level		3.3	3.6	3.9	V
—	Voltage monitor 2 interrupt request generation time <sup>(2)</sup>		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, V <sub>CC</sub> = 5.0 V	—	0.6	—	μA
t <sub>d(E-A)</sub>	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>		—	—	100	μs

**NOTES:**

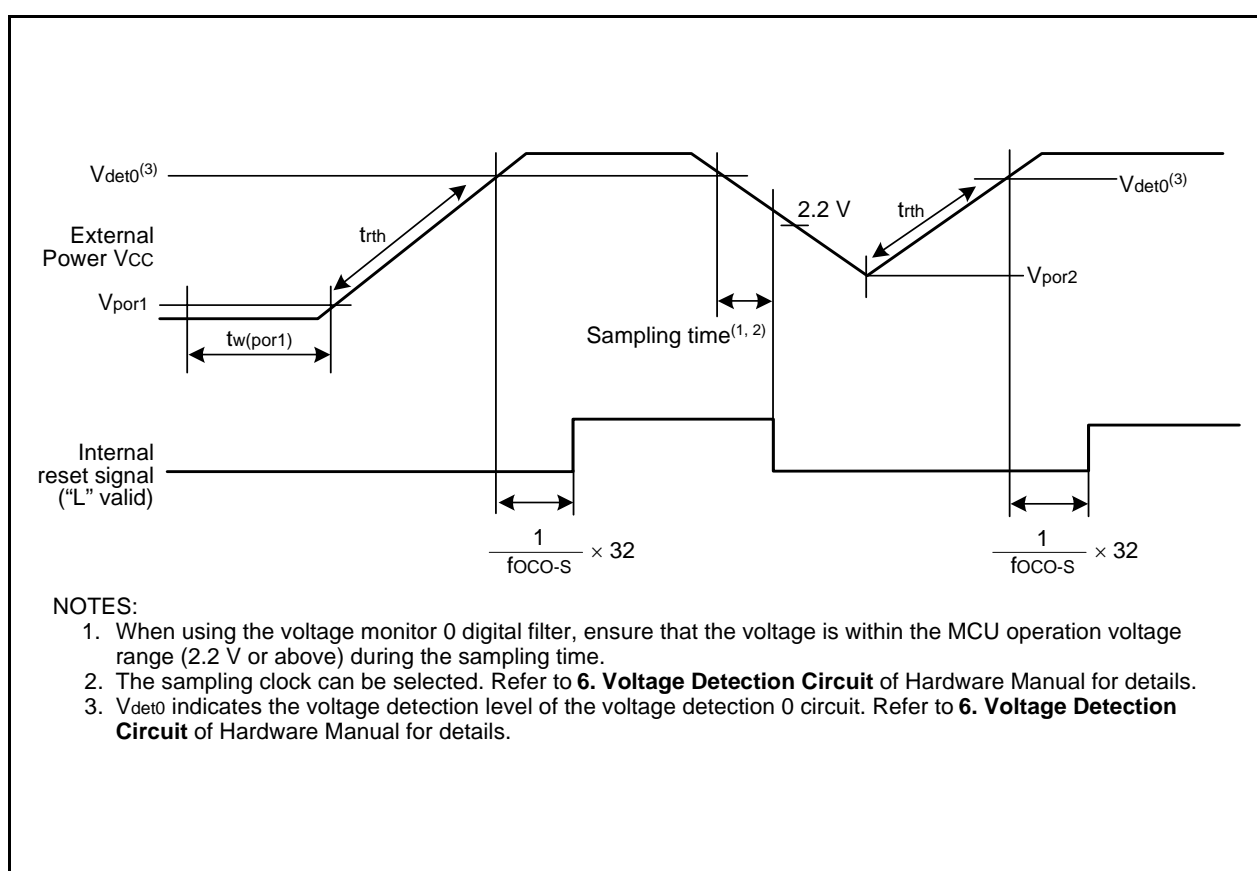
1. The measurement condition is V<sub>CC</sub> = 2.2 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V<sub>det2</sub>.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

**Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics<sup>(3)</sup>**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>por1</sub>	Power-on reset valid voltage <sup>(4)</sup>		–	–	0.1	V
V <sub>por2</sub>	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V <sub>det0</sub>	V
t <sub>rth</sub>	External power V <sub>CC</sub> rise gradient <sup>(2)</sup>		20	–	–	mV/msec

**NOTES:**

1. The measurement condition is T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V<sub>CC</sub> rise gradient) does not apply if V<sub>CC</sub> ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. t<sub>w(por1)</sub> indicates the duration the external power V<sub>CC</sub> must be held below the effective voltage (V<sub>por1</sub>) to enable a power on reset. When turning on the power for the first time, maintain t<sub>w(por1)</sub> for 30 s or more if -20°C ≤ T<sub>opr</sub> ≤ 85°C, maintain t<sub>w(por1)</sub> for 3,000 s or more if -40°C ≤ T<sub>opr</sub> < -20°C.

**NOTES:**

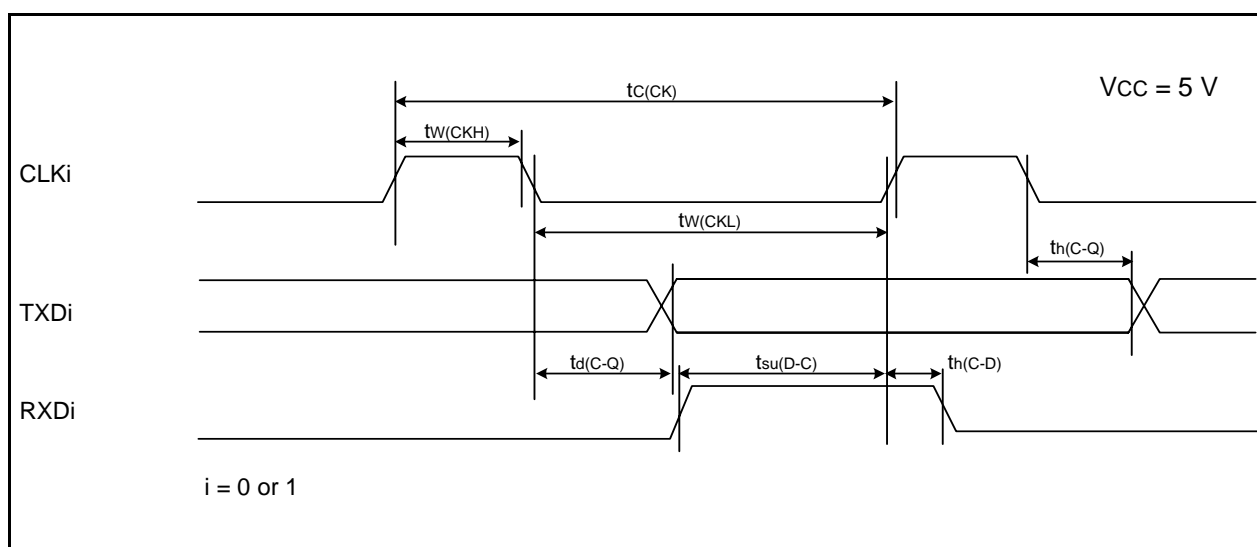
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V<sub>det0</sub> indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

**Table 5.20 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

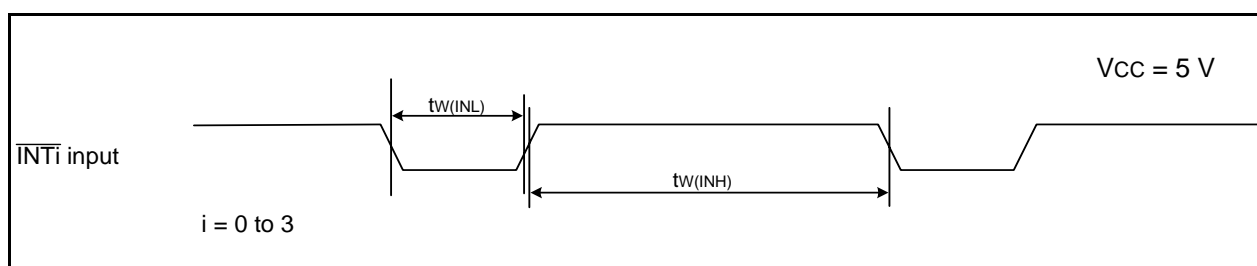
i = 0 or 1

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.21 External Interrupt  $\overline{INTi}$  (i = 0 to 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	250 <sup>(1)</sup>	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	250 <sup>(2)</sup>	—	ns

**NOTES:**

1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.11 External Interrupt  $\overline{INTi}$  Input Timing Diagram when Vcc = 5 V**

**Table 5.23 Electrical Characteristics (4) [Vcc = 3 V]**  
**(T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I <sub>cc</sub>	Power supply current (V <sub>cc</sub> = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V <sub>ss</sub>	High-speed clock mode	—	6	—	mA
				2	—	mA
		High-speed on-chip oscillator mode	—	5	9	mA
				2	—	mA
		Low-speed on-chip oscillator mode	—	130	300	μA
				130	300	μA
		Wait mode	—	25	70	μA
				23	55	μA
		Increase during A/D converter operation	—	0.9	—	mA
				0.5	—	mA
		Stop mode	—	0.7	3.0	μA
				1.1	—	μA



**Table 5.28 Electrical Characteristics (5) [V<sub>CC</sub> = 2.2 V]**

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V <sub>OH</sub>	Output "H" voltage	Except P2_0 to P2_7, XOUT	I <sub>OH</sub> = -1 mA		V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
		P2_0 to P2_7	Drive capacity HIGH	I <sub>OH</sub> = -2 mA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
			Drive capacity LOW	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
		XOUT	Drive capacity HIGH	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
			Drive capacity LOW	I <sub>OH</sub> = -50 μA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
V <sub>OL</sub>	Output "L" voltage	Except P2_0 to P2_7, XOUT	I <sub>OL</sub> = 1 mA		—	—	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I <sub>OL</sub> = 2 mA	—	—	0.5	V
			Drive capacity LOW	I <sub>OL</sub> = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I <sub>OL</sub> = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I <sub>OL</sub> = 50 μA	—	—	0.5	V
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}}, \overline{\text{INT3}}, \text{KI0}, \text{KI1}, \text{KI2}, \text{KI3}, \text{TRAIO}, \text{RXD0}, \text{RXD1}, \text{CLK0}, \text{CLK1}, \text{SSI}, \text{SCL}, \text{SDA}, \text{SSO}$			0.05	0.3	—	V
		$\overline{\text{RESET}}$			0.05	0.15	—	V
I <sub>IH</sub>	Input "H" current		V <sub>I</sub> = 2.2 V		—	—	4.0	μA
I <sub>IL</sub>	Input "L" current		V <sub>I</sub> = 0 V		—	—	-4.0	μA
R <sub>PULLUP</sub>	Pull-up resistance		V <sub>I</sub> = 0 V		100	200	600	kΩ
R <sub>FXIN</sub>	Feedback resistance	XIN			—	5	—	MΩ
R <sub>FXCIN</sub>	Feedback resistance	XCIN			—	35	—	MΩ
V <sub>RAM</sub>	RAM hold voltage		During stop mode		1.8	—	—	V

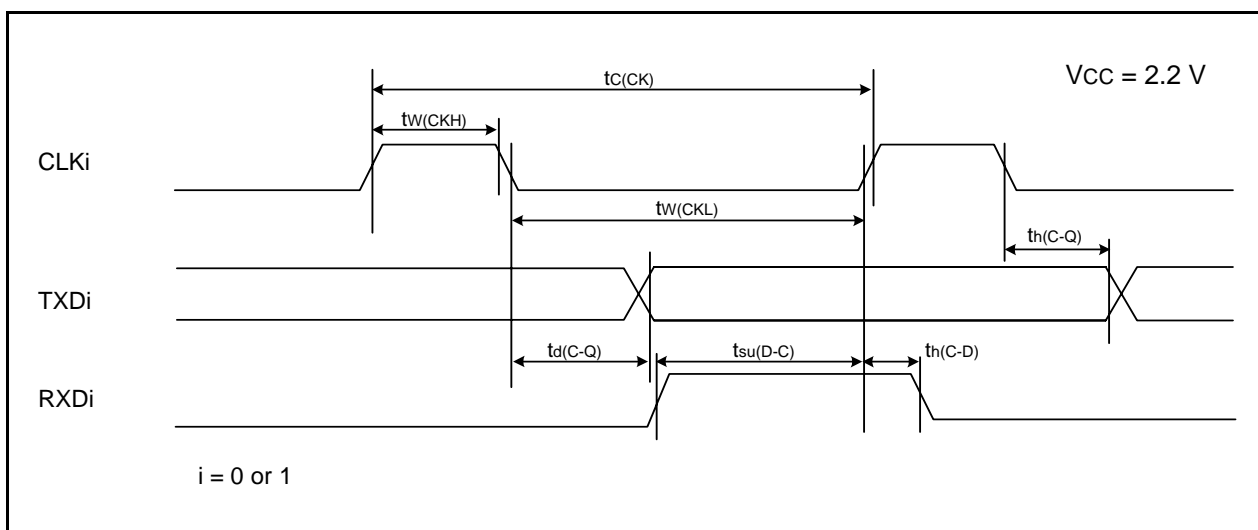
## NOTE:

- V<sub>CC</sub> = 2.2 V at T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

**Table 5.32 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input “H” width	400	—	ns
$t_{w(CKL)}$	CLKi input “L” width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

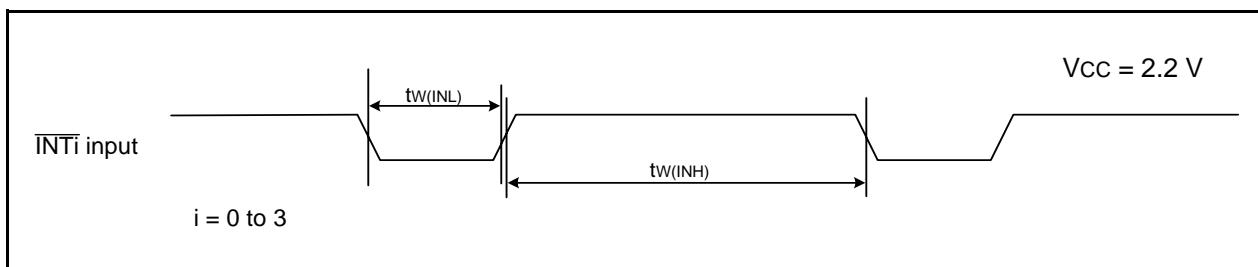
i = 0 or 1

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.33 External Interrupt  $\overline{INTi}$  (i = 0 to 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input “H” width	1000 <sup>(1)</sup>	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input “L” width	1000 <sup>(2)</sup>	—	ns

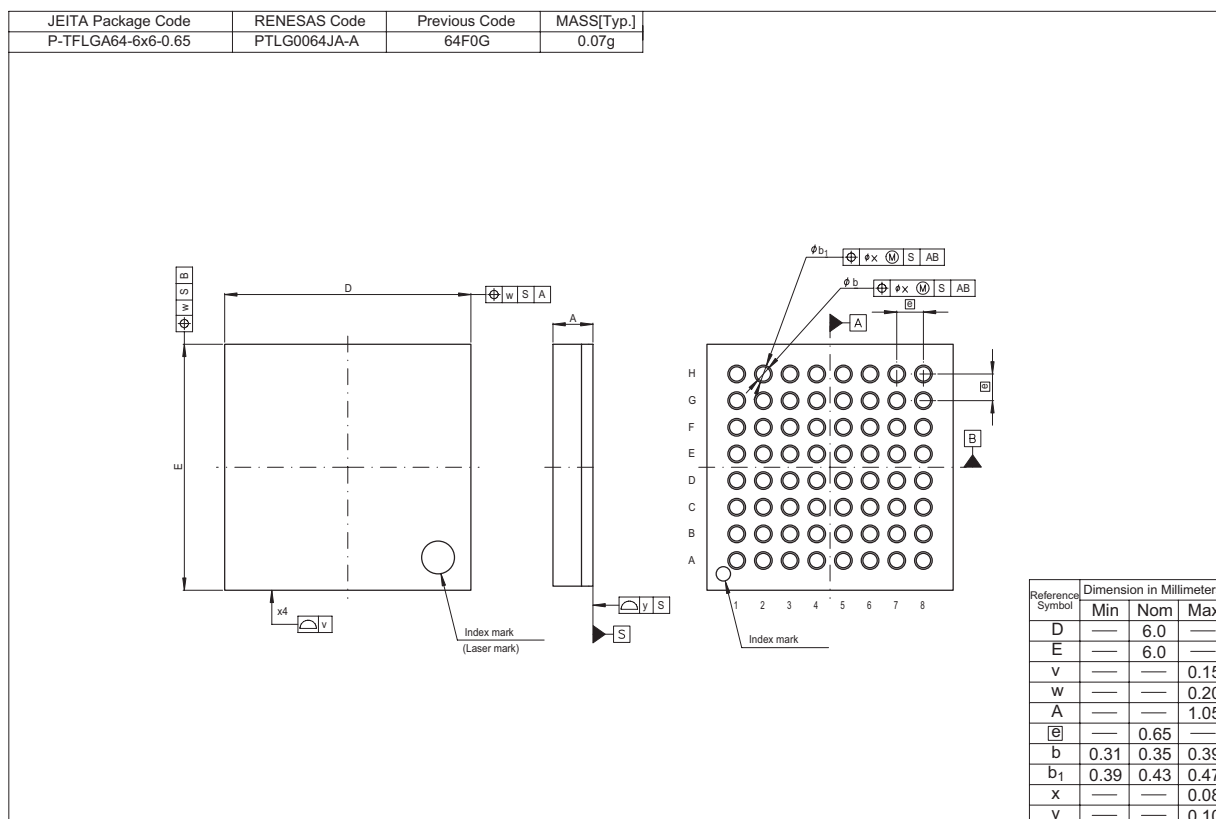
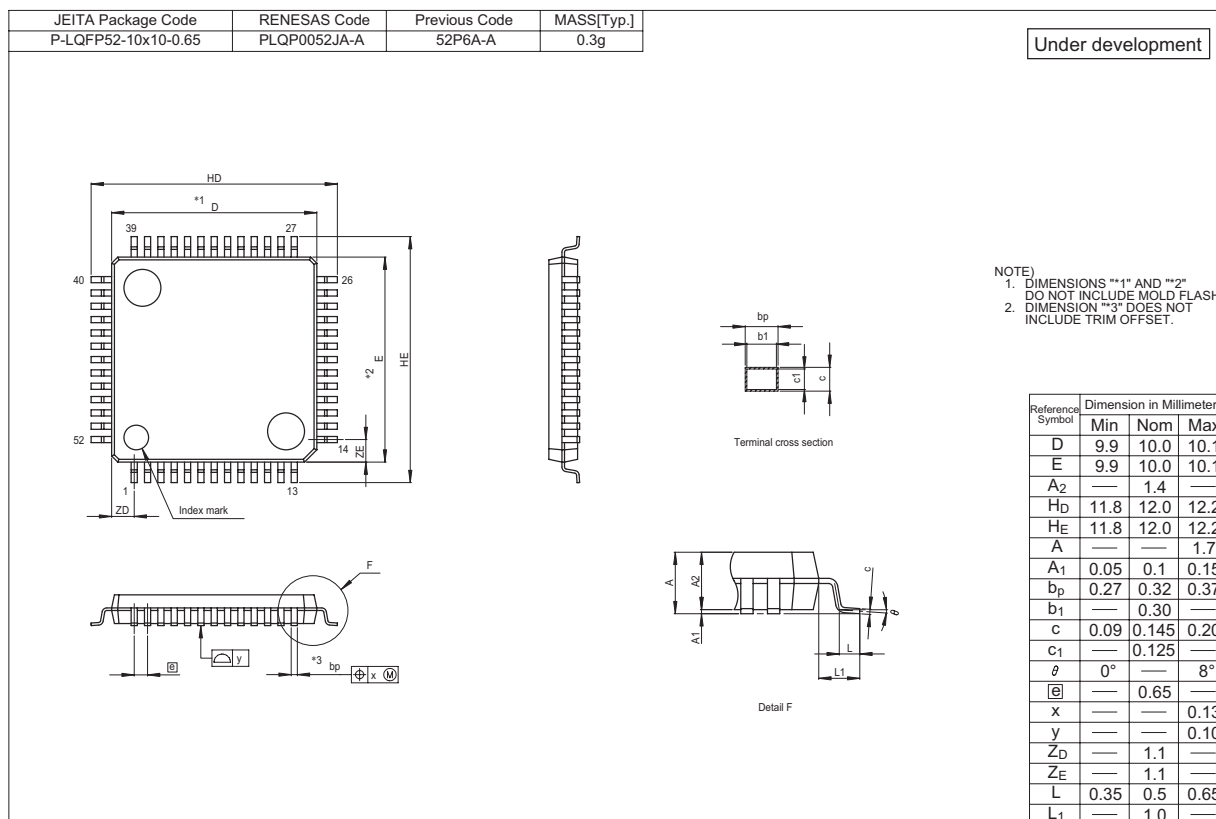
## NOTES:

1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 External Interrupt  $\overline{INTi}$  Input Timing Diagram when Vcc = 2.2 V**

## Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Sep 17, 2004	-	First Edition issued
0.02	Dec 10, 2004	All pages	Part Number revised. R8C/26 → R8C/24, R8C/27 → R8C/25
		2, 3	Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance - Serial Interface: I <sup>2</sup> C Bus Interface and Chip-select clock synchronous (SSU) added. - LIN Module added. - Interrupt: Internal factors revised; 10 → 11 - Note on Operating Ambient Temperature added.
		4	Figure 1.1 Block Diagram - LIN Module added. - Chip-select clock synchronous (SSU) is added to I <sup>2</sup> C Bus Interface.
		5, 6	Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group Date and Development state revised.
		7	Figure 1.4 Pin Assignment P3_5/SCL → P3_5/SCL/SSCK, P3_3 → P3_3/SSI, P3_4/SDA → P3_4/SDA/SCS, P3_7 → P3_7/SSO, VSS/AVSS → VSS, XIN/P4_6 → P4_6/XIN, VCC/AVSS → VCC 12pin P1_7/TRAIO/INT1 to 22pin P1_0/KIO/AN8 → 20pin P1_7/TRAIO/INT1 to 30pin P1_0/KIO/AN8
		8	Table 1.5 Pin Description - Analog Power Supply Input eliminated. - SSU added.
		9	Table 1.6 Pin Name Information by Pin Number added.
		15	Table 4.1 SFR Information (1) - 0031h: Voltage Detection Register 1 → Voltage Detection <u>A</u> Register 1 - 0032h: Voltage Detection Register 1 → Voltage Detection <u>A</u> Register 2 01000001b → 00100001b (Note 4) - 0036h: "(3), 01000001b (4)" eliminated. - 0038h: Voltage Monitor 0 Control Register (2), VW0C, 00001000b (3), 01000001b (4) added.
		16	Table 4.2 SFR Information (2) - 0048h: Timer RD0 Interrupt Control Register, RD0IC, XXXXX000b added. - 0049h: Timer RD Interrupt Control Register, RDIC → Timer RD1 Interrupt Control Register, RD1IC - 004Fh: IIC Interrupt Control Register, IIC → IIC/SSU Interrupt Control Register, IIC2IC
		19	Table 4.5 SFR Information (3) - 0106h: LIN Control Register, LINCR, 00h added. - 0107h: LIN Status Register, LINST, 00h added.

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	19	Tabel 4.5 SFR Information(5) revised: • 0118h : Timer RE Second Data Register/Counter Register → Timer RE Second Data Register/Counter Data Register
		20	Tabel 4.6 SFR Information(6) revised: • 0145h           POCR0     →   TRDPOCR0 • 0146h, 0147h   TRDCNT0 →   TRD0 • 0148h, 0149h   GRA0     →   TRDGRA0 • 014Ah, 014Bh   GRB0     →   TRDGRB0 • 014Ch, 014Dh   GRC0     →   TRDGRC0 • 014Eh, 014Fh   GRD0     →   TRDGRD0 • 0155h           POCR1     →   TRDPOCR1 • 0156h, 0157h   TRDCNT1 →   TRD1 • 0158h, 0159h   GRA1     →   TRDGRA1 • 015Ah, 015Bh   GRB1     →   TRDGRB1 • 015Ch, 015Dh   GRC1     →   TRDGRC1 • 015Eh, 015Fh   GRD1     →   TRDGRD1
		21	Tabel 4.7 SFR Information(7) revised: • 01B5h: 01000101b → 1000000Xb • 01B7h: XX000001b → 00000001b • FFFFh: (Note 2) added
		22 to 44	5. Electrical Characteristics added
0.40	Jan 24, 2006	all pages	• “Preliminary” deleted • Symbol name “TRDMDR” → “TRDMR”, “SSUAIC” → “SSUIC”, and “IIC2AIC” → “IICIC” revised • Pin name “TCLK” → “TRDCLK” revised
		2	Table 1.1 Functions and Specifications for R8C/24 Group revised
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; “Peripheral Functions” added, “System Clock Generation” → “System Clock Generator” revised
		5	Table 1.3 Product Information for R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group revised
		7	Figure 1.4 Pin Assignments (Top View) “TCLK” → “TRDCLK” revised
		8	Table 1.5 Pin Functions “TCLK” → “TRDCLK” revised
		9	Table 1.6 Pin Name Information by Pin Number; “TCLK” → “TRDCLK” revised
		10	Figure 2.1 CPU Registers; “Reserved Area” → “Reserved Bit” revised
		12	2.8.10 Reserved Area; “Reserved Area” → “Reserved bit” revised
		13	Figure 3.1 Memory Map of R8C/24 Group; “Program area” → “program ROM” revised
		14	3.2 R8C/25 Group, Figure 3.2 Memory Map of R8C/25 Group; “Data area” → “data flash”, “Program area” → “program ROM” revised