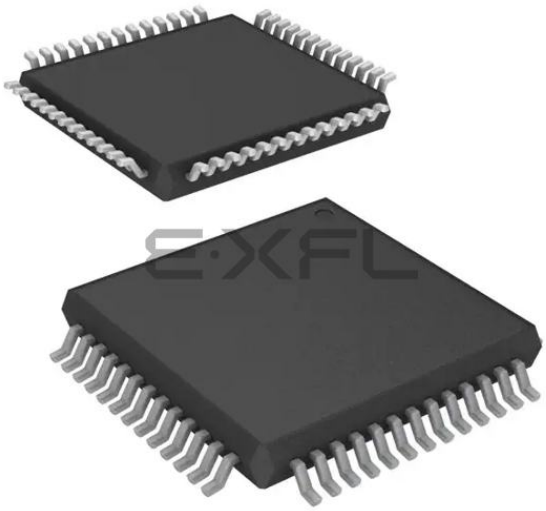

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21248sdfp-v2

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/24 Group and Table 1.2 outlines the Functions and Specifications for R8C/25 Group.

Table 1.1 Functions and Specifications for R8C/24 Group

Item			Specification
CPU	Number of fundamental instructions		89 instructions
	Minimum instruction execution time		50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)
	Operating mode		Single-chip
	Address space		1 Mbyte
	Memory capacity		Refer to **Table 1.3 Product Information for R8C/24 Group**
Peripheral Functions	Ports		I/O ports: 41 pins, Input port: 3 pins
	LED drive ports		I/O ports: 8 pins
	Timers		Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits × 2 channels (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function
	Serial interfaces		2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface		1 channel I²C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module		Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter		10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer		15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupts		Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels
	Clock	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz)
			Real-time clock (timer RE)
	Oscillation stop detection function		XIN clock oscillation stop detection function
	Voltage detection circuit		On-chip
	Power-on reset circuit		On-chip
Electrical Characteristics	Supply voltage		VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz)
	Current consumption		Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage		VCC = 2.7 to 5.5 V
	Programming and erasure endurance		100 times
Operating Ambient Temperature			-20 to 85°C (N version)
			-40 to 85°C (D version)(2)
			-20 to 105°C (Y version)(3)
Package			52-pin molded-plastic LQFP
			64-pin molded-plastic FLGA

NOTES:
1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

Table 1.2 Functions and Specifications for R8C/25 Group

Item			Specification
CPU	Number of fundamental instructions		89 instructions
	Minimum instruction execution time		50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)
	Operating mode		Single-chip
	Address space		1 Mbyte
	Memory capacity		Refer to **Table 1.4 Product Information for R8C/25 Group**
Peripheral Functions	Ports		I/O ports: 41 pins, Input port: 3 pins
	LED drive ports		I/O ports: 8 pins
	Timers		Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits × 2 channels (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function
	Serial interface		2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface		1 channel I2C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module		Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter		10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer		15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupts		Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels
	Clock	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz)
			Real-time clock (timer RE)
	Oscillation stop detection function		XIN clock oscillation stop detection function
	Voltage detection circuit		On-chip
	Power-on reset circuit		On-chip
Electrical Characteristics	Supply voltage		VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz)
	Current consumption		Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash memory	Programming and erasure voltage		VCC = 2.7 to 5.5 V
	Programming and erasure endurance		1,0000 times (data flash)
			1,000 times (program ROM)
Operating Ambient Temperature			-20 to 85°C (N version)
			-40 to 85°C (D version)(2)
			-20 to 105°C (Y version)(3)
Package			52-pin molded-plastic LQFP
			64-pin molded-plastic FLGA

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

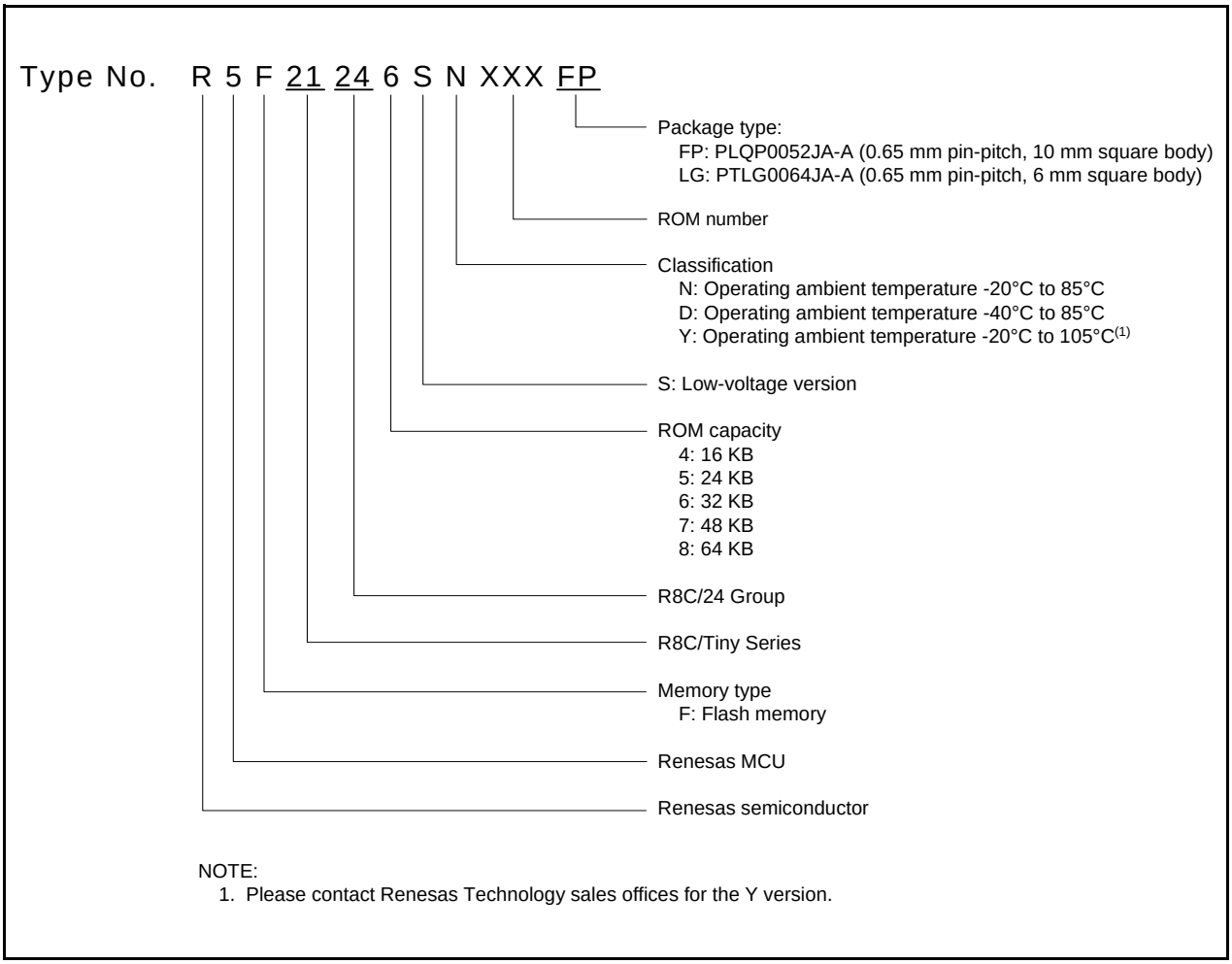


Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group

Table 1.4 Product Information for R8C/25 Group Current of Feb. 2008

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21254SNFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21255SNFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Blank product
R5F21255SDFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Factory programming product(1)
R5F21255SNXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNXXXLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Factory programming product(1)
R5F21255SDXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	

NOTE:
1. The user ROM is programmed before shipment.

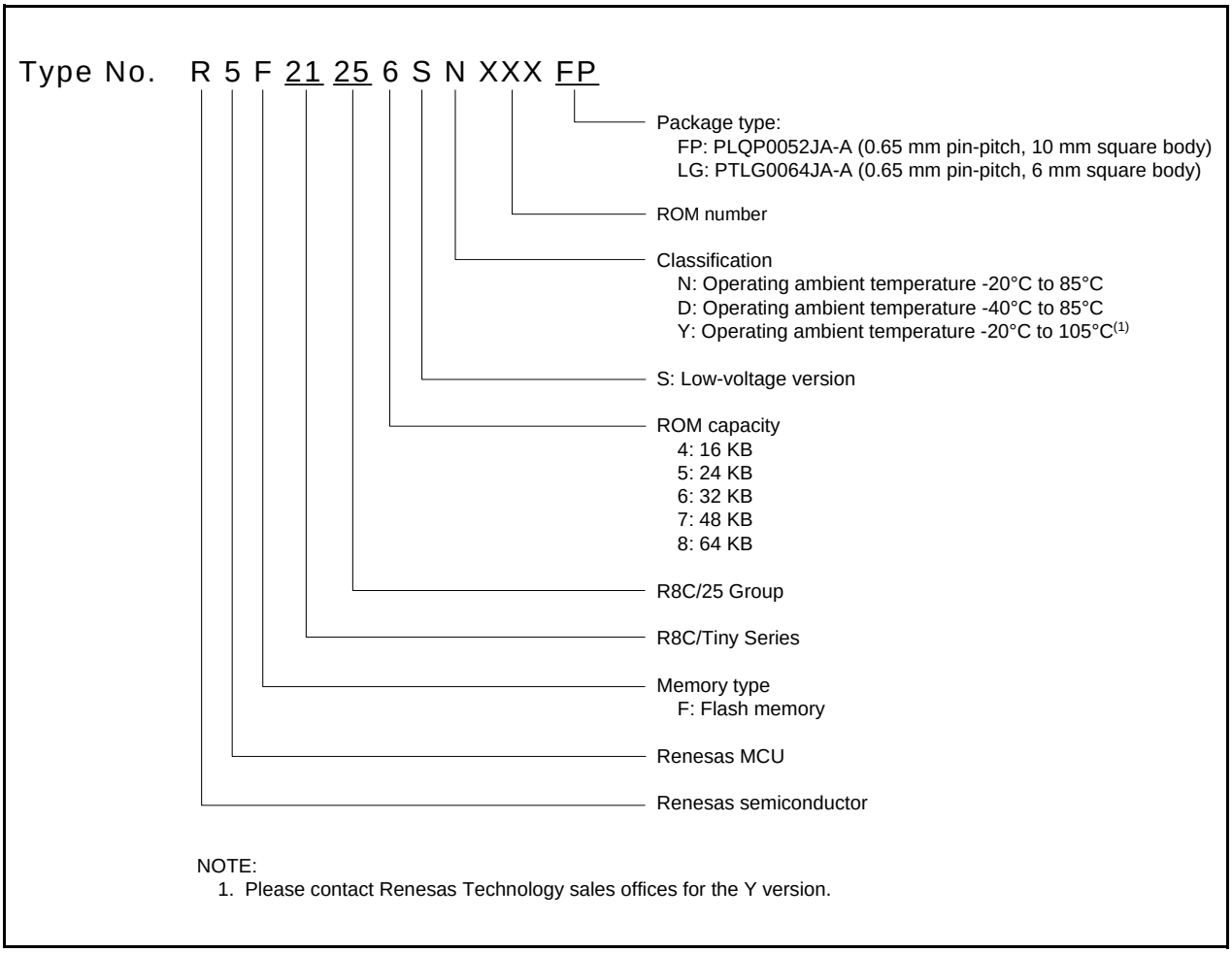


Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group

Pin assignments (top perspective view)

	A	B	C	D	E	F	G	H	
8	3 P3_3/SSI	50 P0_1/AN6	48 P0_3/AN4	46 P6_2	45 P6_0/TREO	NC	36 P6_4	NC	8
7	4 P3_4/SDA/$\overline{\text{SCS}}$	51 P0_0/AN7	49 P0_2/AN5	NC	44 P4_2/VREF	34 P3_0/TRAO	35 P6_5/CLK1	NC	7
6	NC	5 MODE	52 P3_7/SSO	47 P6_1	43 P0_4/AN3	42 P0_5/AN2	NC	33 P3_1/TRBO	6
5	7 P4_4/XCOUT	NC	6 P4_3/XCIN	2 P3_5/SCL/SSCK	37 P6_3	NC	41 P0_6/AN1	38 P0_7/AN0	5
4	13 P2_7/TRDIOD1	12 VCC/AVCC	NC	9 XOUT/P4_7(1)	8 $\overline{\text{RESET}}$	32 P1_0/$\overline{\text{KI0}}$/AN8	31 P1_1/$\overline{\text{KI1}}$/AN9	NC	4
3	NC	10 VSS/AVSS	16 P2_4/TRDIOA1	19 P2_1/TRDIOB0	23 P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)(2)	NC	NC	30 P1_2/$\overline{\text{KI2}}$/AN10	3
2	NC	11 XIN/P4_6	17 P2_3/TRDIOD0	20 P2_0/TRDIOA0/TRDCLK	NC	24 P1_4/TXD0	28 P6_6/$\overline{\text{INT2}}$/TXD1	NC	2
1	14 P2_6/TRDIOC1	15 P2_5/TRDIOB1	18 P2_2/TRDIOC0	21 P1_7/TRAIO/$\overline{\text{INT1}}$	22 P1_6/CLK0	25 P1_3/$\overline{\text{KI3}}$/AN11	27 P4_5/$\overline{\text{INT0}}$	29 P6_7/$\overline{\text{INT3}}$/RXD1	1
	A	B	C	D	E	F	G	H	

Package: PTLG0064JA-A(64F0G)
0.65 mm pin pitch, 6 mm square body

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. In the figure, the numbers in circles are the pin numbers of the 52-pin LQFP package (PLQP0052JA-A).
   NC: Non-Connection

R5F21244S
NLG
JAPAN

Pin assignments (top view)

Figure 1.5 PTLG0064JA-A Package Pin Assignments

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

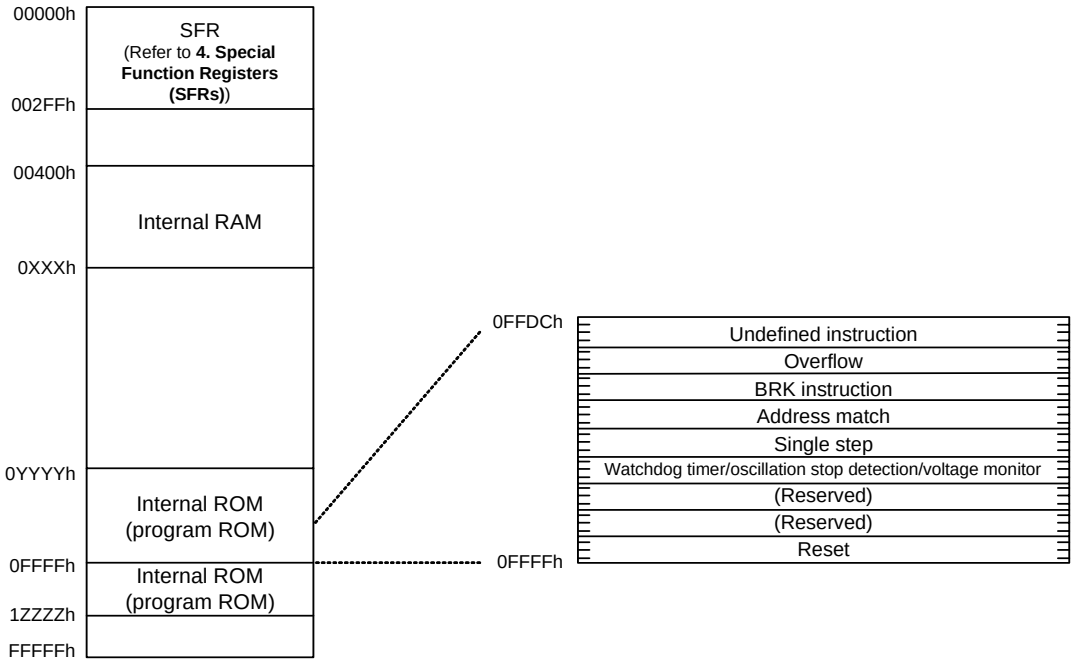
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/24 Group

Figure 3.1 is a Memory Map of R8C/24 Group. The R8C/24 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM area is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address 1ZZZZh	Size	Address 0XXXXh
R5F21244SNFP, R5F21244SNXXXFP, R5F21244SDFP, R5F21244SDXXXFP, R5F21244SNLG, R5F21244SNXXXLG	16 Kbytes	0C000h	–	1 Kbyte	007FFh
R5F21245SNFP, R5F21245SNXXXFP, R5F21245SDFP, R5F21245SDXXXFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21246SNFP, R5F21246SNXXXFP, R5F21246SDFP, R5F21246SDXXXFP, R5F21246SNLG, R5F21246SNXXXLG	32 Kbytes	08000h	–	2 Kbytes	00BFFh
R5F21247SNFP, R5F21247SNXXXFP, R5F21247SDFP, R5F21247SDXXXFP	48 Kbytes	04000h	–	2.5 Kbytes	00DFFh
R5F21248SNFP, R5F21248SNXXXFP, R5F21248SDFP, R5F21248SDXXXFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh

Figure 3.1 Memory Map of R8C/24 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b[6]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 00100000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[5]	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register[2]	VW0C	0000X000b[3] 0100X001b[4]
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset or the LVD0ON bit in the OFS register is set to 0, and hardware reset.
5. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.2 SFR Information (2)[1]

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC Interrupt Control Register[2]	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

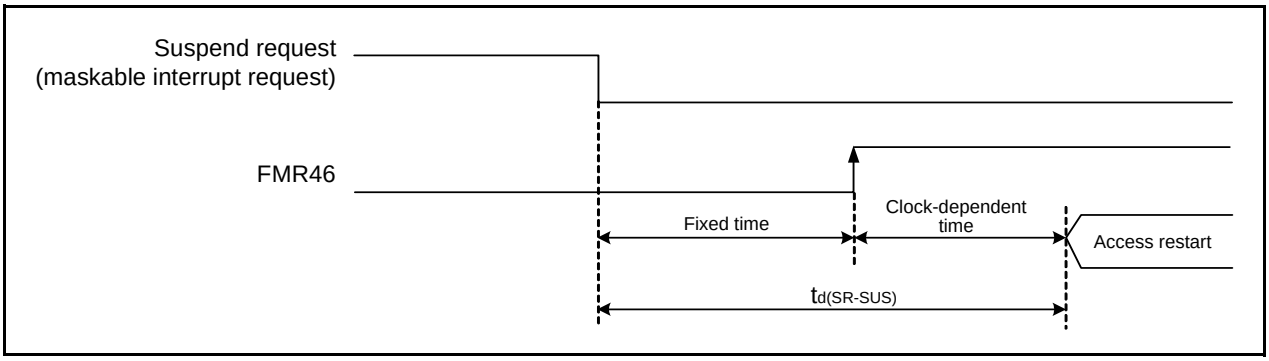


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level		2.2	2.3	2.4	V
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	0.9	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	300	µs
Vccmin	MCU operating voltage minimum value		2.2	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level		2.70	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

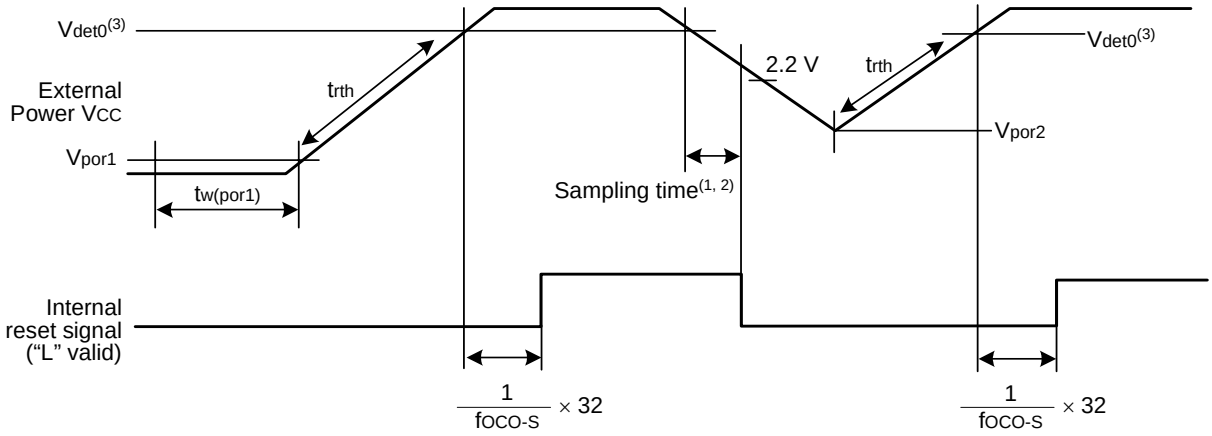
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V_{det0}	V
t_{rth}	External power V_{CC} rise gradient(2)		20	–	–	mV/msec

NOTES:
1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 to 5.25 V 0°C ≤ T_{opr} ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	38.8	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C	38.4	40	40.8	MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 2.7 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38	40	42	MHz
		V_{CC} = 2.7 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	37.6	40	42.4	MHz
		V_{CC} = 2.2 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(3)	35.2	40	44.8	MHz
		V_{CC} = 2.2 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(3)	34	40	46	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4)	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864		MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	-3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

NOTES:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Standard values when the FRA1 register value after reset is assumed.
3. Standard values when the corrected value of the FRA6 register has been written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

NOTES:
1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.18 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

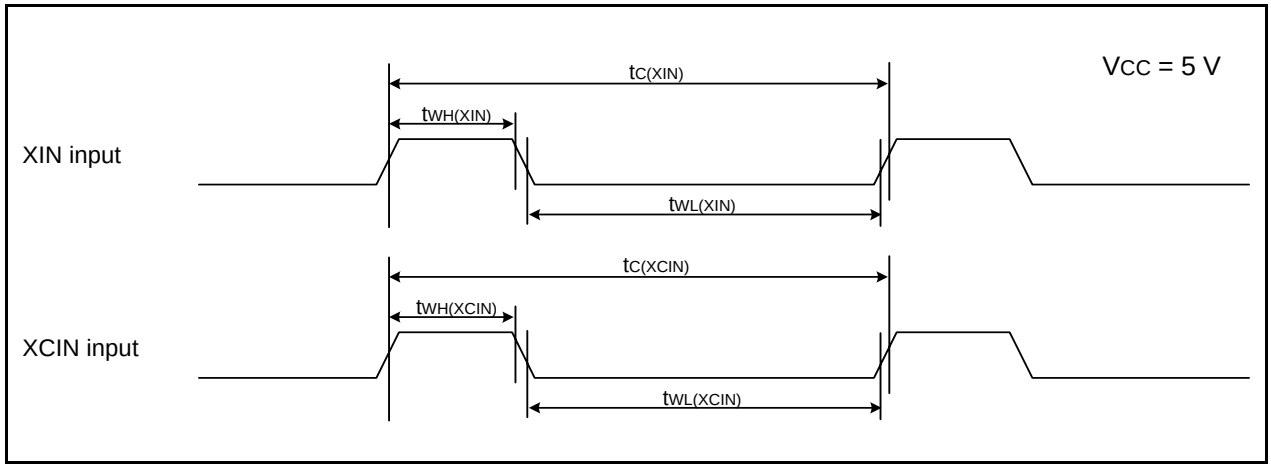


Figure 5.8 XIN Input and XCIN Input Timing Diagram when Vcc = 5 V

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

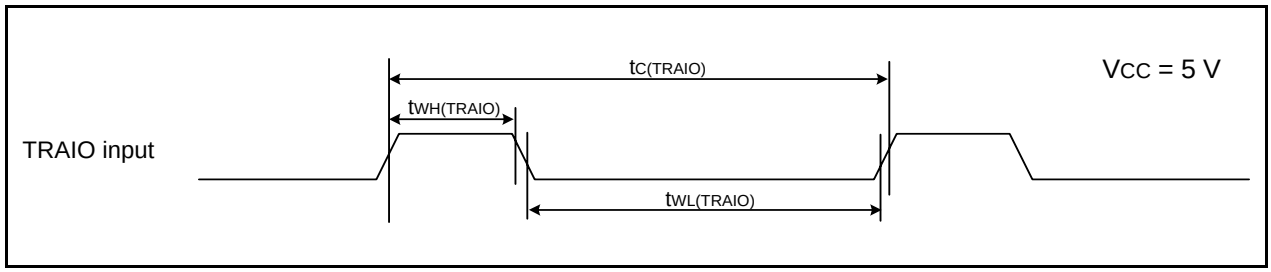


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 5 V

Timing requirements
(Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V at Topr = 25°C) [V_{CC} = 2.2 V]

Table 5.30 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

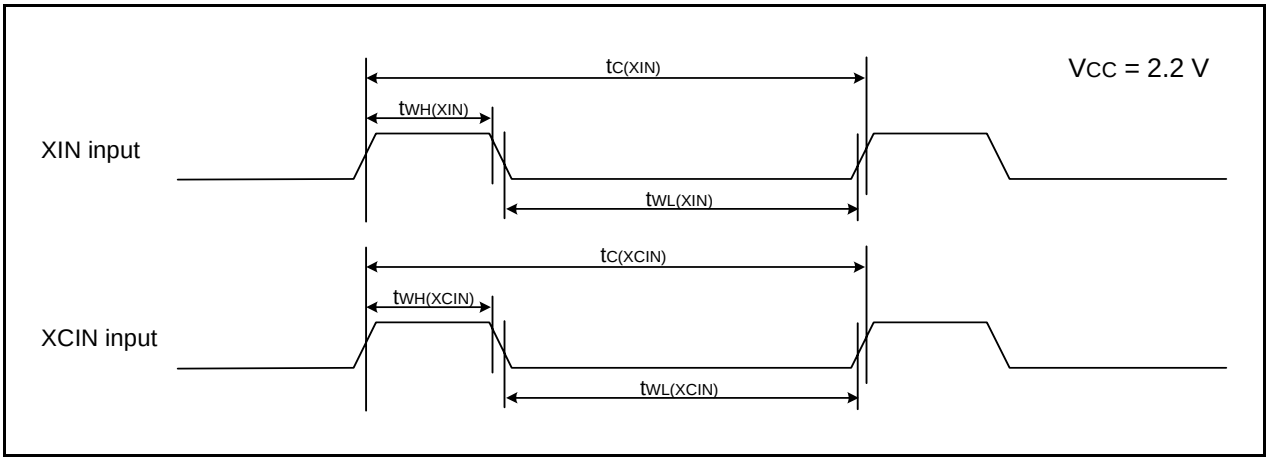


Figure 5.16 XIN Input and XCIN Input Timing Diagram when V_{CC} = 2.2 V

Table 5.31 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

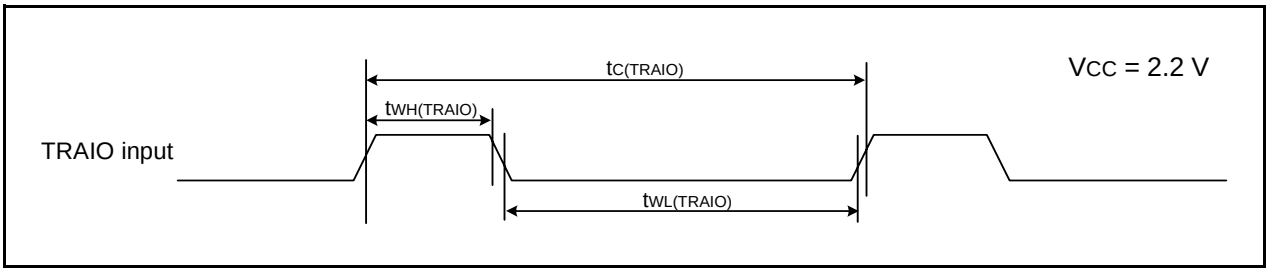


Figure 5.17 TRAIO Input Timing Diagram when V_{CC} = 2.2 V

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Sep 17, 2004	-	First Edition issued
0.02	Dec 10, 2004	All pages	Part Number revised. R8C/26 → R8C/24, R8C/27 → R8C/25
		2, 3	Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance - Serial Interface: I^2C Bus Interface and Chip-select clock synchronous (SSU) added. - LIN Module added. - Interrupt: Internal factors revised; 10 → 11 - Note on Operating Ambient Temperature added.
		4	Figure 1.1 Block Diagram - LIN Module added. - Chip-select clock synchronous (SSU) is added to I^2C Bus Interface.
		5, 6	Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group Date and Development state revised.
		7	Figure 1.4 Pin Assignment P3_5/SCL → P3_5/SCL/SSCK, P3_3 → P3_3/SSI, P3_4/SDA → P3_4/SDA/SCS, P3_7 → P3_7/SSO, VSS/AVSS → VSS, XIN/P4_6 → P4_6/XIN, VCC/AVSS → VCC 12pin P1_7/TRAIO/INT1 to 22pin P1_0/KI0/AN8 → 20pin P1_7/TRAIO/INT1 to 30pin P1_0/KI0/AN8
		8	Table 1.5 Pin Description - Analog Power Supply Input eliminated. - SSU added.
		9	Table 1.6 Pin Name Information by Pin Number added.
		15	Table 4.1 SFR Information (1) - 0031h: Voltage Detection Register 1 → Voltage Detection A Register 1 - 0032h: Voltage Detection Register 1 → Voltage Detection A Register 2 01000001b → 00100001b (Note 4) - 0036h: "(3), 01000001b (4)" eliminated. - 0038h: Voltage Monitor 0 Control Register (2), VW0C, 00001000b (3), 01000001b (4) added.
		16	Table 4.2 SFR Information (2) - 0048h: Timer RD0 Interrupt Control Register, RD0IC, XXXXX000b added. - 0049h: Timer RD Interrupt Control Register, RDIC → Timer RD1 Interrupt Control Register, RD1IC - 004Fh: IIC Interrupt Control Register, IIC → IIC/SSU Interrupt Control Register, IIC2IC
		19	Table 4.5 SFR Information (3) - 0106h: LIN Control Register, LINCR, 00h added. -0107h: LIN Status Register, LINST, 00h added.

Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	7	Figure 1.4 Pin Assignment • Pin name revised; VSS → VSS/AVSS, VCC → VCC/AVCC, P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$) → P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)(2), P6_6/$\overline{\text{INT2}}$/(TXD1) → P6_6/$\overline{\text{INT2}}$/TXD1, P6_7/$\overline{\text{INT3}}$/(RXD1) → P6_7/$\overline{\text{INT3}}$/RXD1, P6_5 → P6_5/CLK1 • NOTE2 added
		8	Table 1.5 Pin Description • Analog Power Supply Input: line added • $\overline{\text{INT}}$ Interrupt Input: "$\overline{\text{INT0}}$ Timer RD input pins. $\overline{\text{INT1}}$ Timer RA input pins." added • Serial Interface: "CLK1" added • "I2C Bus Interface (IIC)" → "I2C Bus Interface" • "SSU" → "Clock Synchronous Serial I/O with Chip Select"
		9	Table 1.6 Pin Name Information by Pin Number revised • Pin Number 10: "VSS" → "VSS/AVSS" • Pin Number 12: "$\overline{\text{VCC}}$" → "VCC/AVCC" • Pin Number 27: "$\overline{\text{INT0}}$" added • Pin Number 28: "(TXD1)" → "TXD1" • Pin Number 29: "(RXD1)" → "RXD1" • Pin Number 35: "CLK1" added
		15	Tabel 4.1 SFR Information(1) revised: • 0012h: X0h → 00h • 0013h: XXXXXX00b → 00h • 0016h: X0h → 00h • 0036h: Voltage Monitor 1 Control Register(2) → Voltage Monitor 1 Control Register(5) • 0038h: 00001000b(3), 01000001b(4) → 0000X000b(3), 0100X001b(4) • NOTES2, 5: "the voltage monitor 1 reset" added • NOTE3: "voltage monitor 1 reset" → "voltage monitor 0 reset"
		16	Tabel 4.2 SFR Information(2) revised: • 0048h: RD0IC → TRD0IC • 0049h: RD1IC → TRD1IC • 004Ah: REIC → TREIC • 004Fh: SSU/IIC Interrupt Control Register, IIC2AIC → SSU/IIC Interrupt Control Register(2), SSUAIC/IIC2AIC • 0056h: RAIC → TRAIC • 0058h: RBIC → TRBIC • NOTE2 added
		17	Tabel 4.3 SFR Information(3) revised: • 00BCh: 00h → 00h/0000X000b
		18	Tabel 4.4 SFR Information(4) revised: • 00D6h: 00000XXXb → 00h • 00F5h: UART1 Function Select Register, U1SR, XXh added

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