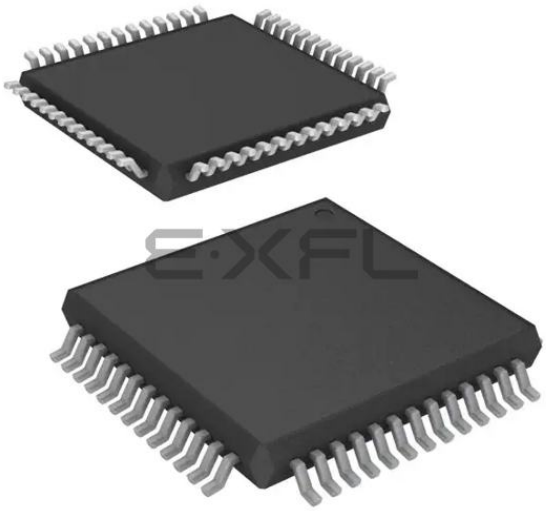


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, Voltage Detect, WDT |
| Number of I/O | 41 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 52-LQFP |
| Supplier Device Package | 52-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21254sdfp-v2 |

**Table 1.4 Product Information for R8C/25 Group Current of Feb. 2008**

| Type No. | ROM Capacity | | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|---|
| | Program ROM | Data flash | | | |
| R5F21254SNFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0052JA-A | N version Blank product |
| R5F21255SNFP | 24 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0052JA-A | |
| R5F21256SNFP | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0052JA-A | |
| R5F21257SNFP | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0052JA-A | |
| R5F21258SNFP | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0052JA-A | |
| R5F21254SNLG | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PTLG0064JA-A | |
| R5F21256SNLG | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PTLG0064JA-A | |
| R5F21254SDFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0052JA-A | D version Blank product |
| R5F21255SDFP | 24 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0052JA-A | |
| R5F21256SDFP | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0052JA-A | |
| R5F21257SDFP | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0052JA-A | |
| R5F21258SDFP | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0052JA-A | |
| R5F21254SNXXXFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0052JA-A | N version Factory programming product(1) |
| R5F21255SNXXXFP | 24 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0052JA-A | |
| R5F21256SNXXXFP | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0052JA-A | |
| R5F21257SNXXXFP | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0052JA-A | |
| R5F21258SNXXXFP | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0052JA-A | |
| R5F21254SNXXXLG | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PTLG0064JA-A | |
| R5F21256SNXXXLG | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PTLG0064JA-A | |
| R5F21254SDXXXFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0052JA-A | D version Factory programming product(1) |
| R5F21255SDXXXFP | 24 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0052JA-A | |
| R5F21256SDXXXFP | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0052JA-A | |
| R5F21257SDXXXFP | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0052JA-A | |
| R5F21258SDXXXFP | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0052JA-A | |

NOTE:
1. The user ROM is programmed before shipment.

Pin assignments (top perspective view)

| | A | B | C | D | E | F | G | H | |
|---|---|---|---|---|---|---|---|---|---|
| 8 | 3<br>P3_3/SSI | 50<br>P0_1/AN6 | 48<br>P0_3/AN4 | 46<br>P6_2 | 45<br>P6_0/TREO | NC | 36<br>P6_4 | NC | 8 |
| 7 | 4<br>P3_4/SDA/$\overline{\text{SCS}}$ | 51<br>P0_0/AN7 | 49<br>P0_2/AN5 | NC | 44<br>P4_2/VREF | 34<br>P3_0/TRAO | 35<br>P6_5/CLK1 | NC | 7 |
| 6 | NC | 5<br>MODE | 52<br>P3_7/SSO | 47<br>P6_1 | 43<br>P0_4/AN3 | 42<br>P0_5/AN2 | NC | 33<br>P3_1/TRBO | 6 |
| 5 | 7<br>P4_4/XCOUT | NC | 6<br>P4_3/XCIN | 2<br>P3_5/SCL/SSCK | 37<br>P6_3 | NC | 41<br>P0_6/AN1 | 38<br>P0_7/AN0 | 5 |
| 4 | 13<br>P2_7/TRDIOD1 | 12<br>VCC/AVCC | NC | 9<br>XOUT/P4_7(1) | 8<br>$\overline{\text{RESET}}$ | 32<br>P1_0/$\overline{\text{KI0}}$/AN8 | 31<br>P1_1/$\overline{\text{KI1}}$/AN9 | NC | 4 |
| 3 | NC | 10<br>VSS/AVSS | 16<br>P2_4/TRDIOA1 | 19<br>P2_1/TRDIOB0 | 23<br>P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)(2) | NC | NC | 30<br>P1_2/$\overline{\text{KI2}}$/AN10 | 3 |
| 2 | NC | 11<br>XIN/P4_6 | 17<br>P2_3/TRDIOD0 | 20<br>P2_0/TRDIOA0/TRDCLK | NC | 24<br>P1_4/TXD0 | 28<br>P6_6/$\overline{\text{INT2}}$/TXD1 | NC | 2 |
| 1 | 14<br>P2_6/TRDIOC1 | 15<br>P2_5/TRDIOB1 | 18<br>P2_2/TRDIOC0 | 21<br>P1_7/TRAIO/$\overline{\text{INT1}}$ | 22<br>P1_6/CLK0 | 25<br>P1_3/$\overline{\text{KI3}}$/AN11 | 27<br>P4_5/$\overline{\text{INT0}}$ | 29<br>P6_7/$\overline{\text{INT3}}$/RXD1 | 1 |
| | A | B | C | D | E | F | G | H | |

Package: PTLG0064JA-A(64F0G)
0.65 mm pin pitch, 6 mm square body

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. In the figure, the numbers in circles are the pin numbers of the 52-pin LQFP package (PLQP0052JA-A).
   NC: Non-Connection

R5F21244S
NLG
JAPAN

Pin assignments (top view)

**Figure 1.5 PTLG0064JA-A Package Pin Assignments**

## 1.6 Pin Functions

Table 1.5 lists Pin Functions.

**Table 1.5 Pin Functions**

| Type | Symbol | I/O Type | Description |
|---|---|---|---|
| Power supply input | VCC, VSS | I | Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | I | Power supply for the A/D converter.<br>Connect a capacitor between AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Input “L” on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| XIN clock input | XIN | I | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open. |
| XIN clock output | XOUT | O | |
| XCIN clock input | XCIN | I | These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins. To use an external clock, input it to the XCIN pin and leave the XCOUT pin open. |
| XCIN clock output | XCOUT | O | |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ | I | $\overline{\text{INT}}$ interrupt input pins.<br>$\overline{\text{INT0}}$ is timer RD input pin. $\overline{\text{INT1}}$ is timer RA input pin. |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins |
| Timer RA | TRAIO | I/O | Timer RA I/O pin |
| | TRAO | O | Timer RA output pin |
| Timer RB | TRBO | O | Timer RB output pin |
| Timer RD | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | I/O | Timer RD I/O ports |
| | TRDCLK | I | External clock input pin |
| Timer RE | TREO | O | Divided clock output pin |
| Serial interface | CLK0, CLK1 | I/O | Transfer clock I/O pin |
| | RXD0, RXD1 | I | Serial data input pins |
| | TXD0, TXD1 | O | Serial data output pins |
| $I^2C$ bus interface | SCL | I/O | Clock I/O pin |
| | SDA | I/O | Data I/O pin |
| Clock synchronous serial I/O with chip select | SSI | I/O | Data I/O pin |
| | $\overline{\text{SCS}}$ | I/O | Chip-select signal I/O pin |
| | SSCK | I/O | Clock I/O pin |
| | SSO | I/O | Data I/O pin |
| Reference voltage input | VREF | I | Reference voltage input pin to A/D converter |
| A/D converter | AN0 to AN11 | I | Analog input pins to A/D converter |
| I/O port | P0_0 to P0_7,<br>P1_0 to P1_7,<br>P2_0 to P2_7,<br>P3_0, P3_1,<br>P3_3 to P3_5, P3_7,<br>P4_3 to P4_5,<br>P6_0 to P6_7 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.<br>Any port set to input can be set to use a pull-up resistor or not by a program.<br>P2_0 to P2_7 also function as LED drive ports. |
| Input port | P4_2, P4_6, P4_7 | I | Input-only ports |

I: Input O: Output I/O: Input and output

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

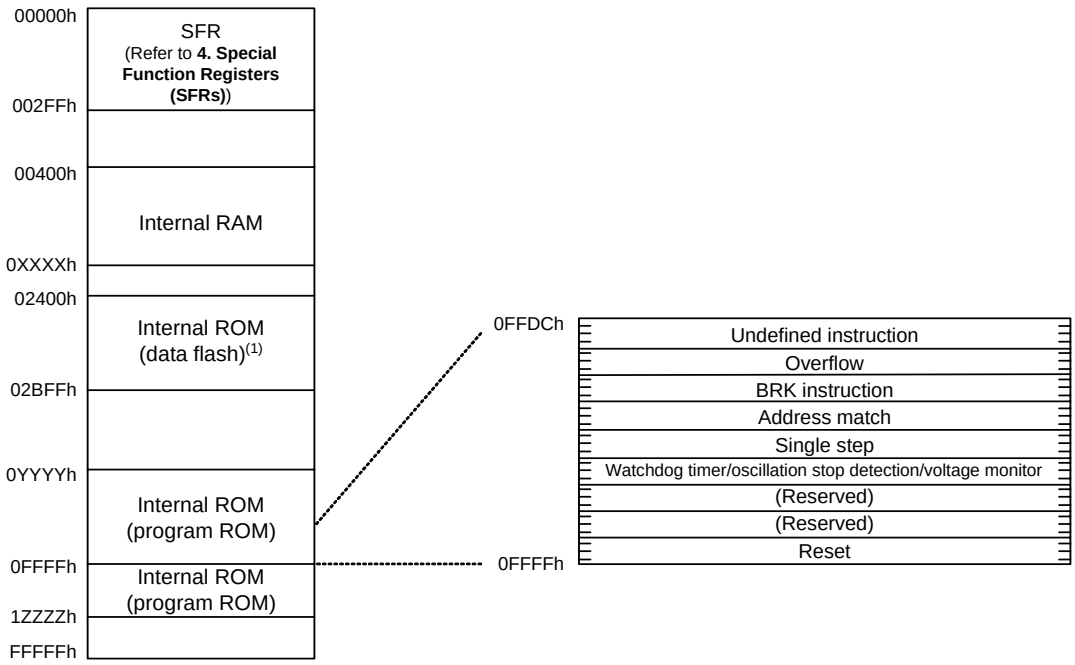
Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

## 3.2 R8C/25 Group

Figure 3.2 is a Memory Map of R8C/25 Group. The R8C/25 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.




NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

| Part Number | Internal ROM | | | Internal RAM | |
|---|---|---|---|---|---|
| | Size | Address 0YYYYh | Address 1ZZZZh | Size | Address 0XXXXh |
| R5F21254SNFP, R5F21254SNXXXFP, R5F21254SDFP, R5F21254SDXXXFP, R5F21254SNLG, R5F21254SNXXXLG | 16 Kbytes | 0C000h | – | 1 Kbyte | 007FFh |
| R5F21255SNFP, R5F21255SNXXXFP, R5F21255SDFP, R5F21255SDXXXFP | 24 Kbytes | 0A000h | – | 2 Kbytes | 00BFFh |
| R5F21256SNFP, R5F21256SNXXXFP, R5F21256SDFP, R5F21256SDXXXFP, R5F21256SNLG, R5F21256SNXXXLG | 32 Kbytes | 08000h | – | 2 Kbytes | 00BFFh |
| R5F21257SNFP, R5F21257SNXXXFP, R5F21257SDFP, R5F21257SDXXXFP | 48 Kbytes | 04000h | – | 2.5 Kbytes | 00DFFh |
| R5F21258SNFP, R5F21258SNXXXFP, R5F21258SDFP, R5F21258SDXXXFP | 64 Kbytes | 04000h | 13FFFh | 3 Kbytes | 00FFFh |

**Figure 3.2 Memory Map of R8C/25 Group**

**Table 4.3 SFR Information (3)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0080h | | | |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | | | |
| 0085h | | | |
| 0086h | | | |
| 0087h | | | |
| 0088h | | | |
| 0089h | | | |
| 008Ah | | | |
| 008Bh | | | |
| 008Ch | | | |
| 008Dh | | | |
| 008Eh | | | |
| 008Fh | | | |
| 0090h | | | |
| 0091h | | | |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | | | |
| 0097h | | | |
| 0098h | | | |
| 0099h | | | |
| 009Ah | | | |
| 009Bh | | | |
| 009Ch | | | |
| 009Dh | | | |
| 009Eh | | | |
| 009Fh | | | |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 00A9h | UART1 Bit Rate Register | U1BRG | XXh |
| 00AAh | UART1 Transmit Buffer Register | U1TB | XXh |
| 00ABh | | | XXh |
| 00ACh | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 00ADh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00000010b |
| 00AEh | UART1 Receive Buffer Register | U1RB | XXh |
| 00AFh | | | XXh |
| 00B0h | | | |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | SS Control Register H / IIC bus Control Register 1[2] | SSCRH / ICCR1 | 00h |
| 00B9h | SS Control Register L / IIC bus Control Register 2[2] | SSCRL / ICCR2 | 01111101b |
| 00BAh | SS Mode Register / IIC bus Mode Register[2] | SSMR / ICMR | 00011000b |
| 00BBh | SS Enable Register / IIC bus Interrupt Enable Register[2] | SSER / ICIER | 00h |
| 00BCh | SS Status Register / IIC bus Status Register[2] | SSSR / ICSR | 00h / 0000X000b |
| 00BDh | SS Mode Register 2 / Slave Address Register[2] | SSMR2 / SAR | 00h |
| 00BEh | SS Transmit Data Register / IIC bus Transmit Data Register[2] | SSTDR / ICDRT | FFh |
| 00BFh | SS Receive Data Register / IIC bus Receive Data Register[2] | SSRDR / ICDRR | FFh |

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

**Table 4.4 SFR Information (4)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 00C0h | A/D Register | AD | XXh |
| 00C1h | | | XXh |
| 00C2h | | | |
| 00C3h | | | |
| 00C4h | | | |
| 00C5h | | | |
| 00C6h | | | |
| 00C7h | | | |
| 00C8h | | | |
| 00C9h | | | |
| 00CAh | | | |
| 00CBh | | | |
| 00CCh | | | |
| 00CDh | | | |
| 00CEh | | | |
| 00CFh | | | |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Control Register 2 | ADCON2 | 00h |
| 00D5h | | | |
| 00D6h | A/D Control Register 0 | ADCON0 | 00h |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | XXh |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | Port P2 Register | P2 | XXh |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | Port P2 Direction Register | PD2 | 00h |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | | | |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | | | |
| 00ECh | Port P6 Register | P6 | XXh |
| 00EDh | | | |
| 00EEh | Port P6 Direction Register | PD6 | 00h |
| 00EFh | | | |
| 00F0h | | | |
| 00F1h | | | |
| 00F2h | | | |
| 00F3h | | | |
| 00F4h | Port P2 Drive Capacity Control Register | P2DRR | 00h |
| 00F5h | UART1 Function Select Register | U1SR | XXh |
| 00F6h | | | |
| 00F7h | | | |
| 00F8h | Port Mode Register | PMR | 00h |
| 00F9h | External Input Enable Register | INTEN | 00h |
| 00FAh | INT Input Filter Select Register | INTF | 00h |
| 00FBh | Key Input Enable Register | KIEN | 00h |
| 00FCh | Pull-Up Control Register 0 | PUR0 | 00h |
| 00FDh | Pull-Up Control Register 1 | PUR1 | XX00XX00b |
| 00FEh | | | |
| 00FFh | | | |

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

**Table 4.6 SFR Information (6)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0140h | Timer RD Control Register 0 | TRDCR0 | 00h |
| 0141h | Timer RD I/O Control Register A0 | TRDIORA0 | 10001000b |
| 0142h | Timer RD I/O Control Register C0 | TRDIORC0 | 10001000b |
| 0143h | Timer RD Status Register 0 | TRDSR0 | 11100000b |
| 0144h | Timer RD Interrupt Enable Register 0 | TRDIER0 | 11100000b |
| 0145h | Timer RD PWM Mode Output Level Control Register 0 | TRDPOCR0 | 11111000b |
| 0146h | Timer RD Counter 0 | TRD0 | 00h |
| 0147h | | | 00h |
| 0148h | Timer RD General Register A0 | TRDGRA0 | FFh |
| 0149h | | | FFh |
| 014Ah | Timer RD General Register B0 | TRDGRB0 | FFh |
| 014Bh | | | FFh |
| 014Ch | Timer RD General Register C0 | TRDGRC0 | FFh |
| 014Dh | | | FFh |
| 014Eh | Timer RD General Register D0 | TRDGRD0 | FFh |
| 014Fh | | | FFh |
| 0150h | Timer RD Control Register 1 | TRDCR1 | 00h |
| 0151h | Timer RD I/O Control Register A1 | TRDIORA1 | 10001000b |
| 0152h | Timer RD I/O Control Register C1 | TRDIORC1 | 10001000b |
| 0153h | Timer RD Status Register 1 | TRDSR1 | 11000000b |
| 0154h | Timer RD Interrupt Enable Register 1 | TRDIER1 | 11100000b |
| 0155h | Timer RD PWM Mode Output Level Control Register 1 | TRDPOCR1 | 11111000b |
| 0156h | Timer RD Counter 1 | TRD1 | 00h |
| 0157h | | | 00h |
| 0158h | Timer RD General Register A1 | TRDGRA1 | FFh |
| 0159h | | | FFh |
| 015Ah | Timer RD General Register B1 | TRDGRB1 | FFh |
| 015Bh | | | FFh |
| 015Ch | Timer RD General Register C1 | TRDGRC1 | FFh |
| 015Dh | | | FFh |
| 015Eh | Timer RD General Register D1 | TRDGRD1 | FFh |
| 015Fh | | | FFh |
| 0160h | | | |
| 0161h | | | |
| 0162h | | | |
| 0163h | | | |
| 0164h | | | |
| 0165h | | | |
| 0166h | | | |
| 0167h | | | |
| 0168h | | | |
| 0169h | | | |
| 016Ah | | | |
| 016Bh | | | |
| 016Ch | | | |
| 016Dh | | | |
| 016Eh | | | |
| 016Fh | | | |
| 0170h | | | |
| 0171h | | | |
| 0172h | | | |
| 0173h | | | |
| 0174h | | | |
| 0175h | | | |
| 0176h | | | |
| 0177h | | | |
| 0178h | | | |
| 0179h | | | |
| 017Ah | | | |
| 017Bh | | | |
| 017Ch | | | |
| 017Dh | | | |
| 017Eh | | | |
| 017Fh | | | |

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

**Table 5.3 A/D Converter Characteristics**

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref}$ = $AV_{CC}$ | – | – | 10 | Bit |
| – | Absolute accuracy | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±3 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±2 | LSB |
| | | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±5 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±2 | LSB |
| | | 10-bit mode | $\phi_{AD}$ = 5 MHz, $V_{ref}$ = $AV_{CC}$ = 2.2 V | – | – | ±5 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 5 MHz, $V_{ref}$ = $AV_{CC}$ = 2.2 V | – | – | ±2 | LSB |
| $R_{ladder}$ | Resistor ladder | | $V_{ref}$ = $AV_{CC}$ | 10 | – | 40 | kΩ |
| $t_{conv}$ | Conversion time | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 3.3 | – | – | µs |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 2.8 | – | – | µs |
| $V_{ref}$ | Reference voltage | | | 2.2 | – | $AV_{CC}$ | V |
| $V_{IA}$ | Analog input voltage(2) | | | 0 | – | $AV_{CC}$ | V |
| – | A/D operating clock frequency | Without sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 0.25 | – | 10 | MHz |
| | | With sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 1 | – | 10 | MHz |
| | | Without sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.2 to 5.5 V | 0.25 | – | 5 | MHz |
| | | With sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.2 to 5.5 V | 1 | – | 5 | MHz |

NOTES:
1. $AV_{CC}$ = 2.2 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

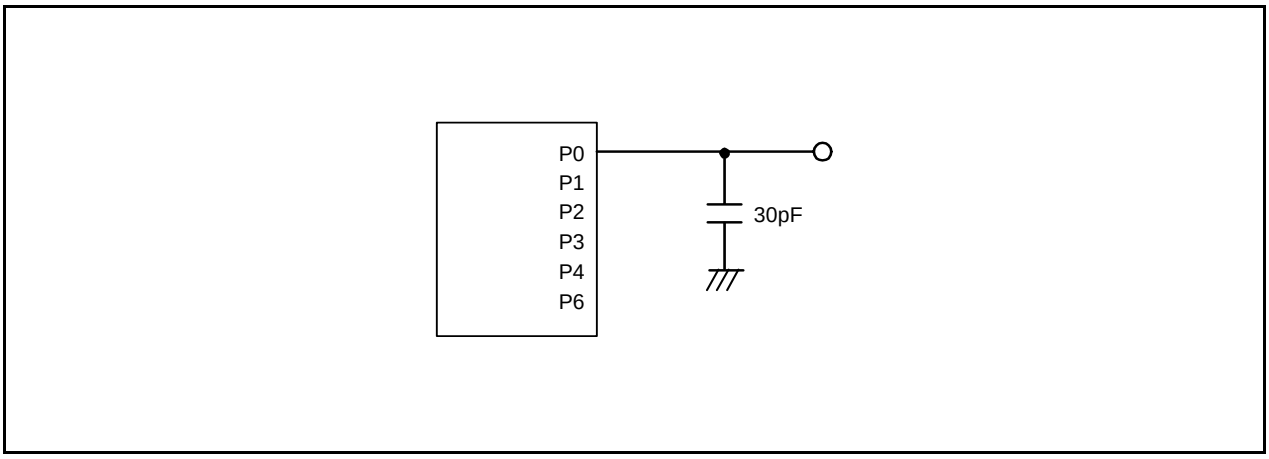



**Figure 5.1 Ports P0 to P4, P6 Timing Measurement Circuit**

**Table 5.4 Flash Memory (Program ROM) Electrical Characteristics**

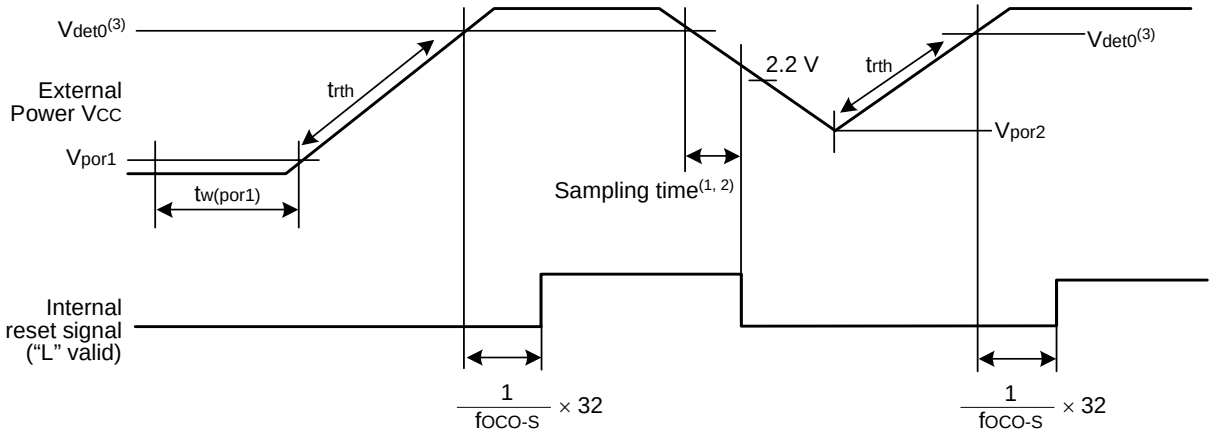
| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance(2) | R8C/24 Group | 100(3) | – | – | times |
| | | R8C/25 Group | 1,000(3) | – | – | times |
| – | Byte program time | | – | 50 | 400 | µs |
| – | Block erase time | | – | 0.4 | 9 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | µs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | µs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time(7) | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{por1}$ | Power-on reset valid voltage(4) | | – | – | 0.1 | V |
| $V_{por2}$ | Power-on reset or voltage monitor 0 reset valid voltage | | 0 | – | $V_{det0}$ | V |
| $t_{rth}$ | External power $V_{CC}$ rise gradient(2) | | 20 | – | – | mV/msec |

NOTES:
1. The measurement condition is $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power $V_{CC}$ rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power $V_{CC}$ must be held below the effective voltage ($V_{por1}$) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if -20°C ≤ $T_{opr}$ ≤ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if -40°C ≤ $T_{opr}$ < -20°C.




NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. $V_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

### Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature • supply voltage dependence | $V_{CC}$ = 4.75 to 5.25 V<br>0°C ≤ $T_{opr}$ ≤ 60°C(2) | 39.2 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 4.5 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C | 38.8 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 4.5 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C | 38.4 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 3.0 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.8 | 40 | 41.2 | MHz |
| | | $V_{CC}$ = 3.0 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.4 | 40 | 41.6 | MHz |
| | | $V_{CC}$ = 2.7 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38 | 40 | 42 | MHz |
| | | $V_{CC}$ = 2.7 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C(2) | 37.6 | 40 | 42.4 | MHz |
| | | $V_{CC}$ = 2.2 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C(3) | 35.2 | 40 | 44.8 | MHz |
| | | $V_{CC}$ = 2.2 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C(3) | 34 | 40 | 46 | MHz |
| | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4) | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 36.864 | | MHz |
| | | $V_{CC}$ = 3.0 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C | -3% | – | 3% | % |
| – | Value in FRA1 register after reset | | 08h | – | F7h | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to -1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 400 | – | µA |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Standard values when the FRA1 register value after reset is assumed.
3. Standard values when the corrected value of the FRA6 register has been written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

### Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 15 | – | µA |

NOTE:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

### Table 5.12 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on(2) | | 1 | – | 2000 | µs |
| $t_{d(R-S)}$ | STOP exit time(3) | | – | – | 150 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

**Table 5.16 Electrical Characteristics (2) [Vcc = 5 V]**
**(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 10 | 17 | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 9 | 15 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6 | – | mA |
| | | | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 5 | – | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 4 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2.5 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 10 | 15 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 4 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5.5 | 10 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2.5 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 130 | 300 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>FMR47 = 1 | – | 130 | 300 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>Program operation on RAM<br>Flash memory off, FMSTP = 1 | – | 30 | – | µA |

**Table 5.20 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 100 | – | ns |
| $t_{W(CKL)}$ | CLKi input “L” width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

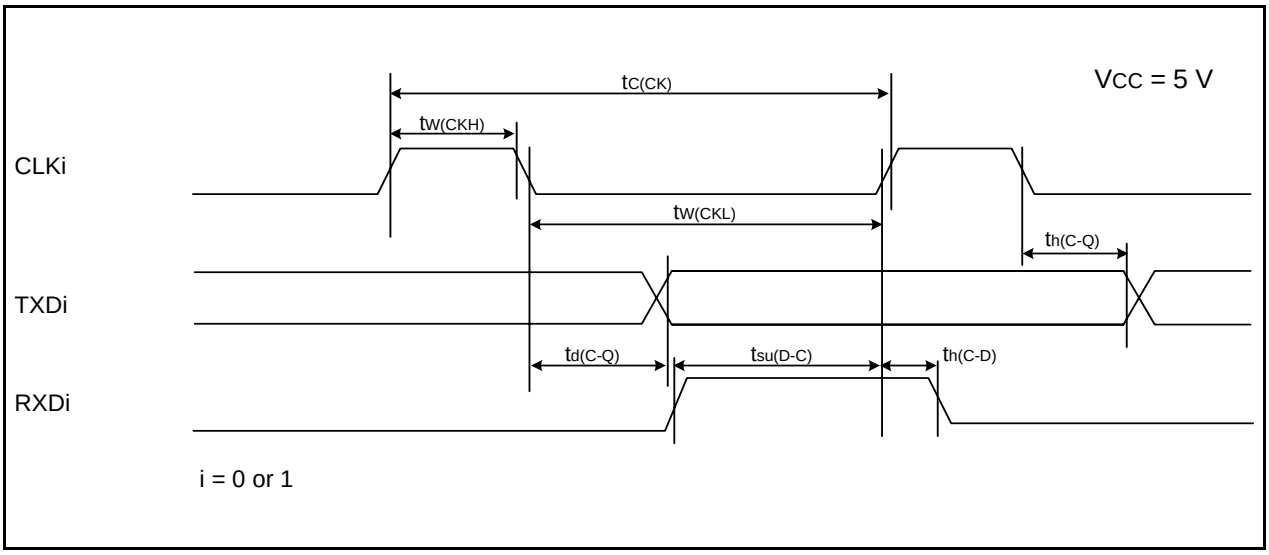



**Figure 5.10 Serial Interface Timing Diagram when VCC = 5 V**

**Table 5.21 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INT0}$ input “H” width | 250(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INT0}$ input “L” width | 250(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

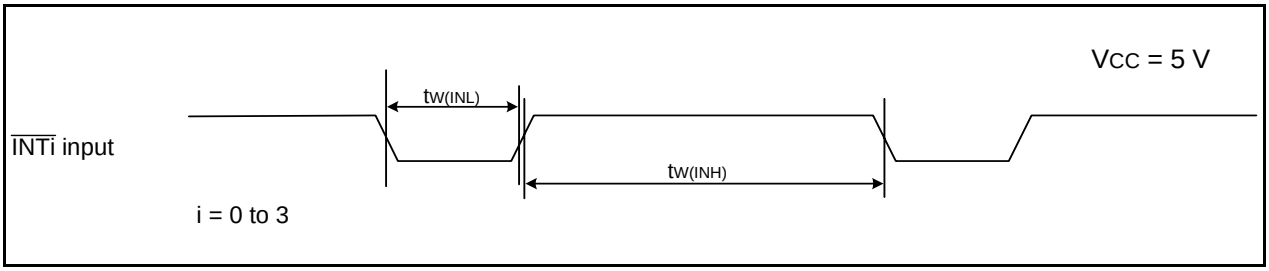



**Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V**

**Table 5.23 Electrical Characteristics (4) [Vcc = 3 V]**
**(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5 | 9 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 130 | 300 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>FMR47 = 1 | – | 130 | 300 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>Program operation on RAM<br>Flash memory off, FMSTP = 1 | – | 30 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 25 | 70 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 23 | 55 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (high drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 3.8 | – | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (low drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 2.0 | – | µA |
| | | Increase during A/D converter operation | Without sample & hold | – | 0.9 | – | mA |
| | | | With sample & hold | – | 0.5 | – | mA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | µA |

**Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V]**
**(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.5 | – | mA |
| | | | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.5 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 100 | 230 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>FMR47 = 1 | – | 100 | 230 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>Program operation on RAM<br>Flash memory off, FMSTP = 1 | – | 25 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 22 | 60 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 20 | 55 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (high drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 3.0 | – | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (low drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 1.8 | – | µA |
| | | Increase during A/D converter operation | Without sample & hold | – | 0.4 | – | mA |
| | | | With sample & hold | – | 0.3 | – | mA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | µA |

**Table 5.32 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 800 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 400 | – | ns |
| $t_{W(CKL)}$ | CLKi input “L” width | 400 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 200 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 150 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

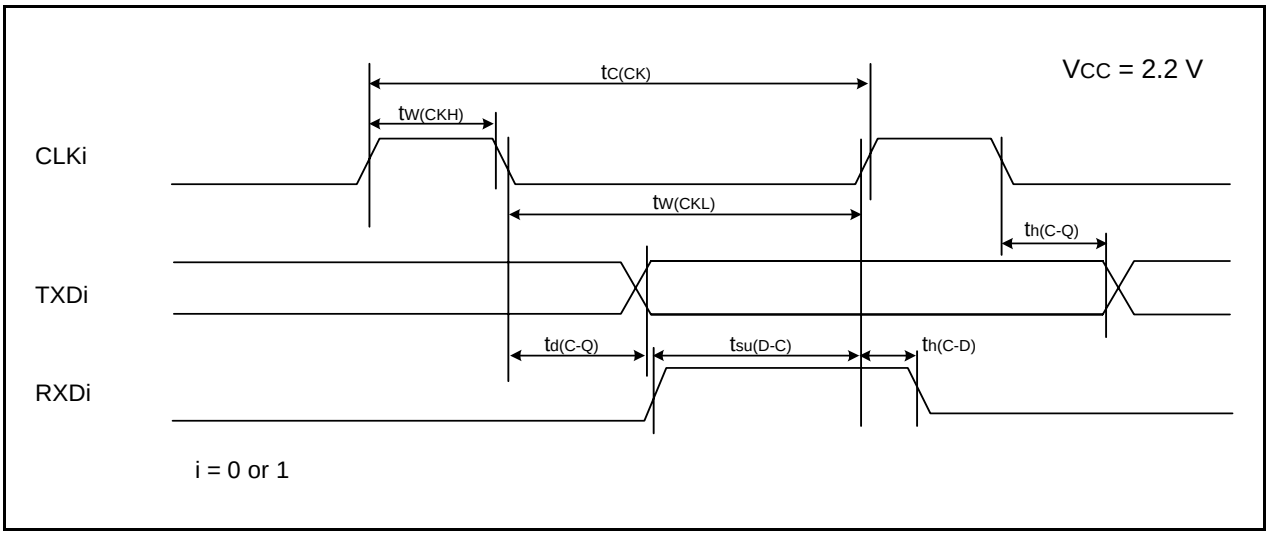



**Figure 5.18 Serial Interface Timing Diagram when VCC = 2.2 V**

**Table 5.33 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INT0}$ input “H” width | 1000(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INT0}$ input “L” width | 1000(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

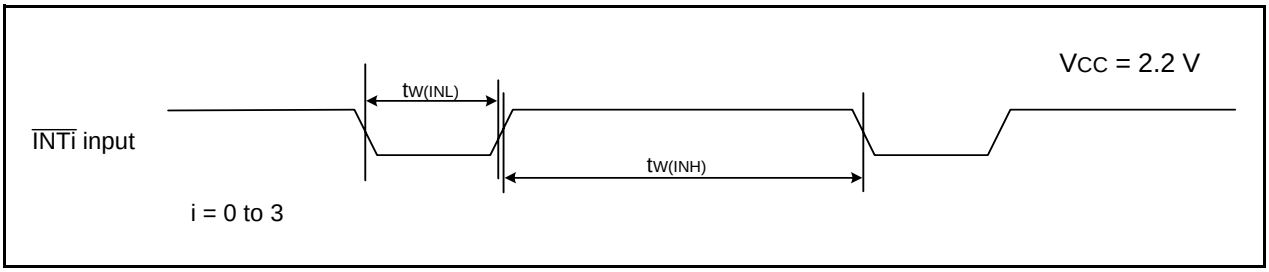



**Figure 5.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 2.2 V**

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.30 | Sep 01, 2005 | 7 | Figure 1.4 Pin Assignment<br>• Pin name revised;<br>VSS → VSS/AVSS,<br>VCC → VCC/AVCC,<br>P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$) → P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)(2),<br>P6_6/$\overline{\text{INT2}}$/(TXD1) → P6_6/$\overline{\text{INT2}}$/TXD1,<br>P6_7/$\overline{\text{INT3}}$/(RXD1) → P6_7/$\overline{\text{INT3}}$/RXD1,<br>P6_5 → P6_5/CLK1<br>• NOTE2 added |
| | | 8 | Table 1.5 Pin Description<br>• Analog Power Supply Input: line added<br>• $\overline{\text{INT}}$ Interrupt Input: "$\overline{\text{INT0}}$ Timer RD input pins. $\overline{\text{INT1}}$ Timer RA input pins." added<br>• Serial Interface: "CLK1" added<br>• "I2C Bus Interface (IIC)" → "I2C Bus Interface"<br>• "SSU" → "Clock Synchronous Serial I/O with Chip Select" |
| | | 9 | Table 1.6 Pin Name Information by Pin Number revised<br>• Pin Number 10: "VSS" → "VSS/AVSS"<br>• Pin Number 12: "$\overline{\text{VCC}}$" → "VCC/AVCC"<br>• Pin Number 27: "$\overline{\text{INT0}}$" added<br>• Pin Number 28: "(TXD1)" → "TXD1"<br>• Pin Number 29: "(RXD1)" → "RXD1"<br>• Pin Number 35: "CLK1" added |
| | | 15 | Tabel 4.1 SFR Information(1) revised:<br>• 0012h: X0h → 00h<br>• 0013h: XXXXXX00b → 00h<br>• 0016h: X0h → 00h<br>• 0036h: Voltage Monitor 1 Control Register(2) → Voltage Monitor 1 Control Register(5)<br>• 0038h: 00001000b(3), 01000001b(4) → 0000X000b(3), 0100X001b(4)<br>• NOTES2, 5: "the voltage monitor 1 reset" added<br>• NOTE3: "voltage monitor 1 reset" → "voltage monitor 0 reset" |
| | | 16 | Tabel 4.2 SFR Information(2) revised:<br>• 0048h: RD0IC → TRD0IC<br>• 0049h: RD1IC → TRD1IC<br>• 004Ah: REIC → TREIC<br>• 004Fh: SSU/IIC Interrupt Control Register, IIC2AIC → SSU/IIC Interrupt Control Register(2), SSUAIC/IIC2AIC<br>• 0056h: RAIC → TRAIC<br>• 0058h: RBIC → TRBIC<br>• NOTE2 added |
| | | 17 | Tabel 4.3 SFR Information(3) revised:<br>• 00BCh: 00h → 00h/0000X000b |
| | | 18 | Tabel 4.4 SFR Information(4) revised:<br>• 00D6h: 00000XXXb → 00h<br>• 00F5h: UART1 Function Select Register, U1SR, XXh added |

| REVISION HISTORY | R8C/24 Group, R8C/25 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.40 | Jan 24, 2006 | 46 | Package Dimensions;<br>"TBD" → "PLQP0052JA-A (52P6A-A)" added |
| 1.00 | May 31, 2006 | all pages | "Under development" deleted |
| | | 1 | 1. Overview; "data flash ROM" → "data flash" revised |
| | | 3 | Table 1.2 Functions and Specifications for R8C/25 Group revised |
| | | 4 | Figure 1.1 Block Diagram;<br>"System clock generator" → "System clock generation circuit" revised |
| | | 5 to 6 | Table 1.3 Product Information for R8C/24 Group and Table 1.4 Product Information for R8C/25 Group; A part of (D) mark is deleted. |
| | | 9 | Table 1.6 Pin Name Information by Pin Number NOTE1 added |
| | | 15 | Table 4.1 SFR Information(1);<br>001Ch: "00h" → "00h, 10000000b" revised<br>0029h: High-Speed On-Chip Oscillator Control Register 4 FRA4 When shipping added<br>002Bh: High-Speed On-Chip Oscillator Control Register 6 FRA6 When shipping added<br>NOTE6 added |
| | | 19 | Table 4.5 SFR Information(5);<br>0118h: Timer RE Second Data Register / Counter Data Register,<br>0119h: Timer RE Minute Data Register / Compare Data Register<br>register name revised |
| | | 20 | Table 4.6 SFR Information(6);<br>0143h: "11000000b" → "11100000b" revised |
| | | 22 | Table 5.2 Recommended Operating Conditions revised |
| | | 24 | Table 5.4 Flash Memory (Program ROM) Electrical Characteristics revised |
| | | 25 | Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics revised |
| | | 26 | Figure 5.2 Time delay until Suspend title revised |
| | | 27 | Table 5.9 Voltage Monitor 0 Reset Electrical Characteristics → Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics revised<br>Table 5.10 Power-on Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 0 Reset) deleted<br>Figure 5.3 Power-on Reset Circuit Electrical Characteristics revised |
| | | 28 | Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised<br>Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised |
| | | 35 | Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] revised |
| | | 39 | Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] revised |
| | | 43 | Table 5.28 Electrical Characteristics (6) [Vcc = 2.2 V] revised |
| | | 46 | Package Dimensions;<br>"The latest package ... Renesas Technology website." added |

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Colophon .7.2