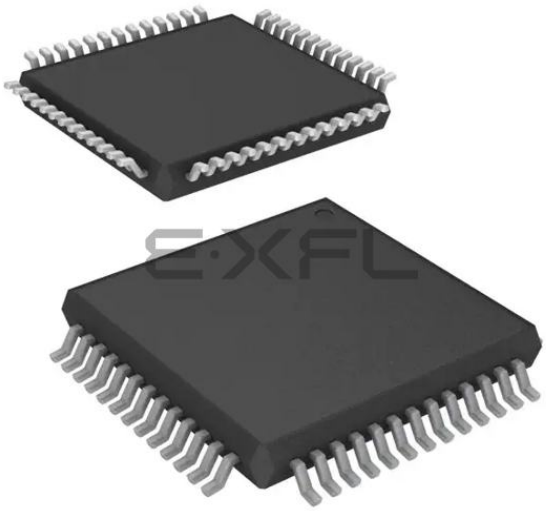


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, Voltage Detect, WDT |
| Number of I/O | 41 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 52-LQFP |
| Supplier Device Package | 52-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21254sdfp-x6 |

## 1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/24 Group and Table 1.2 outlines the Functions and Specifications for R8C/25 Group.

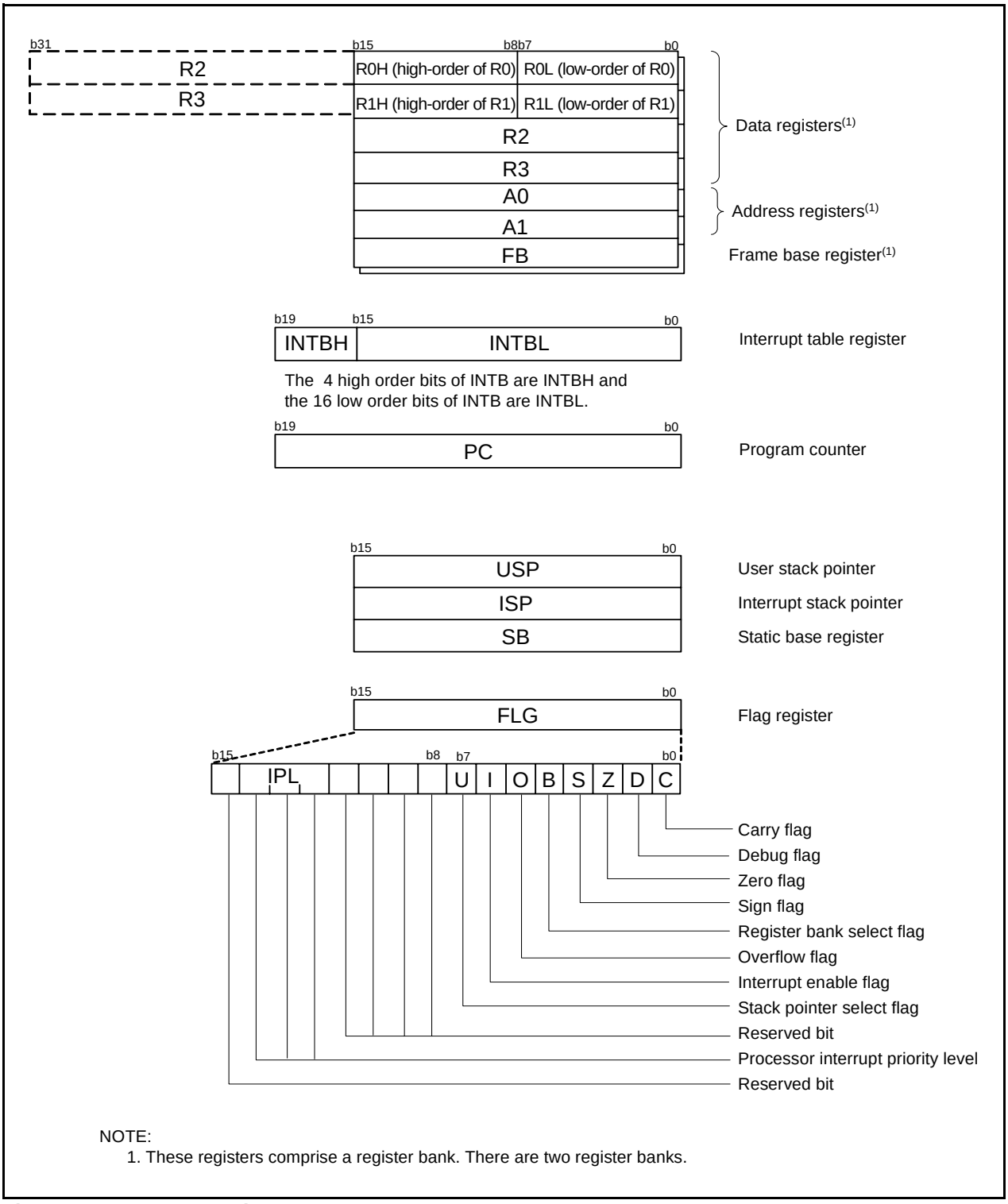
**Table 1.1 Functions and Specifications for R8C/24 Group**

| Item | | | Specification |
|---|---|---|---|
| CPU | Number of fundamental instructions | | 89 instructions |
| | Minimum instruction execution time | | 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) |
| | Operating mode | | Single-chip |
| | Address space | | 1 Mbyte |
| | Memory capacity | | Refer to **Table 1.3 Product Information for R8C/24 Group** |
| Peripheral Functions | Ports | | I/O ports: 41 pins, Input port: 3 pins |
| | LED drive ports | | I/O ports: 8 pins |
| | Timers | | Timer RA: 8 bits × 1 channel<br>Timer RB: 8 bits × 1 channel<br>(Each timer equipped with 8-bit prescaler)<br>Timer RD: 16 bits × 2 channels<br>(Input capture and output compare circuits)<br>Timer RE: With real-time clock and compare match function |
| | Serial interfaces | | 2 channels (UART0, UART1)<br>Clock synchronous serial I/O, UART |
| | Clock synchronous serial interface | | 1 channel<br>I²C bus Interface(1)<br>Clock synchronous serial I/O with chip select |
| | LIN module | | Hardware LIN: 1 channel (timer RA, UART0) |
| | A/D converter | | 10-bit A/D converter: 1 circuit, 12 channels |
| | Watchdog timer | | 15 bits × 1 channel (with prescaler)<br>Reset start selectable |
| | Interrupts | | Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels |
| | Clock | Clock generation circuits | 3 circuits<br>• XIN clock generation circuit (with on-chip feedback resistor)<br>• On-chip oscillator (high speed, low speed)<br>High-speed on-chip oscillator has a frequency adjustment function<br>• XCIN clock generation circuit (32 kHz) |
| | | | Real-time clock (timer RE) |
| | Oscillation stop detection function | | XIN clock oscillation stop detection function |
| | Voltage detection circuit | | On-chip |
| | Power-on reset circuit | | On-chip |
| Electrical Characteristics | Supply voltage | | VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)<br>VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)<br>VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) |
| | Current consumption | | Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz)<br>Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz)<br>Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)<br>Typ. 0.7 μA (VCC = 3.0 V, stop mode) |
| Flash Memory | Programming and erasure voltage | | VCC = 2.7 to 5.5 V |
| | Programming and erasure endurance | | 100 times |
| Operating Ambient Temperature | | | -20 to 85°C (N version) |
| | | | -40 to 85°C (D version)(2) |
| | | | -20 to 105°C (Y version)(3) |
| Package | | | 52-pin molded-plastic LQFP |
| | | | 64-pin molded-plastic FLGA |

NOTES:
1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.




NOTE:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 CPU Registers**

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

**Table 4.4 SFR Information (4)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 00C0h | A/D Register | AD | XXh |
| 00C1h | | | XXh |
| 00C2h | | | |
| 00C3h | | | |
| 00C4h | | | |
| 00C5h | | | |
| 00C6h | | | |
| 00C7h | | | |
| 00C8h | | | |
| 00C9h | | | |
| 00CAh | | | |
| 00CBh | | | |
| 00CCh | | | |
| 00CDh | | | |
| 00CEh | | | |
| 00CFh | | | |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Control Register 2 | ADCON2 | 00h |
| 00D5h | | | |
| 00D6h | A/D Control Register 0 | ADCON0 | 00h |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | XXh |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | Port P2 Register | P2 | XXh |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | Port P2 Direction Register | PD2 | 00h |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | | | |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | | | |
| 00ECh | Port P6 Register | P6 | XXh |
| 00EDh | | | |
| 00EEh | Port P6 Direction Register | PD6 | 00h |
| 00EFh | | | |
| 00F0h | | | |
| 00F1h | | | |
| 00F2h | | | |
| 00F3h | | | |
| 00F4h | Port P2 Drive Capacity Control Register | P2DRR | 00h |
| 00F5h | UART1 Function Select Register | U1SR | XXh |
| 00F6h | | | |
| 00F7h | | | |
| 00F8h | Port Mode Register | PMR | 00h |
| 00F9h | External Input Enable Register | INTEN | 00h |
| 00FAh | INT Input Filter Select Register | INTF | 00h |
| 00FBh | Key Input Enable Register | KIEN | 00h |
| 00FCh | Pull-Up Control Register 0 | PUR0 | 00h |
| 00FDh | Pull-Up Control Register 1 | PUR1 | XX00XX00b |
| 00FEh | | | |
| 00FFh | | | |

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

**Table 5.3 A/D Converter Characteristics**

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref}$ = $AV_{CC}$ | – | – | 10 | Bit |
| – | Absolute accuracy | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±3 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±2 | LSB |
| | | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±5 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±2 | LSB |
| | | 10-bit mode | $\phi_{AD}$ = 5 MHz, $V_{ref}$ = $AV_{CC}$ = 2.2 V | – | – | ±5 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 5 MHz, $V_{ref}$ = $AV_{CC}$ = 2.2 V | – | – | ±2 | LSB |
| $R_{ladder}$ | Resistor ladder | | $V_{ref}$ = $AV_{CC}$ | 10 | – | 40 | kΩ |
| $t_{conv}$ | Conversion time | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 3.3 | – | – | µs |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 2.8 | – | – | µs |
| $V_{ref}$ | Reference voltage | | | 2.2 | – | $AV_{CC}$ | V |
| $V_{IA}$ | Analog input voltage(2) | | | 0 | – | $AV_{CC}$ | V |
| – | A/D operating clock frequency | Without sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 0.25 | – | 10 | MHz |
| | | With sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 1 | – | 10 | MHz |
| | | Without sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.2 to 5.5 V | 0.25 | – | 5 | MHz |
| | | With sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.2 to 5.5 V | 1 | – | 5 | MHz |

NOTES:
1. $AV_{CC}$ = 2.2 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

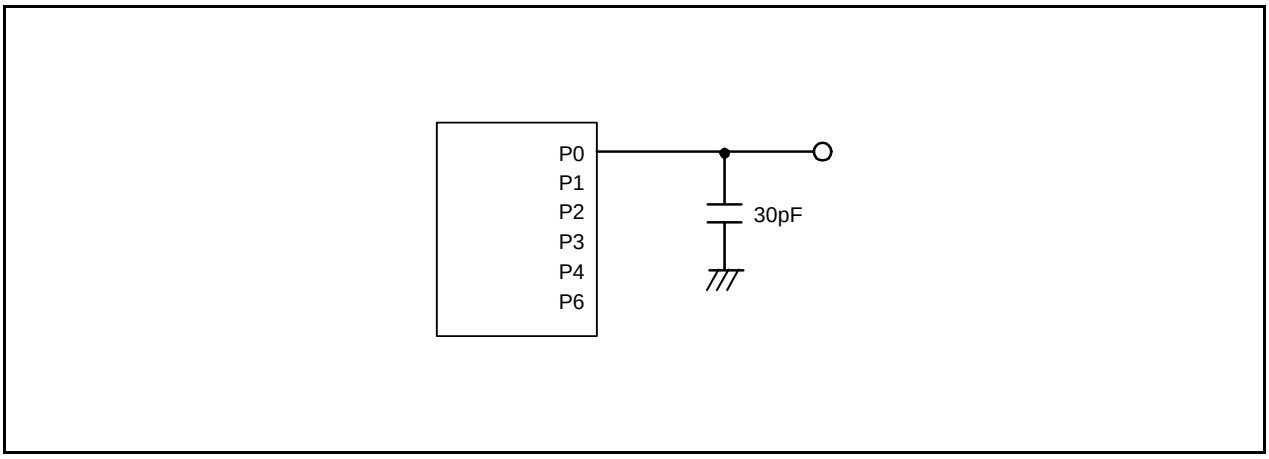



**Figure 5.1 Ports P0 to P4, P6 Timing Measurement Circuit**

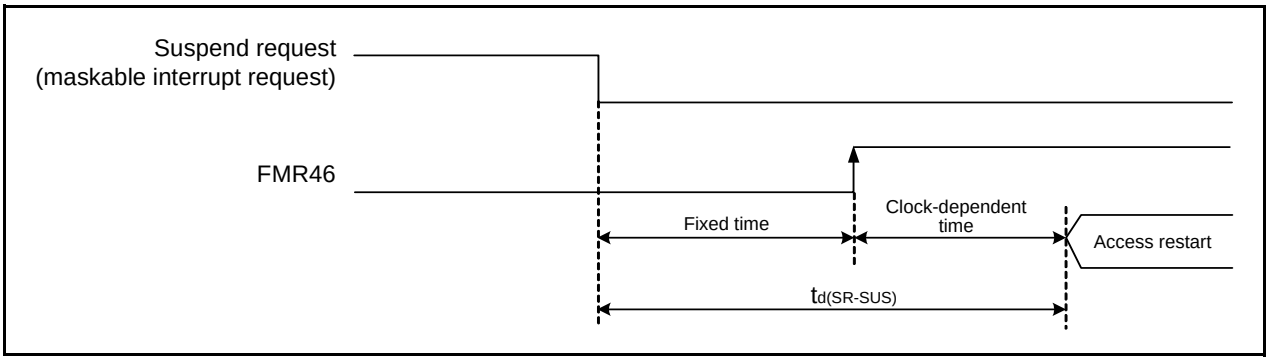



**Figure 5.2 Time delay until Suspend**

### Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det0}$ | Voltage detection level | | 2.2 | 2.3 | 2.4 | V |
| – | Voltage detection circuit self power consumption | VCA25 = 1, $V_{CC}$ = 5.0 V | – | 0.9 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(2) | | – | – | 300 | µs |
| Vccmin | MCU operating voltage minimum value | | 2.2 | – | – | V |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

### Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level | | 2.70 | 2.85 | 3.00 | V |
| – | Voltage monitor 1 interrupt request generation time(2) | | – | 40 | – | µs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes $V_{det1}$.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

### Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

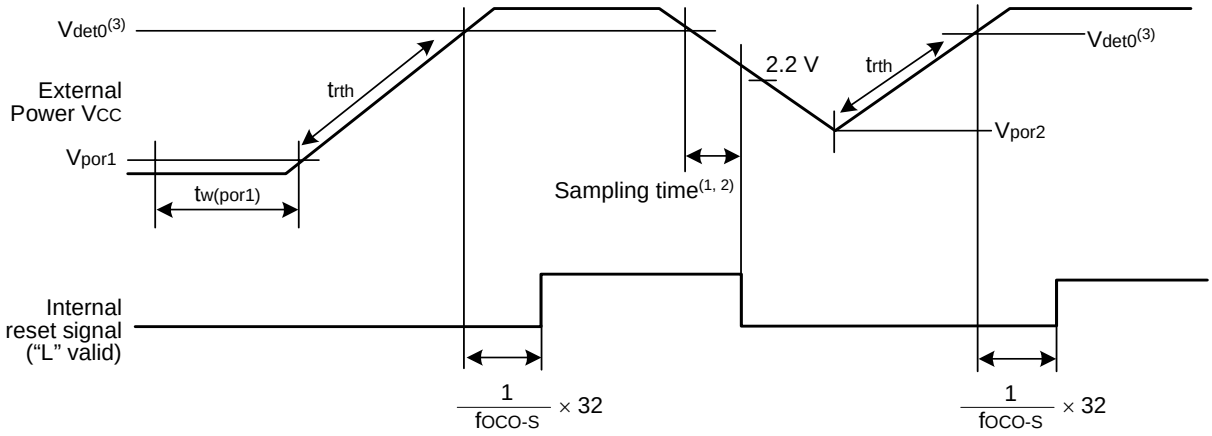
| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level | | 3.3 | 3.6 | 3.9 | V |
| – | Voltage monitor 2 interrupt request generation time(2) | | – | 40 | – | µs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{det2}$.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

**Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{por1}$ | Power-on reset valid voltage(4) | | – | – | 0.1 | V |
| $V_{por2}$ | Power-on reset or voltage monitor 0 reset valid voltage | | 0 | – | $V_{det0}$ | V |
| $t_{rth}$ | External power $V_{CC}$ rise gradient(2) | | 20 | – | – | mV/msec |

NOTES:
1. The measurement condition is $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power $V_{CC}$ rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power $V_{CC}$ must be held below the effective voltage ($V_{por1}$) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if -20°C ≤ $T_{opr}$ ≤ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if -40°C ≤ $T_{opr}$ < -20°C.




NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. $V_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

### Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature • supply voltage dependence | $V_{CC}$ = 4.75 to 5.25 V<br>0°C ≤ $T_{opr}$ ≤ 60°C(2) | 39.2 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 4.5 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C | 38.8 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 4.5 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C | 38.4 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 3.0 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.8 | 40 | 41.2 | MHz |
| | | $V_{CC}$ = 3.0 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.4 | 40 | 41.6 | MHz |
| | | $V_{CC}$ = 2.7 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38 | 40 | 42 | MHz |
| | | $V_{CC}$ = 2.7 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C(2) | 37.6 | 40 | 42.4 | MHz |
| | | $V_{CC}$ = 2.2 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C(3) | 35.2 | 40 | 44.8 | MHz |
| | | $V_{CC}$ = 2.2 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C(3) | 34 | 40 | 46 | MHz |
| | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4) | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 36.864 | | MHz |
| | | $V_{CC}$ = 3.0 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C | -3% | – | 3% | % |
| – | Value in FRA1 register after reset | | 08h | – | F7h | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to -1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 400 | – | µA |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Standard values when the FRA1 register value after reset is assumed.
3. Standard values when the corrected value of the FRA6 register has been written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

### Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 15 | – | µA |

NOTE:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

### Table 5.12 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on(2) | | 1 | – | 2000 | µs |
| $t_{d(R-S)}$ | STOP exit time(3) | | – | – | 150 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

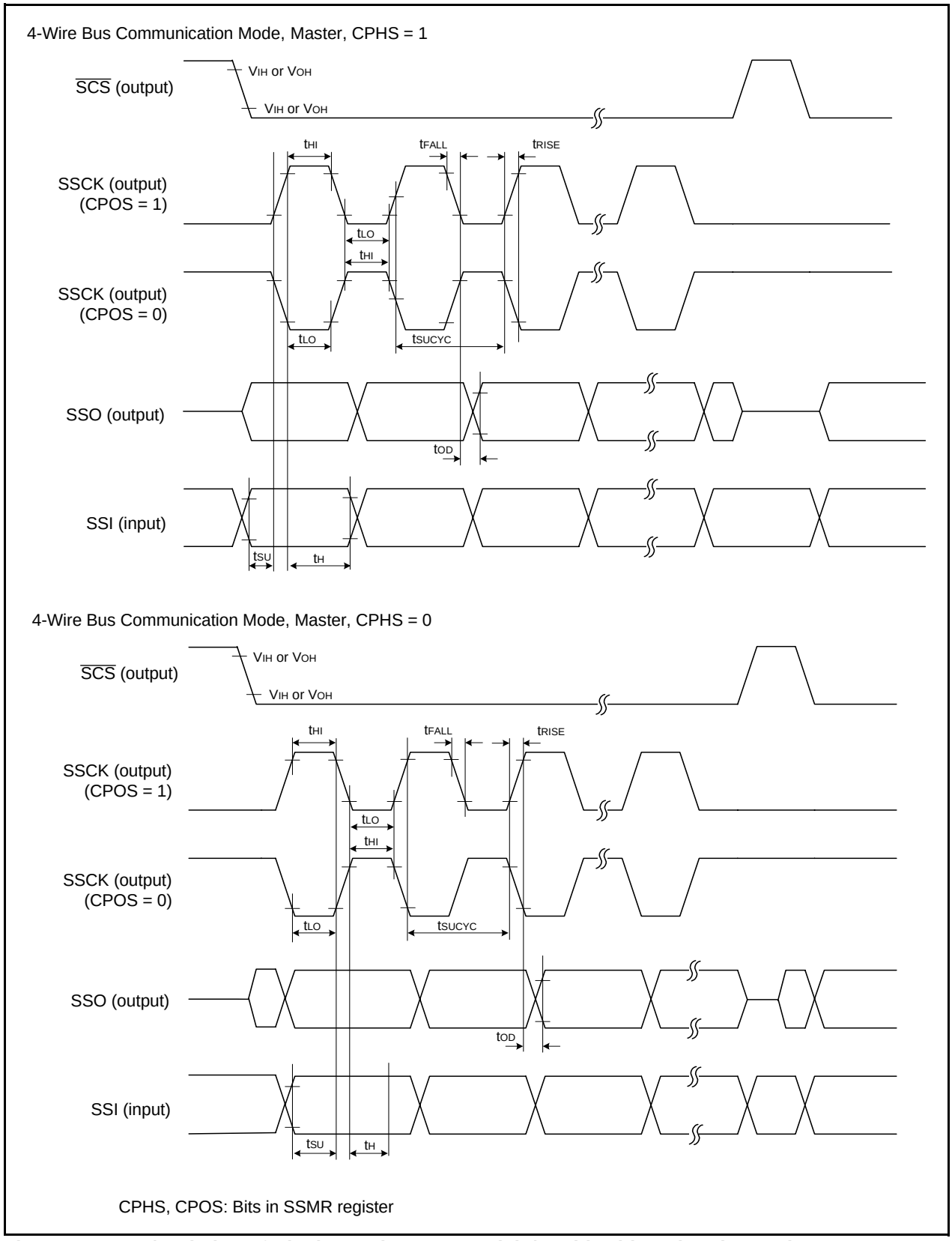



**Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)**

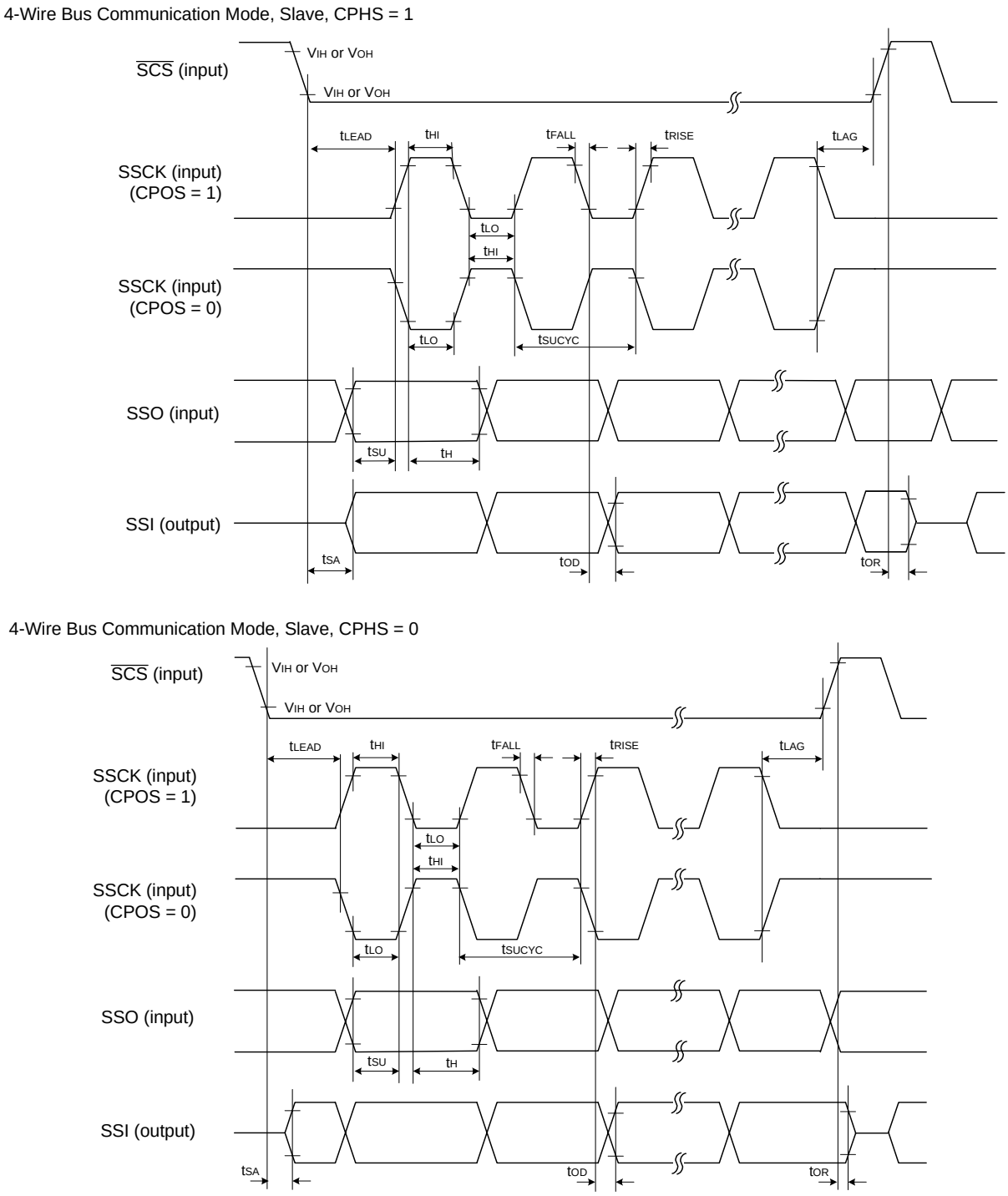



**Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)**

**Table 5.20 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 100 | – | ns |
| $t_{W(CKL)}$ | CLKi input “L” width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

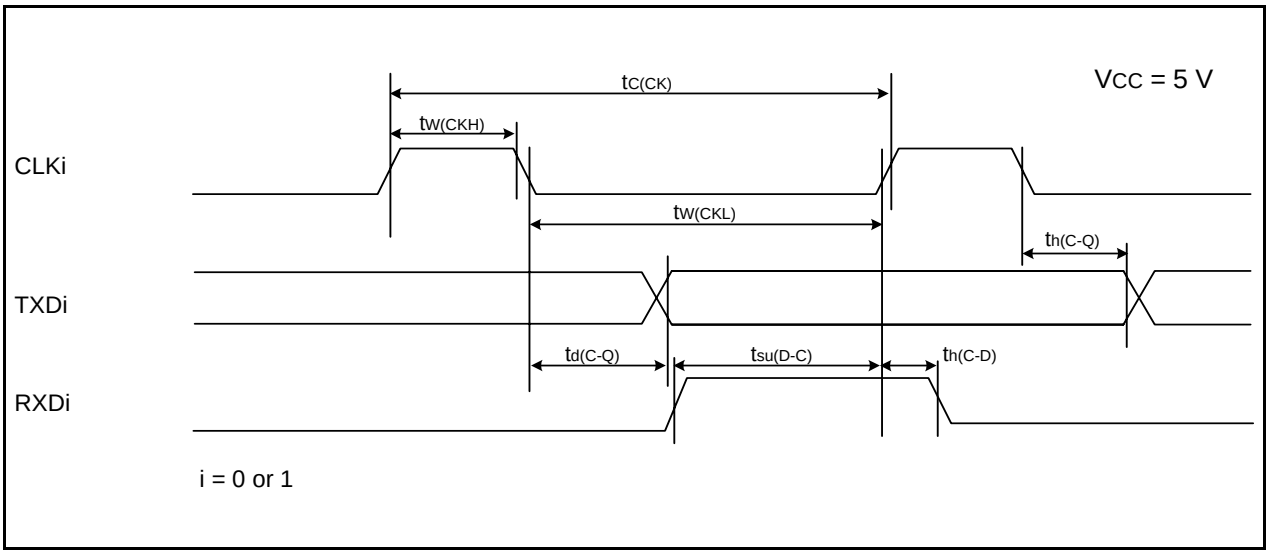



**Figure 5.10 Serial Interface Timing Diagram when VCC = 5 V**

**Table 5.21 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INT0}$ input “H” width | 250(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INT0}$ input “L” width | 250(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

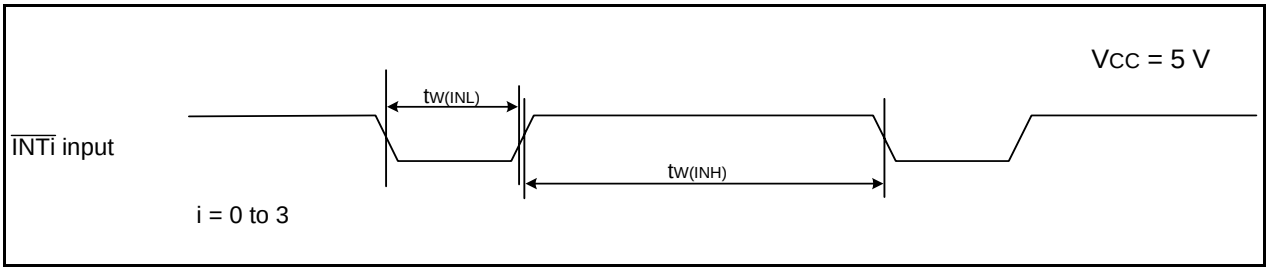



**Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V**

**Table 5.22 Electrical Characteristics (3) [Vcc = 3 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P2_0 to P2_7, XOUT | $I_{OH}$ = -1 mA | | Vcc - 0.5 | – | Vcc | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OH}$ = -5 mA | Vcc - 0.5 | – | Vcc | V |
| | | | Drive capacity LOW | $I_{OH}$ = -1 mA | Vcc - 0.5 | – | Vcc | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = -0.1 mA | Vcc - 0.5 | – | Vcc | V |
| | | | Drive capacity LOW | $I_{OH}$ = -50 µA | Vcc - 0.5 | – | Vcc | V |
| $V_{OL}$ | Output “L” voltage | Except P2_0 to P2_7, XOUT | $I_{OL}$ = 1 mA | | – | – | 0.5 | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OL}$ = 5 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 50 µA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO | | | 0.1 | 0.3 | – | V |
| | | $\overline{RESET}$ | | | 0.1 | 0.4 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 3 V, Vcc = 3V | | – | – | 4.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, Vcc = 3V | | – | – | -4.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, Vcc = 3V | | 66 | 160 | 500 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 3.0 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 18 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:
1. Vcc =2.7 to 3.3 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

**Table 5.23 Electrical Characteristics (4) [Vcc = 3 V]**
**(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5 | 9 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 130 | 300 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>FMR47 = 1 | – | 130 | 300 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>Program operation on RAM<br>Flash memory off, FMSTP = 1 | – | 30 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 25 | 70 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 23 | 55 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (high drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 3.8 | – | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (low drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 2.0 | – | µA |
| | | Increase during A/D converter operation | Without sample & hold | – | 0.9 | – | mA |
| | | | With sample & hold | – | 0.5 | – | mA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | µA |

**Timing requirements**
**(Unless Otherwise Specified: $V_{CC}$ = 3 V, $V_{SS}$ = 0 V at Topr = 25°C) [$V_{CC}$ = 3 V]**

**Table 5.24 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 100 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 40 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 40 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | – | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | – | µs |

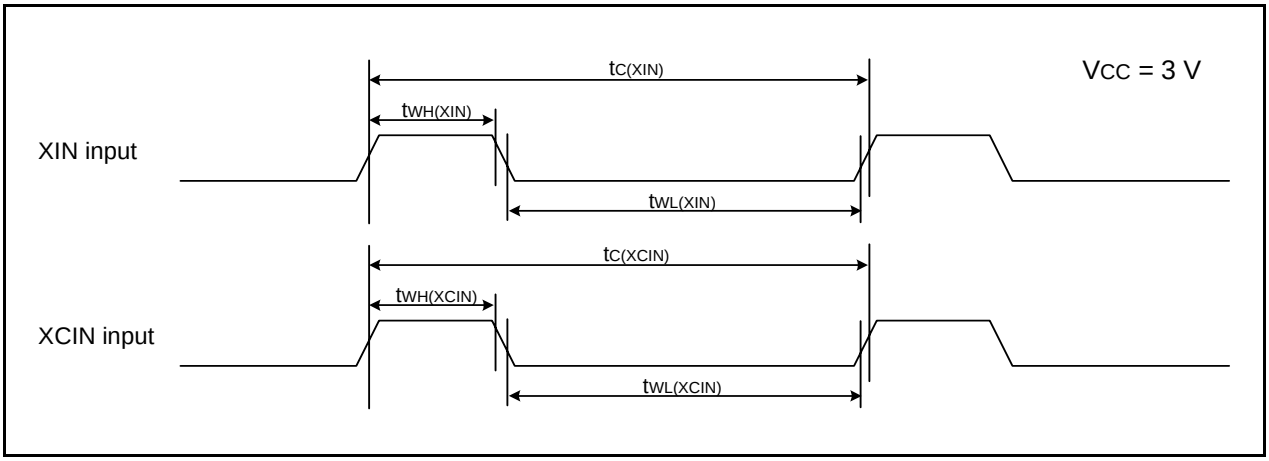



**Figure 5.12 XIN Input and XCIN Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.25 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 300 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 120 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 120 | – | ns |

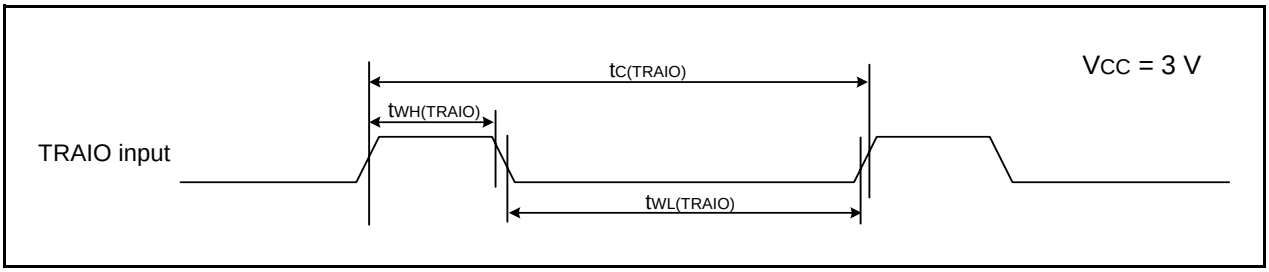



**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.26 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 150 | – | ns |
| $t_{W(CKL)}$ | CLKi Input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

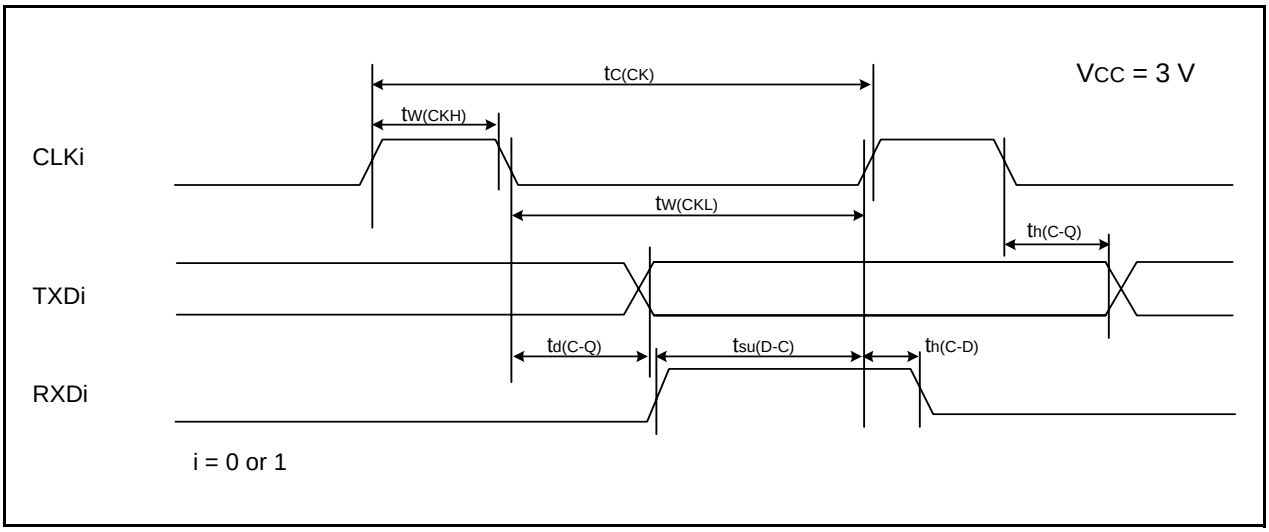



**Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V**

**Table 5.27 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INT0}$ input “H” width | 380(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INT0}$ input “L” width | 380(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

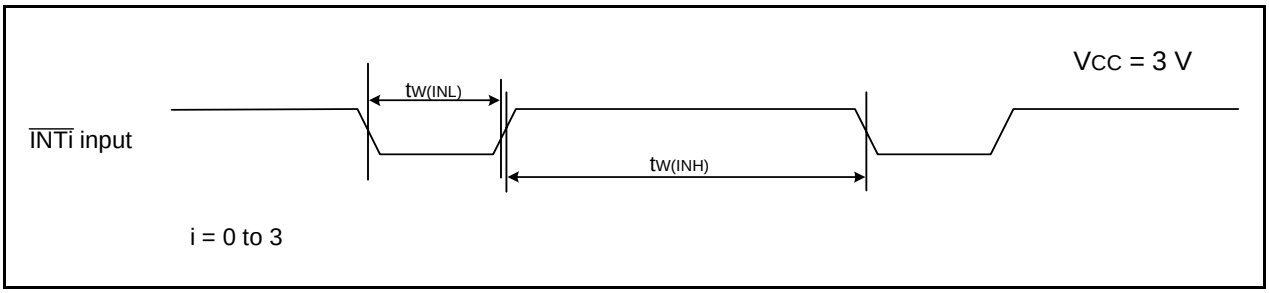



**Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V**

**Table 5.28 Electrical Characteristics (5) [Vcc = 2.2 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P2_0 to P2_7, XOUT | $I_{OH}$ = -1 mA | | Vcc - 0.5 | – | Vcc | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OH}$ = -2 mA | Vcc - 0.5 | – | Vcc | V |
| | | | Drive capacity LOW | $I_{OH}$ = -1 mA | Vcc - 0.5 | – | Vcc | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = -0.1 mA | Vcc - 0.5 | – | Vcc | V |
| | | | Drive capacity LOW | $I_{OH}$ = -50 µA | Vcc - 0.5 | – | Vcc | V |
| $V_{OL}$ | Output “L” voltage | Except P2_0 to P2_7, XOUT | $I_{OL}$ = 1 mA | | – | – | 0.5 | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OL}$ = 2 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 50 µA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO | | | 0.05 | 0.3 | – | V |
| | | $\overline{RESET}$ | | | 0.05 | 0.15 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 2.2 V | | – | – | 4.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V | | – | – | -4.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V | | 100 | 200 | 600 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 5 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 35 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:
1. Vcc = 2.2 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

| REVISION HISTORY | R8C/24 Group, R8C/25 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.01 | Sep 17, 2004 | - | First Edition issued |
| 0.02 | Dec 10, 2004 | All pages | Part Number revised. R8C/26 → R8C/24, R8C/27 → R8C/25 |
| | | 2, 3 | Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance<br>- Serial Interface: $I^2C$ Bus Interface and Chip-select clock synchronous (SSU) added.<br>- LIN Module added.<br>- Interrupt: Internal factors revised; 10 → 11<br>- Note on Operating Ambient Temperature added. |
| | | 4 | Figure 1.1 Block Diagram<br>- LIN Module added.<br>- Chip-select clock synchronous (SSU) is added to $I^2C$ Bus Interface. |
| | | 5, 6 | Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group<br>Date and Development state revised. |
| | | 7 | Figure 1.4 Pin Assignment<br>P3_5/SCL → P3_5/SCL/SSCK, P3_3 → P3_3/SSI,<br>P3_4/SDA → P3_4/SDA/SCS, P3_7 → P3_7/SSO, VSS/AVSS → VSS,<br>XIN/P4_6 → P4_6/XIN, VCC/AVSS → VCC<br>12pin P1_7/TRAIO/INT1 to 22pin P1_0/KI0/AN8<br>→ 20pin P1_7/TRAIO/INT1 to 30pin P1_0/KI0/AN8 |
| | | 8 | Table 1.5 Pin Description<br>- Analog Power Supply Input eliminated.<br>- SSU added. |
| | | 9 | Table 1.6 Pin Name Information by Pin Number added. |
| | | 15 | Table 4.1 SFR Information (1)<br>- 0031h: Voltage Detection Register 1 → Voltage Detection A Register 1<br>- 0032h: Voltage Detection Register 1 → Voltage Detection A Register 2<br>01000001b → 00100001b (Note 4)<br>- 0036h: "(3), 01000001b (4)" eliminated.<br>- 0038h: Voltage Monitor 0 Control Register (2), VW0C,<br>00001000b (3), 01000001b (4) added. |
| | | 16 | Table 4.2 SFR Information (2)<br>- 0048h: Timer RD0 Interrupt Control Register, RD0IC, XXXXX000b added.<br>- 0049h: Timer RD Interrupt Control Register, RDIC<br>→ Timer RD1 Interrupt Control Register, RD1IC<br>- 004Fh: IIC Interrupt Control Register, IIC<br>→ IIC/SSU Interrupt Control Register, IIC2IC |
| | | 19 | Table 4.5 SFR Information (3)<br>- 0106h: LIN Control Register, LINCR, 00h added.<br>-0107h: LIN Status Register, LINST, 00h added. |

| REVISION HISTORY | R8C/24 Group, R8C/25 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.10 | Feb 24, 2005 | 1 to 3<br>5, 6 | Pin type changed: 48-pin(under consideration) → 52-pin. |
| | | 5 to 7 | Package type revised: 48-pin LQFP(under consideration) → PLQP0052JA-A |
| | | 8 | Table 1.5 TCLK added, VREF revised. |
| | | 9 | Table 1.6 revised. |
| | | 13, 14 | Figures 3.1 and 3.2 part number revised. |
| | | 15 | Tabel 4.1 revised:<br>- 000Fh: 000XXXXXb → 00011111b<br>- 0023h: FR0 → FRA0<br>- 0024h: FR1 → FRA1<br>- 0025h: FR2 → FRA2<br>- 0031h: Voltage Detection A Register 1, VC1<br>→ Voltage Detection Register 1, VCA1<br>- 0032h: Voltage Detection A Register 2, VC2<br>→ Voltage Detection Register 2, VCA2 |
| | | 17 | Tabel 4.3 Register name and the value after reset at 00B8h to 00BFh revised; NOTE2 added. |
| | | 19 | Tabel 4.5 revised:<br>- 0107h: LINSR → LINST<br>- 0137h to 013Fh: Register symbol revised |
| | | 20 | Tabel 4.6 revised:<br>- 0140h to 015Fh: Register symbol revised<br>- 0158h, 0159h: Timer RD General Register → Timer RD General Register A1 |
| 0.20 | Mar 8, 2005 | 2, 3<br>8 | Tables 1.1, 1.2 and 1.5 revised: “main clock” → “XIN clock”; “sub clock” → “XCIN clock” |
| | | 15 | - 0023h to 0025h: 40MHz On-Chip Oscillator Control Register<br>→ High-Speed On-Chip Oscillator Control Register |
| 0.30 | Sep 01, 2005 | 2, 3 | Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance<br>• Serial Interface revised:<br>- Serial Interface: 2 channels Clock synchronous serial I/O, UART<br>- Clock Synchronous Serial Interface: 1 channel<br>$I^2C$ bus Interface(1), Clock synchronous serial I/O with chip select |
| | | 4 | Figure 1.1 Block Diagram<br>• UART or Clock Synchronous Serial Interface: “(8 bits × 1 channel)” → “(8 bits × 2 channels)” revised<br>• UART (8 bits × 1 channel) deleted |
| | | 5, 6 | Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group<br>“Flash Memory Version” → “N Version” revised |

| REVISION HISTORY | R8C/24 Group, R8C/25 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.00 | Jul 14, 2006 | all pages | “PTLG0064JA-A (64F0G)” package added |
| | | 1 | 1. Overview; “... or a 64-pin molded-plastic FLGA.“ added |
| | | 2, 3 | Table 1.1 Functions and Specifications for R8C/24 Group, Table 1.2 Functions and Specifications for R8C/25 Group;<br>Package: “64-pin molded-plastic FLGA” added |
| | | 5 | Table 1.3 Product Information for R8C/24 Group, Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group revised |
| | | 6 | Table 1.4 Product Information for R8C/25 Group, Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group revised |
| | | 7 | Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View);<br>NOTE3 revised |
| | | 8 | Figure 1.5 PTLG0064JA-A Package Pin Assignments added |
| | | 14 | Figure 3.1 Memory Map of R8C/24 Group revised |
| | | 15 | Figure 3.2 Memory Map of R8C/25 Group revised |
| | | 23 | Table 5.1 Absolute Maximum Ratings; NOTE1 added |
| | | 47 | Package Dimensions; “PTLG0064JA-A (64F0G)” added |
| 3.00 | Feb 29, 2008 | all pages | Y version added<br>Factory programming product added |
| | | 2, 3 | Table 1.1, Table 1.2 Clock; “Real-time clock (timer RE)” added |
| | | 5, 7 | Table 1.3, Table 1.4 revised |
| | | 6, 8 | Figure 1.2, Figure 1.3; ROM number “XXX” added |
| | | 16, 17 | Figure 3.1, Figure 3.2; “Expanded area” deleted |
| | | 18 | Table 4.1 revised |
| | | 26 | Table 5.2 NOTE2 revised |
| | | 32 | Table 5.10; revised, NOTE4 added<br>Table 5.11; Oscillation stability time: Condition “$V_{CC}$ = 5.0 V, Topr = 25°C” deleted |
| | | 38 | Table 5.15; $I_{IH}$, $I_{IL}$, $R_{PULLUP}$ Condition: “Vcc = 5V” added |
| | | 39 | Table 5.16; Condition: High-speed on-chip oscillator mode revised |
| | | 40 | Table 5.17 added |
| | | 41 | Figure 5.8 revised |
| | | 43 | Table 5.22; $I_{IH}$, $I_{IL}$, $R_{PULLUP}$ Condition: “Vcc = 3V” added |
| | | 44 | Table 5.23; Condition “Increase during A/D converter operation” added |
| | | 45 | Figure 5.12 revised |
| | | 48 | Table 5.29; Condition “Increase during A/D converter operation” added |
| | | 49 | Figure 5.16 revised |
| | | | |

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