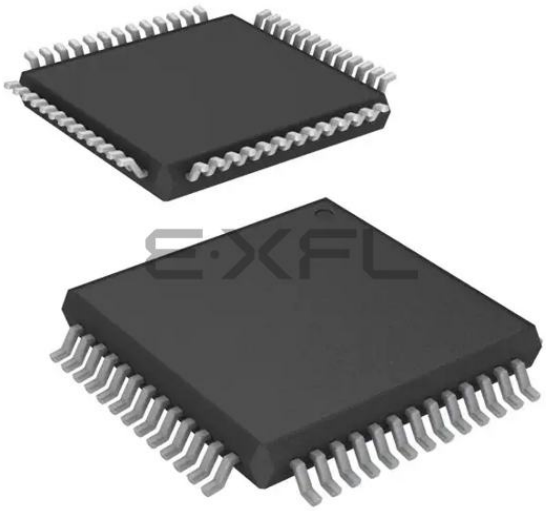
Renesas Electronics America Inc - R5F21255SNFP#X6 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21255snfp-x6

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

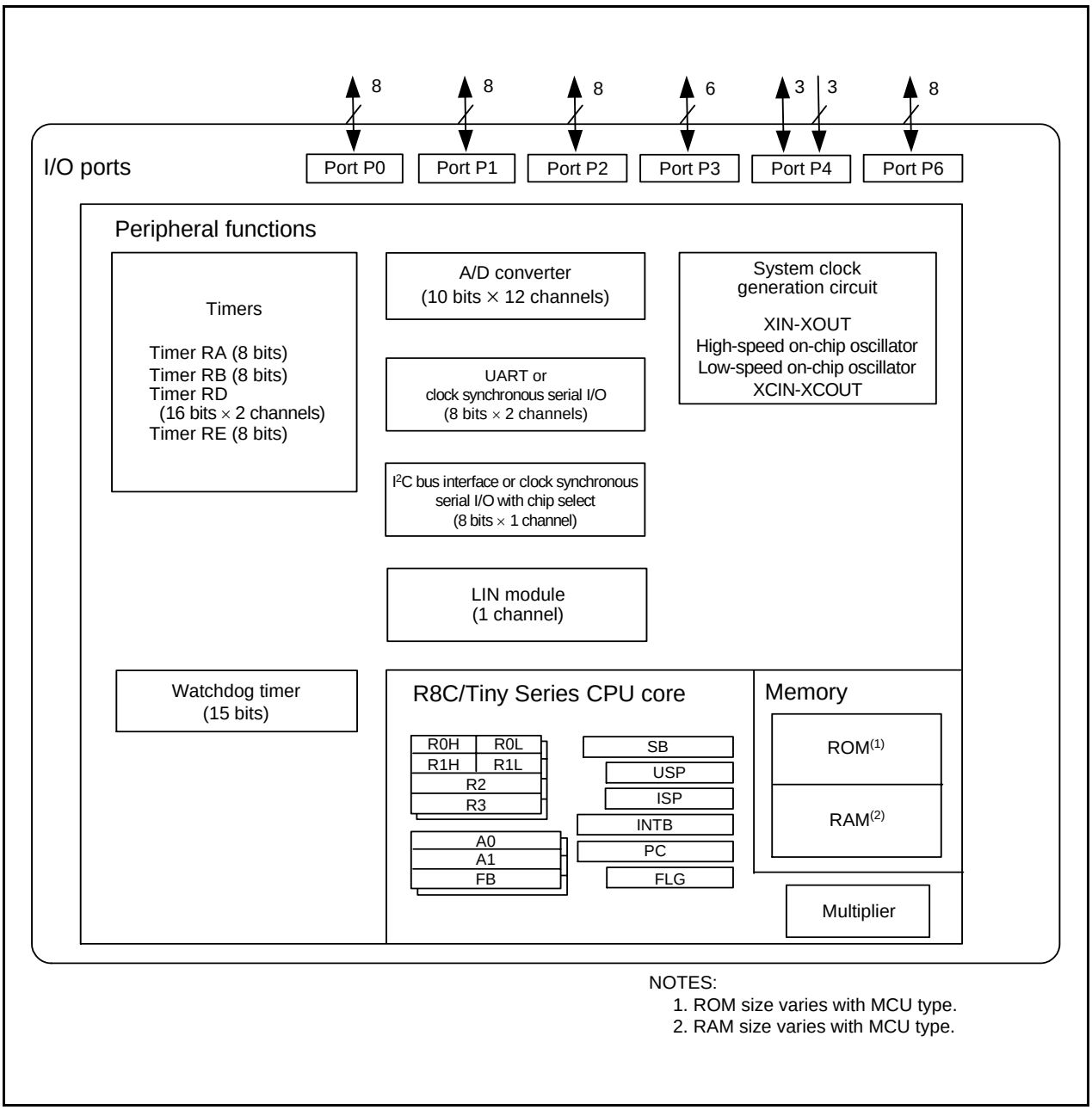


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information for R8C/24 Group and Table 1.4 lists the Product Information for R8C/25 Group.

Table 1.3 Product Information for R8C/24 Group **Current of Feb. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21244SNFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21245SNFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	
R5F21244SDFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	D version Blank product
R5F21245SDFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Factory programming product(1)
R5F21245SNXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNXXXLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	
R5F21244SDXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	D version Factory programming product(1)
R5F21245SDXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	

NOTE:
1. The user ROM is programmed before shipment.

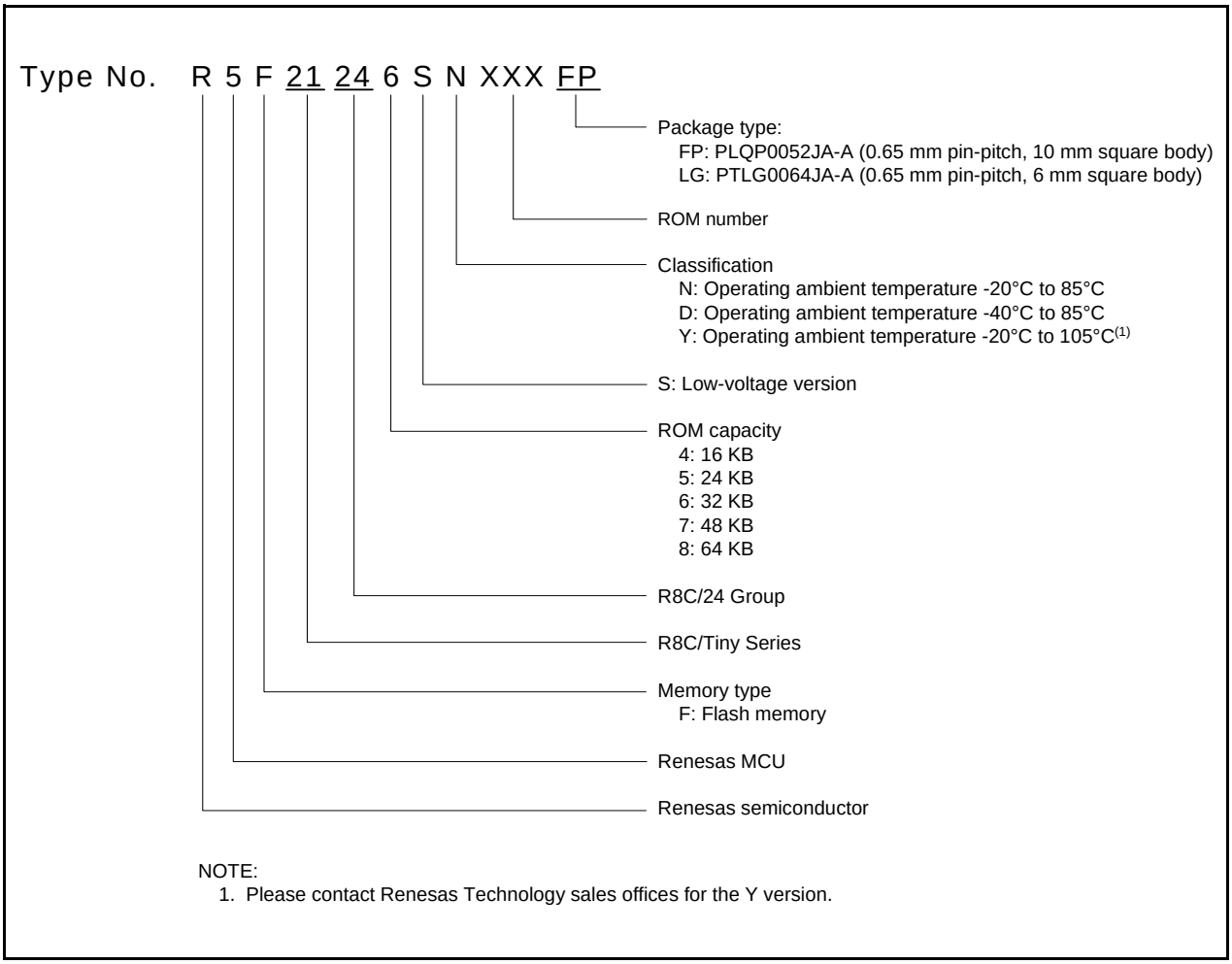


Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group

Pin assignments (top perspective view)

	A	B	C	D	E	F	G	H	
8	3 P3_3/SSI	50 P0_1/AN6	48 P0_3/AN4	46 P6_2	45 P6_0/TREO	NC	36 P6_4	NC	8
7	4 P3_4/SDA/$\overline{\text{SCS}}$	51 P0_0/AN7	49 P0_2/AN5	NC	44 P4_2/VREF	34 P3_0/TRAO	35 P6_5/CLK1	NC	7
6	NC	5 MODE	52 P3_7/SSO	47 P6_1	43 P0_4/AN3	42 P0_5/AN2	NC	33 P3_1/TRBO	6
5	7 P4_4/XCOUT	NC	6 P4_3/XCIN	2 P3_5/SCL/SSCK	37 P6_3	NC	41 P0_6/AN1	38 P0_7/AN0	5
4	13 P2_7/TRDIOD1	12 VCC/AVCC	NC	9 XOUT/P4_7(1)	8 $\overline{\text{RESET}}$	32 P1_0/$\overline{\text{KI0}}$/AN8	31 P1_1/$\overline{\text{KI1}}$/AN9	NC	4
3	NC	10 VSS/AVSS	16 P2_4/TRDIOA1	19 P2_1/TRDIOB0	23 P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)(2)	NC	NC	30 P1_2/$\overline{\text{KI2}}$/AN10	3
2	NC	11 XIN/P4_6	17 P2_3/TRDIOD0	20 P2_0/TRDIOA0/TRDCLK	NC	24 P1_4/TXD0	28 P6_6/$\overline{\text{INT2}}$/TXD1	NC	2
1	14 P2_6/TRDIOC1	15 P2_5/TRDIOB1	18 P2_2/TRDIOC0	21 P1_7/TRAIO/$\overline{\text{INT1}}$	22 P1_6/CLK0	25 P1_3/$\overline{\text{KI3}}$/AN11	27 P4_5/$\overline{\text{INT0}}$	29 P6_7/$\overline{\text{INT3}}$/RXD1	1
	A	B	C	D	E	F	G	H	

Package: PTLG0064JA-A(64F0G)
0.65 mm pin pitch, 6 mm square body

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. In the figure, the numbers in circles are the pin numbers of the 52-pin LQFP package (PLQP0052JA-A).
   NC: Non-Connection

R5F21244S
NLG
JAPAN

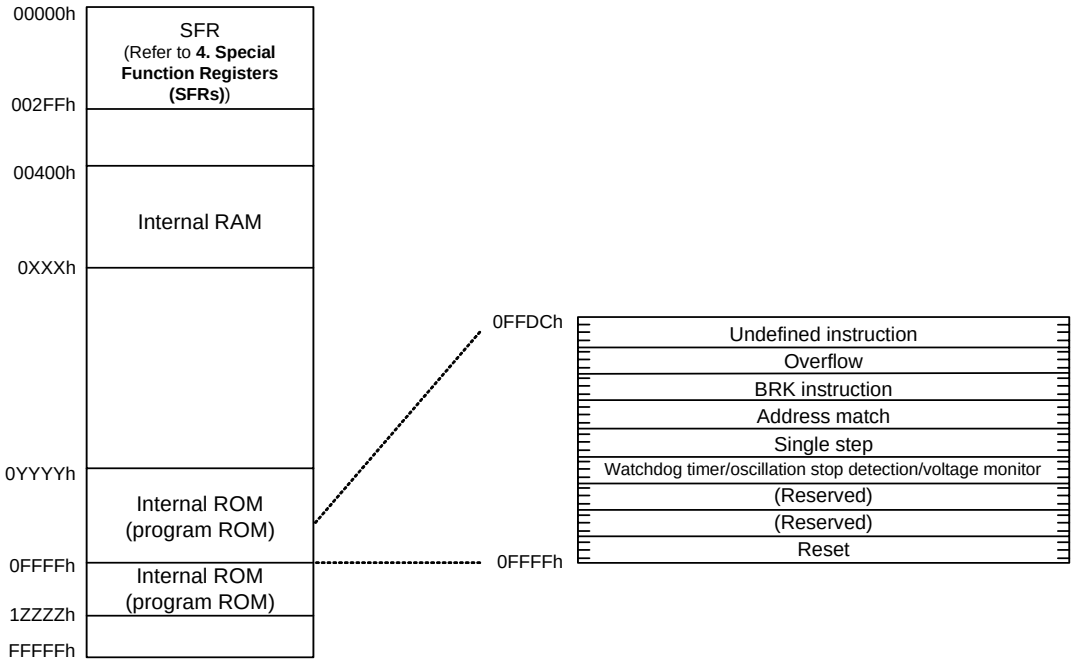
Pin assignments (top view)

Figure 1.5 PTLG0064JA-A Package Pin Assignments

3. Memory

3.1 R8C/24 Group

Figure 3.1 is a Memory Map of R8C/24 Group. The R8C/24 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM area is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address 1ZZZZh	Size	Address 0XXXXh
R5F21244SNFP, R5F21244SNXXXFP, R5F21244SDFP, R5F21244SDXXXFP, R5F21244SNLG, R5F21244SNXXXLG	16 Kbytes	0C000h	–	1 Kbyte	007FFh
R5F21245SNFP, R5F21245SNXXXFP, R5F21245SDFP, R5F21245SDXXXFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21246SNFP, R5F21246SNXXXFP, R5F21246SDFP, R5F21246SDXXXFP, R5F21246SNLG, R5F21246SNXXXLG	32 Kbytes	08000h	–	2 Kbytes	00BFFh
R5F21247SNFP, R5F21247SNXXXFP, R5F21247SDFP, R5F21247SDXXXFP	48 Kbytes	04000h	–	2.5 Kbytes	00DFFh
R5F21248SNFP, R5F21248SNXXXFP, R5F21248SDFP, R5F21248SDXXXFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh

Figure 3.1 Memory Map of R8C/24 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b[6]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 00100000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[5]	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register[2]	VW0C	0000X000b[3] 0100X001b[4]
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset or the LVD0ON bit in the OFS register is set to 0, and hardware reset.
5. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P2 Drive Capacity Control Register	P2DRR	00h
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}	–	–	10	Bit
–	Absolute accuracy	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 3.3 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 3.3 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 5 MHz, V_{ref} = AV_{CC} = 2.2 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 5 MHz, V_{ref} = AV_{CC} = 2.2 V	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = AV_{CC}	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage(2)			0	–	AV_{CC}	V
–	A/D operating clock frequency	Without sample and hold	V_{ref} = AV_{CC} = 2.7 to 5.5 V	0.25	–	10	MHz
		With sample and hold	V_{ref} = AV_{CC} = 2.7 to 5.5 V	1	–	10	MHz
		Without sample and hold	V_{ref} = AV_{CC} = 2.2 to 5.5 V	0.25	–	5	MHz
		With sample and hold	V_{ref} = AV_{CC} = 2.2 to 5.5 V	1	–	5	MHz

NOTES:
1. AV_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

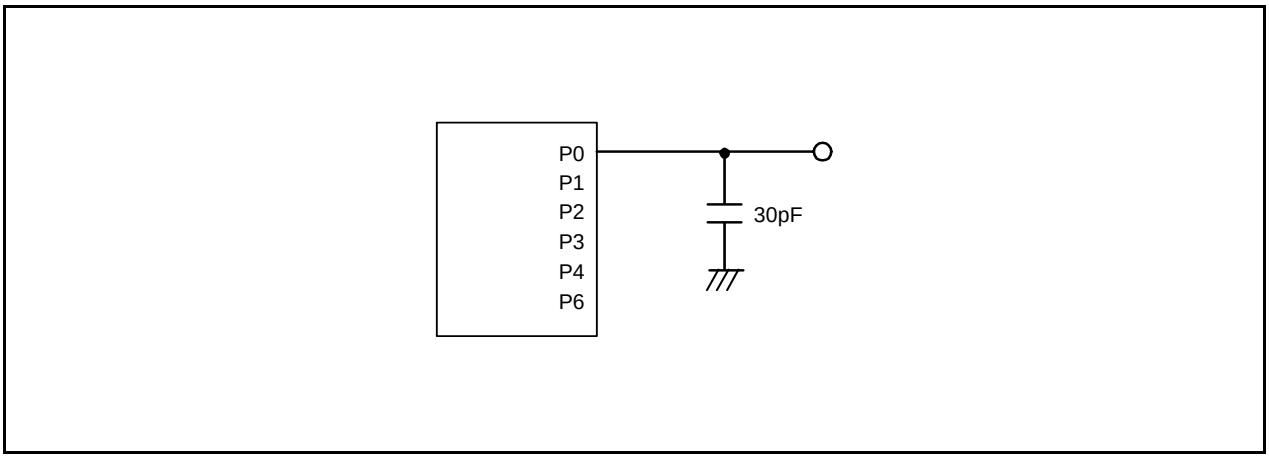


Figure 5.1 Ports P0 to P4, P6 Timing Measurement Circuit

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		-20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 to 5.25 V 0°C ≤ T_{opr} ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	38.8	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C	38.4	40	40.8	MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 2.7 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38	40	42	MHz
		V_{CC} = 2.7 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	37.6	40	42.4	MHz
		V_{CC} = 2.2 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(3)	35.2	40	44.8	MHz
		V_{CC} = 2.2 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(3)	34	40	46	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4)	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864		MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	-3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

NOTES:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Standard values when the FRA1 register value after reset is assumed.
3. Standard values when the corrected value of the FRA6 register has been written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.15 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200 µA		V_{CC} – 0.5	–	V_{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 µA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 µA		–	–	0.45	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 µA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, KI1, KI2, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, Vcc = 5V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 5V		–	–	-5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, Vcc = 5V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.18 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

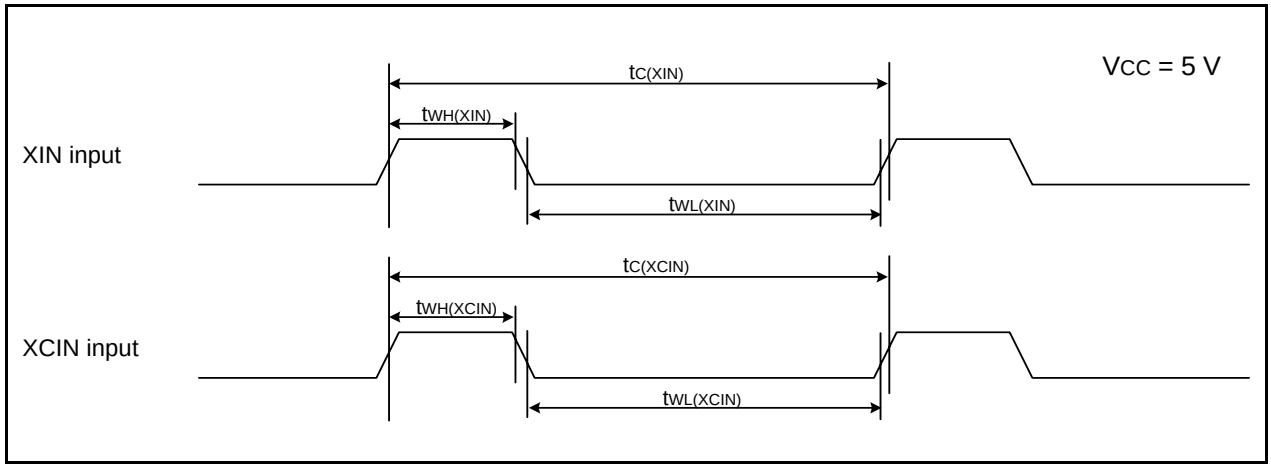


Figure 5.8 XIN Input and XCIN Input Timing Diagram when Vcc = 5 V

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

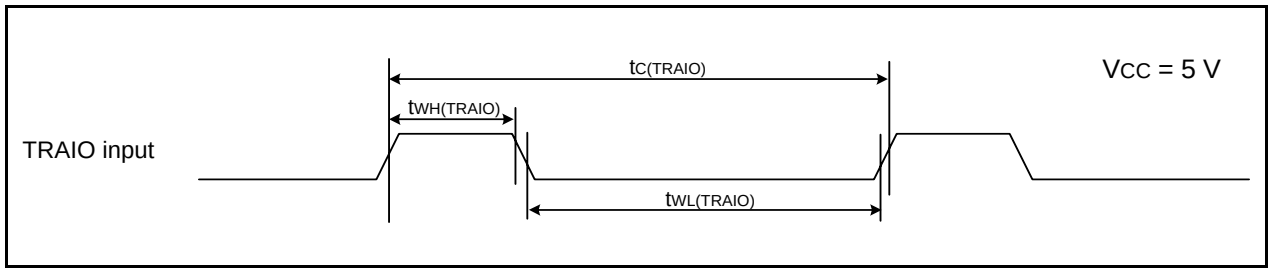


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.23 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	9	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	70	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	55	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.8	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.0	–	µA
		Increase during A/D converter operation	Without sample & hold	–	0.9	–	mA
			With sample & hold	–	0.5	–	mA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

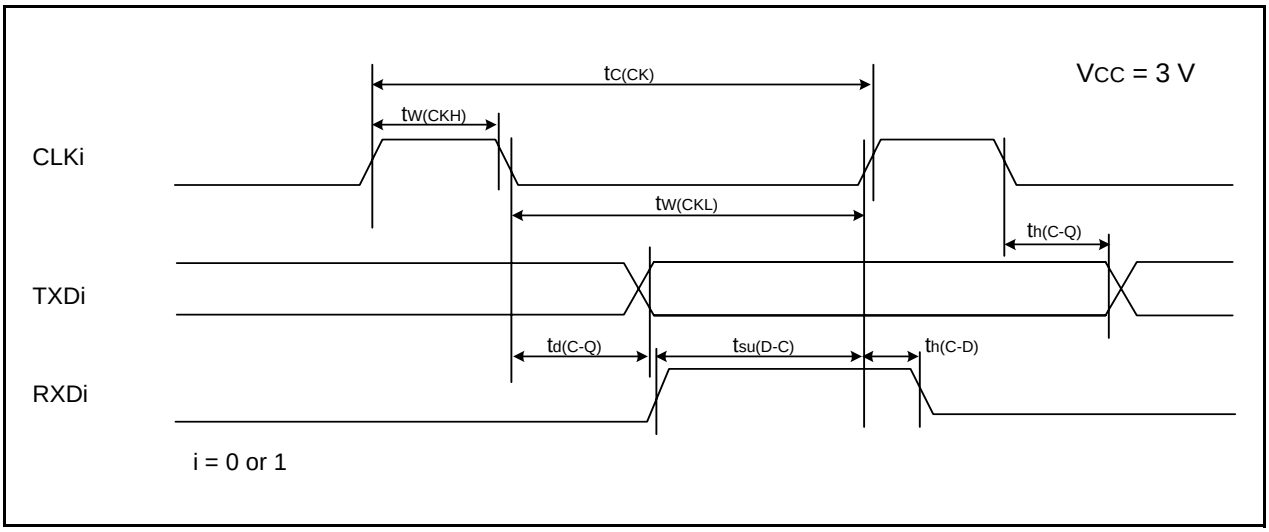


Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

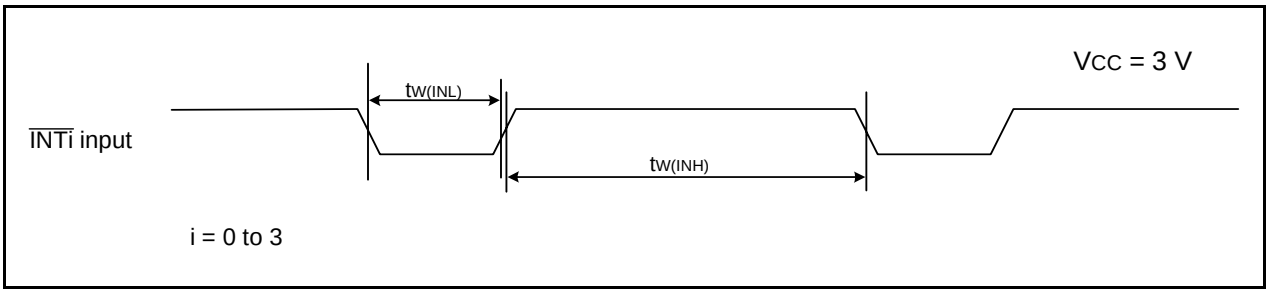


Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V

Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	100	230	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	25	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.0	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	1.8	–	µA
		Increase during A/D converter operation	Without sample & hold	–	0.4	–	mA
			With sample & hold	–	0.3	–	mA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

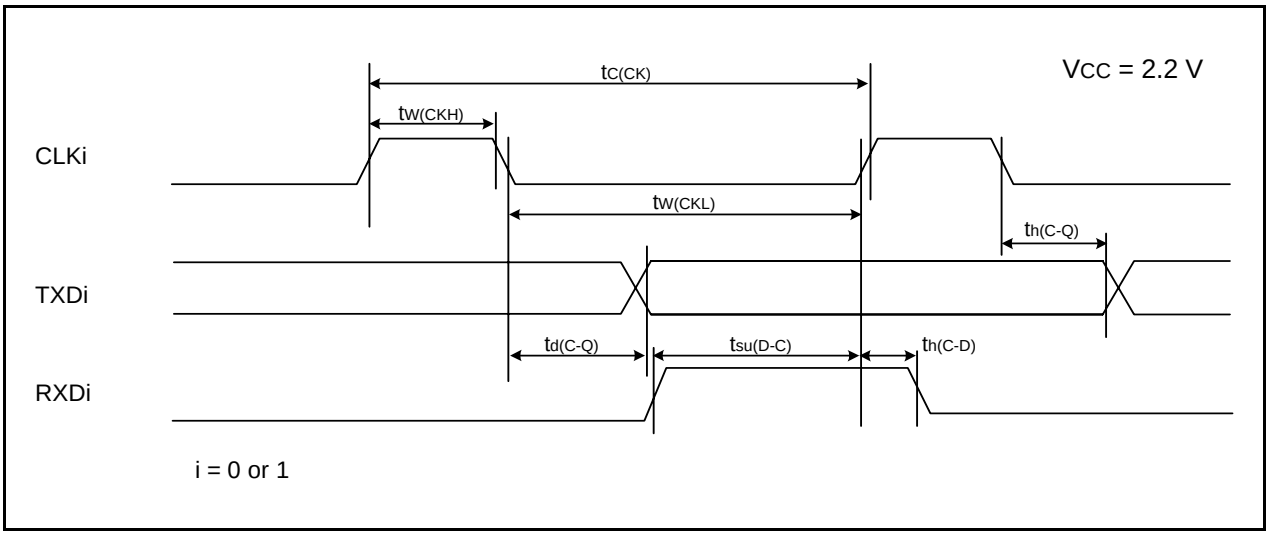


Figure 5.18 Serial Interface Timing Diagram when VCC = 2.2 V

Table 5.33 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	1000(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	1000(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

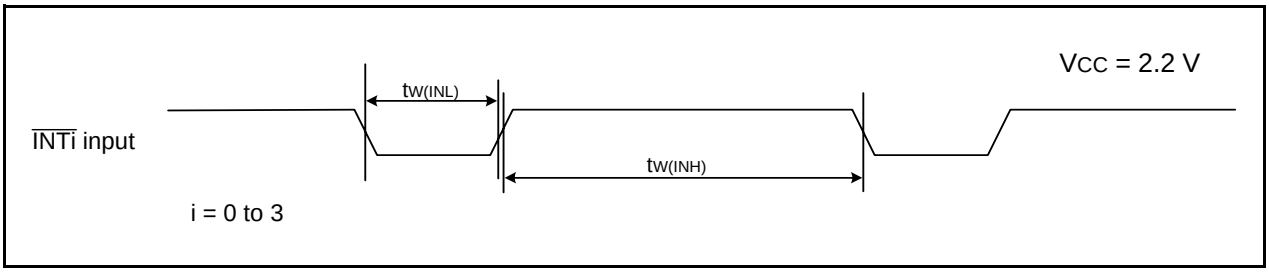


Figure 5.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 2.2 V

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.40	Jan 24, 2006	46	Package Dimensions; "TBD" → "PLQP0052JA-A (52P6A-A)" added
1.00	May 31, 2006	all pages	"Under development" deleted
		1	1. Overview; "data flash ROM" → "data flash" revised
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; "System clock generator" → "System clock generation circuit" revised
		5 to 6	Table 1.3 Product Information for R8C/24 Group and Table 1.4 Product Information for R8C/25 Group; A part of (D) mark is deleted.
		9	Table 1.6 Pin Name Information by Pin Number NOTE1 added
		15	Table 4.1 SFR Information(1); 001Ch: "00h" → "00h, 10000000b" revised 0029h: High-Speed On-Chip Oscillator Control Register 4 FRA4 When shipping added 002Bh: High-Speed On-Chip Oscillator Control Register 6 FRA6 When shipping added NOTE6 added
		19	Table 4.5 SFR Information(5); 0118h: Timer RE Second Data Register / Counter Data Register, 0119h: Timer RE Minute Data Register / Compare Data Register register name revised
		20	Table 4.6 SFR Information(6); 0143h: "11000000b" → "11100000b" revised
		22	Table 5.2 Recommended Operating Conditions revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics revised
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics revised
		26	Figure 5.2 Time delay until Suspend title revised
		27	Table 5.9 Voltage Monitor 0 Reset Electrical Characteristics → Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics revised Table 5.10 Power-on Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 0 Reset) deleted Figure 5.3 Power-on Reset Circuit Electrical Characteristics revised
		28	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised
		35	Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] revised
		39	Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] revised
		43	Table 5.28 Electrical Characteristics (6) [Vcc = 2.2 V] revised
		46	Package Dimensions; "The latest package ... Renesas Technology website." added

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Jul 14, 2006	all pages	“PTLG0064JA-A (64F0G)” package added
		1	1. Overview; “... or a 64-pin molded-plastic FLGA.“ added
		2, 3	Table 1.1 Functions and Specifications for R8C/24 Group, Table 1.2 Functions and Specifications for R8C/25 Group; Package: “64-pin molded-plastic FLGA” added
		5	Table 1.3 Product Information for R8C/24 Group, Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group, Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group revised
		7	Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View); NOTE3 revised
		8	Figure 1.5 PTLG0064JA-A Package Pin Assignments added
		14	Figure 3.1 Memory Map of R8C/24 Group revised
		15	Figure 3.2 Memory Map of R8C/25 Group revised
		23	Table 5.1 Absolute Maximum Ratings; NOTE1 added
		47	Package Dimensions; “PTLG0064JA-A (64F0G)” added
3.00	Feb 29, 2008	all pages	Y version added Factory programming product added
		2, 3	Table 1.1, Table 1.2 Clock; “Real-time clock (timer RE)” added
		5, 7	Table 1.3, Table 1.4 revised
		6, 8	Figure 1.2, Figure 1.3; ROM number “XXX” added
		16, 17	Figure 3.1, Figure 3.2; “Expanded area” deleted
		18	Table 4.1 revised
		26	Table 5.2 NOTE2 revised
		32	Table 5.10; revised, NOTE4 added Table 5.11; Oscillation stability time: Condition “V_{CC} = 5.0 V, Topr = 25°C” deleted
		38	Table 5.15; I_{IH}, I_{IL}, R_{PULLUP} Condition: “Vcc = 5V” added
		39	Table 5.16; Condition: High-speed on-chip oscillator mode revised
		40	Table 5.17 added
		41	Figure 5.8 revised
		43	Table 5.22; I_{IH}, I_{IL}, R_{PULLUP} Condition: “Vcc = 3V” added
		44	Table 5.23; Condition “Increase during A/D converter operation” added
		45	Figure 5.12 revised
		48	Table 5.29; Condition “Increase during A/D converter operation” added
		49	Figure 5.16 revised

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