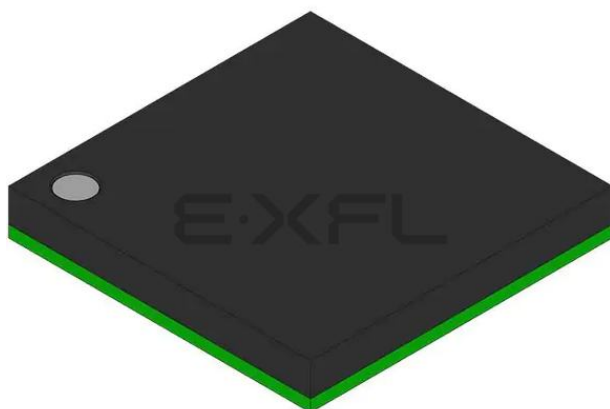




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFLGA
Supplier Device Package	64-TFLGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21256snlg-u0

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and are packaged in a 52-pin molded-plastic LQFP or a 64-pin molded-plastic FLGA. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/25 Group has on-chip data flash (1 KB x 2 blocks).

The difference between the R8C/24 Group and R8C/25 Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/24 Group and Table 1.2 outlines the Functions and Specifications for R8C/25 Group.

Table 1.1 Functions and Specifications for R8C/24 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 2.2$ to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.3 Product Information for R8C/24 Group
Peripheral Functions	Ports	I/O ports: 41 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins
	Timers	Timer RA: 8 bits $\times$ 1 channel Timer RB: 8 bits $\times$ 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits $\times$ 2 channels (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function
	Serial interfaces	2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface	1 channel I ² C bus Interface ⁽¹⁾ Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits $\times$ 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels
	Clock	Clock generation circuits
		3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz)
		Real-time clock (timer RE)
	Oscillation stop detection function	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	$VCC = 3.0$ to 5.5 V ($f(XIN) = 20$ MHz) $VCC = 2.7$ to 5.5 V ($f(XIN) = 10$ MHz) $VCC = 2.2$ to 5.5 V ($f(XIN) = 5$ MHz)
	Current consumption	Typ. 10 mA ($VCC = 5.0$ V, $f(XIN) = 20$ MHz) Typ. 6 mA ($VCC = 3.0$ V, $f(XIN) = 10$ MHz) Typ. 2.0 μ A ($VCC = 3.0$ V, wait mode ($f(XCIN) = 32$ kHz)) Typ. 0.7 μ A ($VCC = 3.0$ V, stop mode)
Flash Memory	Programming and erasure voltage	$VCC = 2.7$ to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C (N version)
		-40 to 85°C (D version) ⁽²⁾
		-20 to 105°C (Y version) ⁽³⁾
Package		52-pin molded-plastic LQFP
		64-pin molded-plastic FLGA

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

1.4 Product Information

Table 1.3 lists the Product Information for R8C/24 Group and Table 1.4 lists the Product Information for R8C/25 Group.

Table 1.3 Product Information for R8C/24 Group

Current of Feb. 2008

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21244SNFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21245SNFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	D version Blank product
R5F21244SDFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	
R5F21245SDFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Factory programming product ⁽¹⁾
R5F21245SNXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNXXXLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	D version Factory programming product ⁽¹⁾
R5F21244SDXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	
R5F21245SDXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	

NOTE:

1. The user ROM is programmed before shipment.

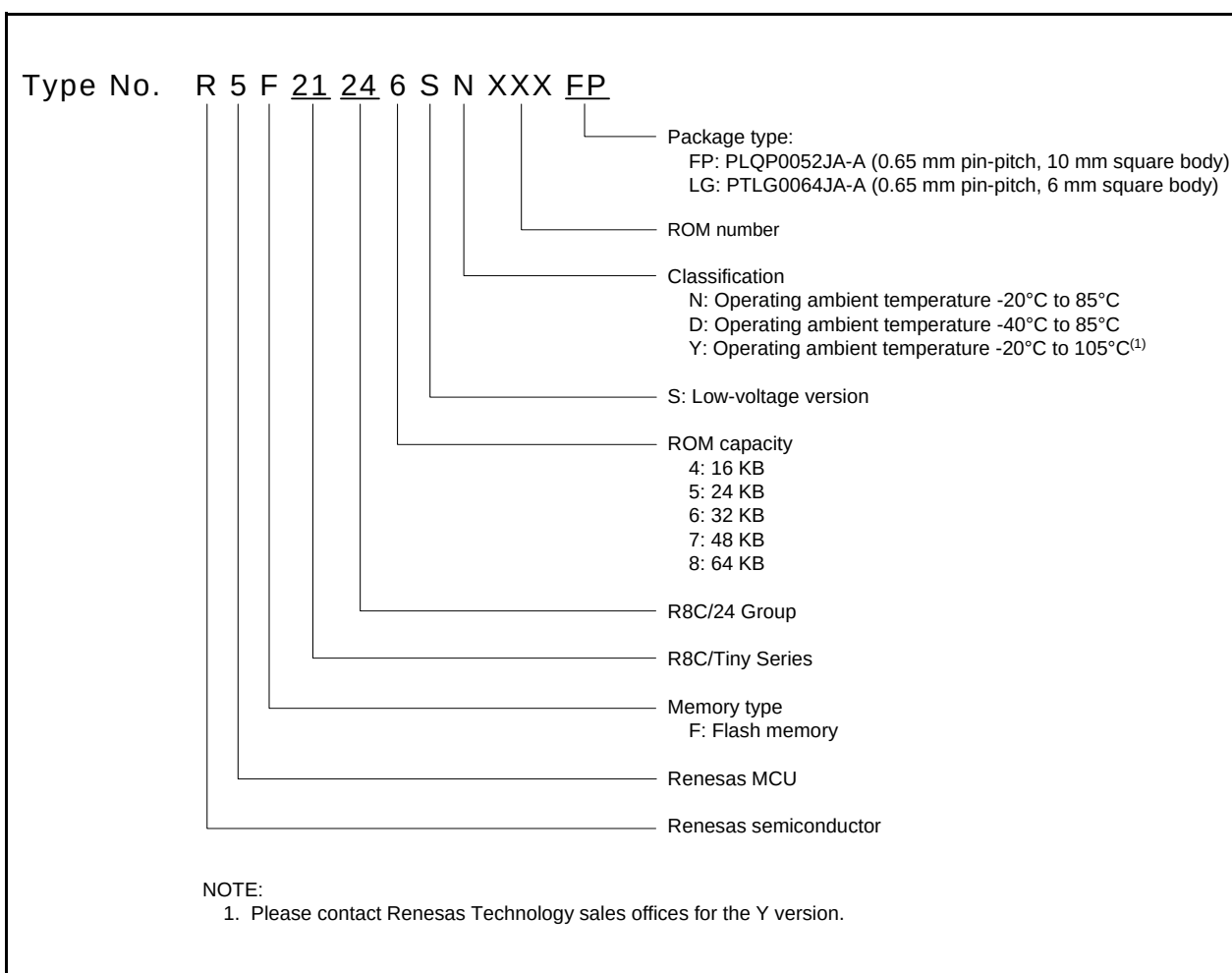


Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.5 SFR Information (5)⁽¹⁾

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRES	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)⁽¹⁾

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIOA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIOA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)⁽¹⁾

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V _{CC} = 4.75 to 5.25 V 0°C ≤ T _{opr} ≤ 60°C ⁽²⁾	39.2	40	40.8	MHz
		V _{CC} = 4.5 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C	38.8	40	40.8	MHz
		V _{CC} = 4.5 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C	38.4	40	40.8	MHz
		V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.8	40	41.2	MHz
		V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38.4	40	41.6	MHz
		V _{CC} = 2.7 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	38	40	42	MHz
		V _{CC} = 2.7 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	37.6	40	42.4	MHz
		V _{CC} = 2.2 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽³⁾	35.2	40	44.8	MHz
		V _{CC} = 2.2 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽³⁾	34	40	46	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register ⁽⁴⁾	V _{CC} = 5.0 V, T _{opr} = 25°C	—	36.864	—	MHz
		V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C	-3%	—	3%	%
—	Value in FRA1 register after reset		08h	—	F7h	—
—	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	—	+0.3	—	MHz
—	Oscillation stability time		—	10	100	μs
—	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	—	400	—	μA

NOTES:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Standard values when the FRA1 register value after reset is assumed.
3. Standard values when the corrected value of the FRA6 register has been written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
—	Oscillation stability time		—	10	100	μs
—	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	—	15	—	μA

NOTE:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	—	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		—	—	150	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

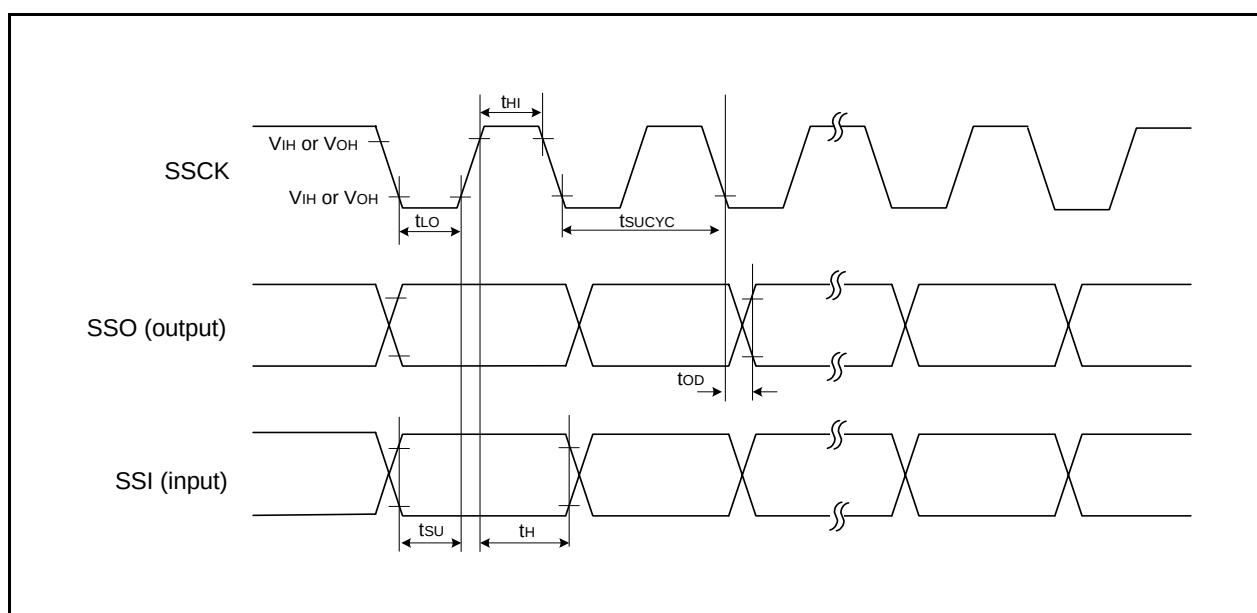


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.14 Timing Requirements of I²C bus Interface⁽¹⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{CYC} + 600 ⁽²⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3t _{CYC} + 300 ⁽²⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5t _{CYC} + 500 ⁽²⁾	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1t _{CYC} ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{CYC} ⁽²⁾	–	–	ns
t _{STAH}	Start condition input hold time		3t _{CYC} ⁽²⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3t _{CYC} ⁽²⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3t _{CYC} ⁽²⁾	–	–	ns
t _{SDAS}	Data input setup time		1t _{CYC} + 20 ⁽²⁾	–	–	ns
t _{SDAH}	Data input hold time		0	–	–	ns

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1t_{CYC} = 1/f₁(s)

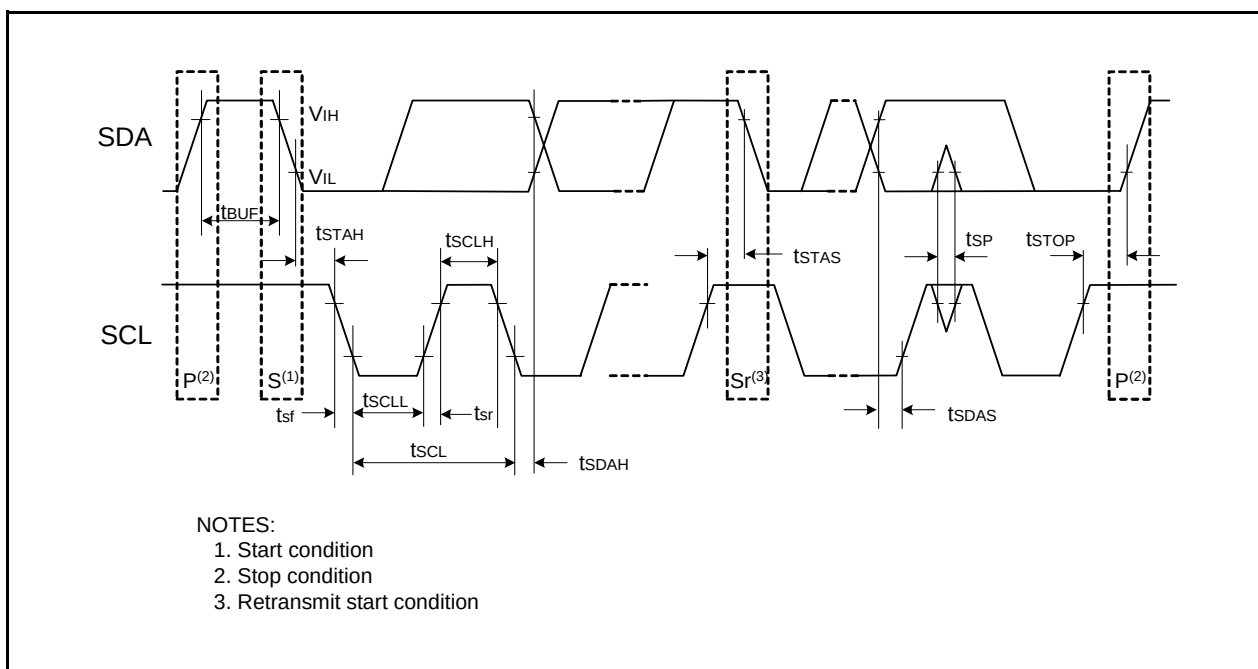
**Figure 5.7 I/O Timing of I²C bus Interface**

Table 5.15 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output "H" voltage	Except P2_0 to P2_7, XOUT	IOH = -5 mA	Vcc - 2.0	—	Vcc	V
			IOH = -200 μ A	Vcc - 0.5	—	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH IOH = -20 mA	Vcc - 2.0	—	Vcc	V
			Drive capacity LOW IOH = -5 mA	Vcc - 2.0	—	Vcc	V
		XOUT	Drive capacity HIGH IOH = -1 mA	Vcc - 2.0	—	Vcc	V
			Drive capacity LOW IOH = -500 μ A	Vcc - 2.0	—	Vcc	V
VOL	Output "L" voltage	Except P2_0 to P2_7, XOUT	IOL = 5 mA	—	—	2.0	V
			IOL = 200 μ A	—	—	0.45	V
		P2_0 to P2_7	Drive capacity HIGH IOL = 20 mA	—	—	2.0	V
			Drive capacity LOW IOL = 5 mA	—	—	2.0	V
		XOUT	Drive capacity HIGH IOL = 1 mA	—	—	2.0	V
			Drive capacity LOW IOL = 500 μ A	—	—	2.0	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO		0.1	0.5	—	V
		RESET		0.1	1.0	—	V
IiH	Input "H" current		VI = 5 V, Vcc = 5V	—	—	5.0	μ A
IiL	Input "L" current		VI = 0 V, Vcc = 5V	—	—	-5.0	μ A
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5V	30	50	167	k Ω
RfXIN	Feedback resistance	XIN		—	1.0	—	M Ω
RfXCIN	Feedback resistance	XCIN		—	18	—	M Ω
VRAM	RAM hold voltage		During stop mode	1.8	—	—	V

NOTE:

1. Vcc = 4.2 to 5.5 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

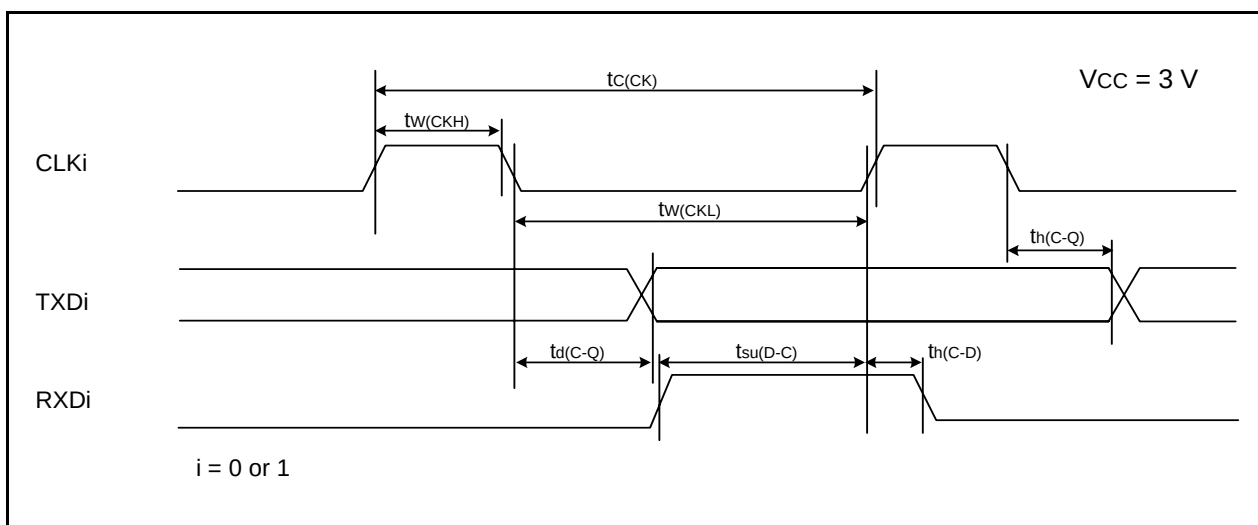
Table 5.16 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	μA

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

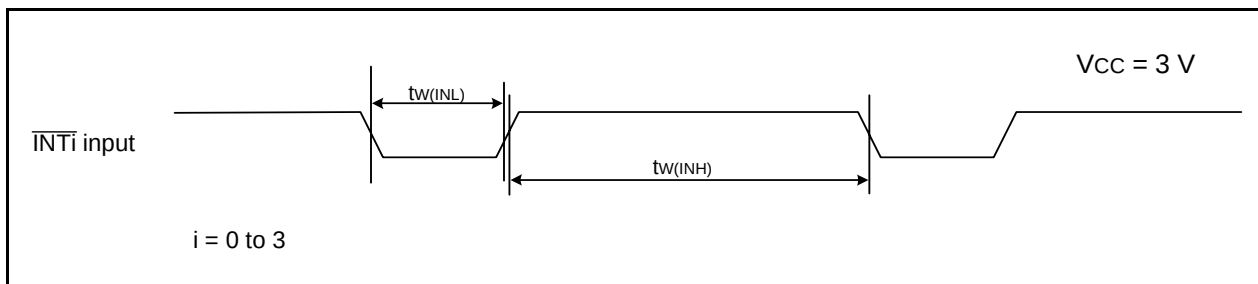
i = 0 or 1

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.27 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	380 ⁽²⁾	—	ns

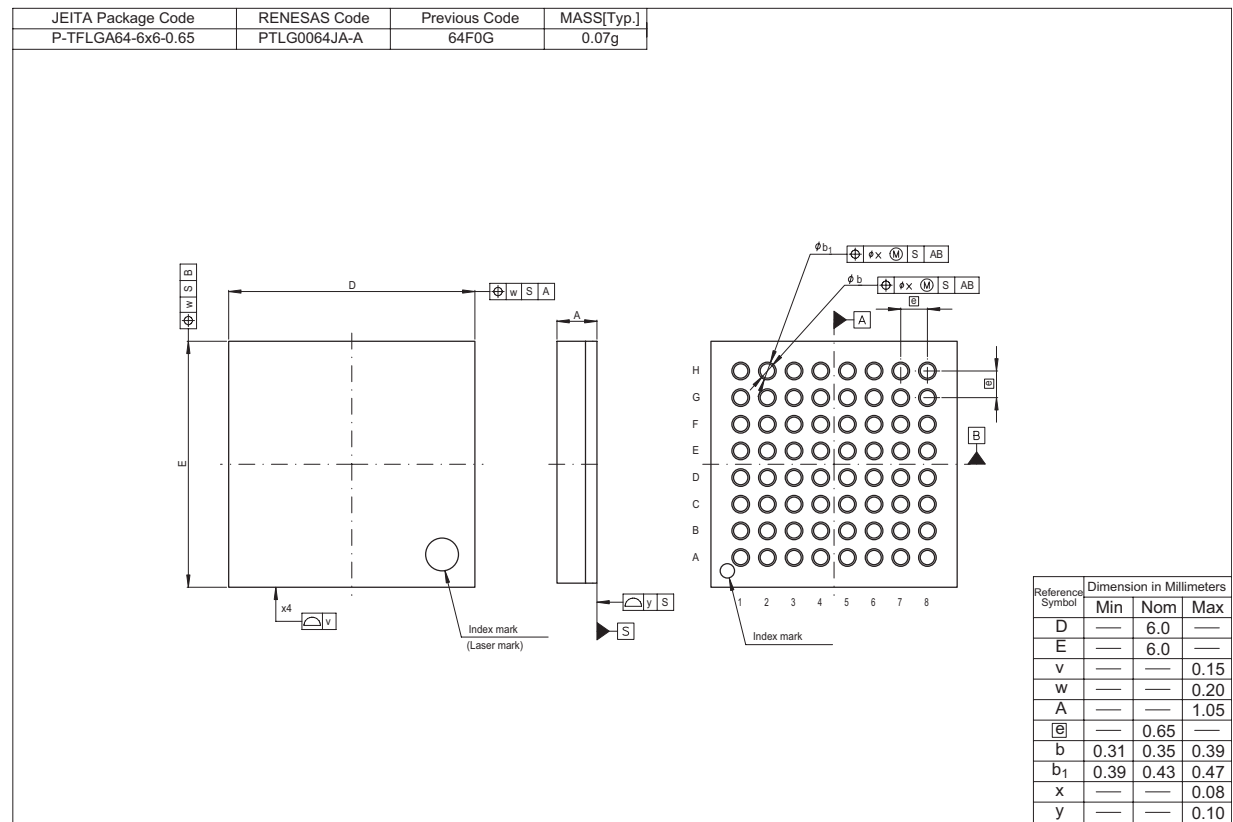
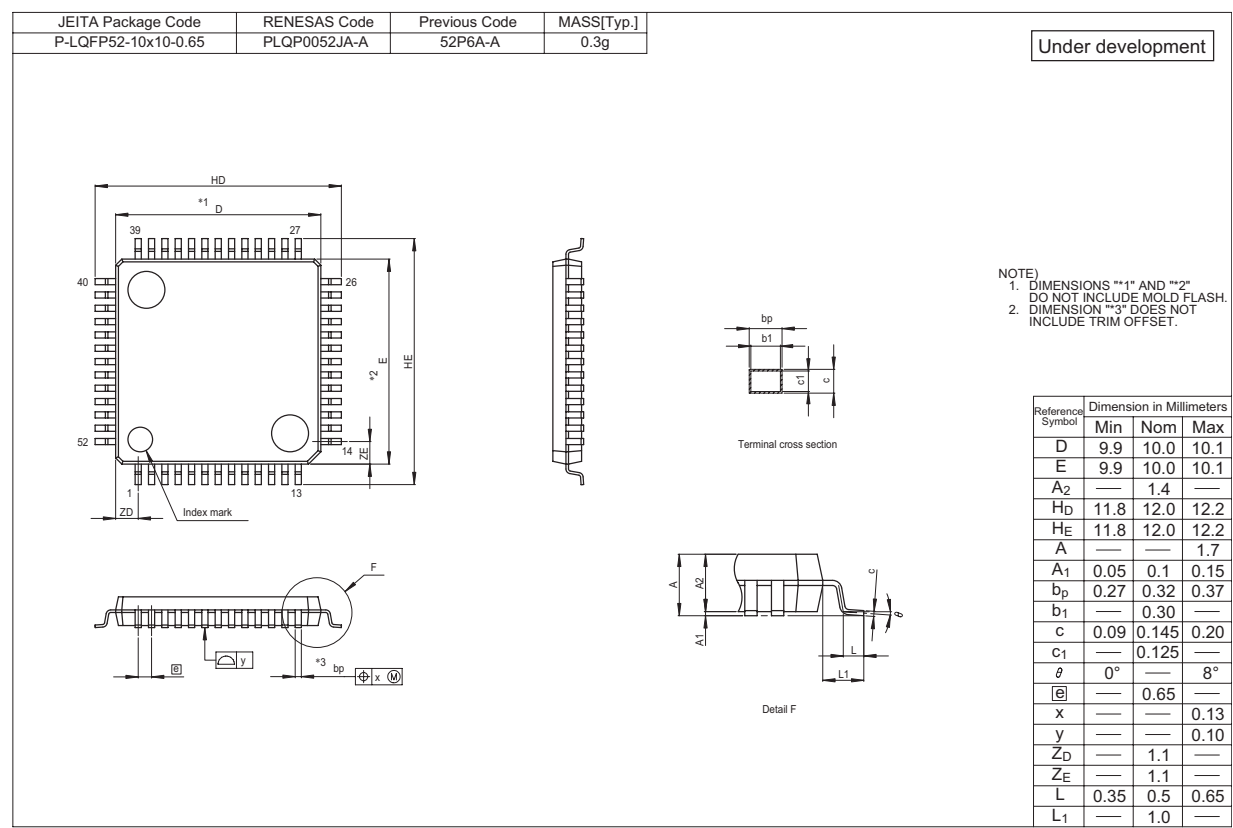
NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Sep 17, 2004	-	First Edition issued
0.02	Dec 10, 2004	All pages 2, 3 4 5, 6 7 8 9 15 16 19	Part Number revised. R8C/26 → R8C/24, R8C/27 → R8C/25 Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance - Serial Interface: I²C Bus Interface and Chip-select clock synchronous (SSU) added. - LIN Module added. - Interrupt: Internal factors revised; 10 → 11 - Note on Operating Ambient Temperature added. Figure 1.1 Block Diagram - LIN Module added. - Chip-select clock synchronous (SSU) is added to I²C Bus Interface. Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group Date and Development state revised. Figure 1.4 Pin Assignment P3_5/SCL → P3_5/SCL/SSCK, P3_3 → P3_3/SSI, P3_4/SDA → P3_4/SDA/SCS, P3_7 → P3_7/SSO, VSS/AVSS → VSS, XIN/P4_6 → P4_6/XIN, VCC/AVSS → VCC 12pin P1_7/TRAO/INT1 to 22pin P1_0/KIO/AN8 → 20pin P1_7/TRAO/INT1 to 30pin P1_0/KIO/AN8 Table 1.5 Pin Description - Analog Power Supply Input eliminated. - SSU added. Table 1.6 Pin Name Information by Pin Number added. Table 4.1 SFR Information (1) - 0031h: Voltage Detection Register 1 → Voltage Detection <u>A</u> Register 1 - 0032h: Voltage Detection Register 1 → Voltage Detection <u>A</u> Register 2 01000001b → 00100001b (Note 4) - 0036h: "(3), 01000001b (4)" eliminated. - 0038h: Voltage Monitor 0 Control Register (2), VW0C, 00001000b (3), 01000001b (4) added. Table 4.2 SFR Information (2) - 0048h: Timer RD0 Interrupt Control Register, RD0IC, XXXXX000b added. - 0049h: Timer RD Interrupt Control Register, RDIC → Timer RD1 Interrupt Control Register, RD1IC - 004Fh: IIC Interrupt Control Register, IIC → IIC/SSU Interrupt Control Register, IIC2IC Table 4.5 SFR Information (3) - 0106h: LIN Control Register, LINCR, 00h added. - 0107h: LIN Status Register, LINST, 00h added.

REVISION HISTORY

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Rev.	Date	Description	
		Page	Summary
0.10	Feb 24, 2005	1 to 3 5, 6	Pin type changed: 48-pin(under consideration) → 52-pin.
		5 to 7	Package type revised: 48-pin LQFP(under consideration) → PLQP0052JA-A
		8	Table 1.5 TCLK added, VREF revised.
		9	Table 1.6 revised.
		13, 14	Figures 3.1 and 3.2 part number revised.
		15	Tabel 4.1 revised: - 000Fh: 000XXXXXb → 00011111b - 0023h: FR0 → FRA0 - 0024h: FR1 → FRA1 - 0025h: FR2 → FRA2 - 0031h: Voltage Detection A Register 1, VC1 → Voltage Detection Register 1, VCA1 - 0032h: Voltage Detection A Register 2, VC2 → Voltage Detection Register 2, VCA2
		17	Tabel 4.3 Register name and the value after reset at 00B8h to 00BFh revised; NOTE2 added.
		19	Tabel 4.5 revised: - 0107h: LINSR → LINST - 0137h to 013Fh: Register symbol revised
		20	Tabel 4.6 revised: - 0140h to 015Fh: Register symbol revised - 0158h, 0159h: Timer RD General Register → Timer RD General Register A1
0.20	Mar 8, 2005	2, 3 8	Tables 1.1, 1.2 and 1.5 revised: "main clock" → "XIN clock"; "sub clock" → "XCIN clock"
		15	- 0023h to 0025h: 40MHz On-Chip Oscillator Control Register → High-Speed On-Chip Oscillator Control Register
0.30	Sep 01, 2005	2, 3	Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance • Serial Interface revised: - Serial Interface: 2 channels Clock synchronous serial I/O, UART - Clock Synchronous Serial Interface: 1 channel I ² C bus Interface ⁽¹⁾ , Clock synchronous serial I/O with chip select
		4	Figure 1.1 Block Diagram • UART or Clock Synchronous Serial Interface: "(8 bits × 1 channel)" → "(8 bits × 2 channels)" revised • UART (8 bits × 1 channel) deleted
		5, 6	Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group "Flash Memory Version" → "N Version" revised

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Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	19	Tabel 4.5 SFR Information(5) revised: • 0118h : Timer RE Second Data Register/Counter Register → Timer RE Second Data Register/Counter Data Register
		20	Tabel 4.6 SFR Information(6) revised: • 0145h POCR0 → TRDPOCR0 • 0146h, 0147h TRDCNT0 → TRD0 • 0148h, 0149h GRA0 → TRDGRA0 • 014Ah, 014Bh GRB0 → TRDGRB0 • 014Ch, 014Dh GRC0 → TRDGRC0 • 014Eh, 014Fh GRD0 → TRDGRD0 • 0155h POCR1 → TRDPOCR1 • 0156h, 0157h TRDCNT1 → TRD1 • 0158h, 0159h GRA1 → TRDGRA1 • 015Ah, 015Bh GRB1 → TRDGRB1 • 015Ch, 015Dh GRC1 → TRDGRC1 • 015Eh, 015Fh GRD1 → TRDGRD1
		21	Tabel 4.7 SFR Information(7) revised: • 01B5h: 01000101b → 1000000Xb • 01B7h: XX000001b → 00000001b • FFFFh: (Note 2) added
		22 to 44	5. Electrical Characteristics added
0.40	Jan 24, 2006	all pages	• “Preliminary” deleted • Symbol name “TRDMDR” → “TRDMR”, “SSUAIC” → “SSUIC”, and “IIC2AIC” → “IICIC” revised • Pin name “TCLK” → “TRDCLK” revised
		2	Table 1.1 Functions and Specifications for R8C/24 Group revised
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; “Peripheral Functions” added, “System Clock Generation” → “System Clock Generator” revised
		5	Table 1.3 Product Information for R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group revised
		7	Figure 1.4 Pin Assignments (Top View) “TCLK” → “TRDCLK” revised
		8	Table 1.5 Pin Functions “TCLK” → “TRDCLK” revised
		9	Table 1.6 Pin Name Information by Pin Number; “TCLK” → “TRDCLK” revised
		10	Figure 2.1 CPU Registers; “Reserved Area” → “Reserved Bit” revised
		12	2.8.10 Reserved Area; “Reserved Area” → “Reserved bit” revised
		13	Figure 3.1 Memory Map of R8C/24 Group; “Program area” → “program ROM” revised
		14	3.2 R8C/25 Group, Figure 3.2 Memory Map of R8C/25 Group; “Data area” → “data flash”, “Program area” → “program ROM” revised

REVISION HISTORY

R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Jul 14, 2006	all pages	"PTLG0064JA-A (64F0G)" package added
		1	1. Overview; "... or a 64-pin molded-plastic FLGA." added
		2, 3	Table 1.1 Functions and Specifications for R8C/24 Group, Table 1.2 Functions and Specifications for R8C/25 Group; Package: "64-pin molded-plastic FLGA" added
		5	Table 1.3 Product Information for R8C/24 Group, Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group, Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group revised
		7	Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View); NOTE3 revised
		8	Figure 1.5 PTLG0064JA-A Package Pin Assignments added
		14	Figure 3.1 Memory Map of R8C/24 Group revised
		15	Figure 3.2 Memory Map of R8C/25 Group revised
		23	Table 5.1 Absolute Maximum Ratings; NOTE1 added
		47	Package Dimensions; "PTLG0064JA-A (64F0G)" added
3.00	Feb 29, 2008	all pages	Y version added
			Factory programming product added
		2, 3	Table 1.1, Table 1.2 Clock; "Real-time clock (timer RE)" added
		5, 7	Table 1.3, Table 1.4 revised
		6, 8	Figure 1.2, Figure 1.3; ROM number "XXX" added
		16, 17	Figure 3.1, Figure 3.2; "Expanded area" deleted
		18	Table 4.1 revised
		26	Table 5.2 NOTE2 revised
		32	Table 5.10; revised, NOTE4 added
			Table 5.11; Oscillation stability time: Condition "Vcc = 5.0 V, Topr = 25°C" deleted
		38	Table 5.15; I _{IH} , I _L , R _{PULLUP} Condition: "Vcc = 5V" added
		39	Table 5.16; Condition: High-speed on-chip oscillator mode revised
		40	Table 5.17 added
		41	Figure 5.8 revised
		43	Table 5.22; I _{IH} , I _L , R _{PULLUP} Condition: "Vcc = 3V" added
		44	Table 5.23; Condition "Increase during A/D converter operation" added
		45	Figure 5.12 revised
		48	Table 5.29; Condition "Increase during A/D converter operation" added
		49	Figure 5.16 revised