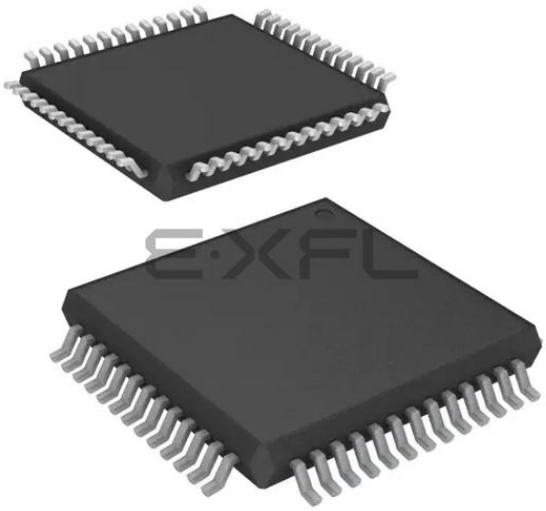

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21257snfp-x6

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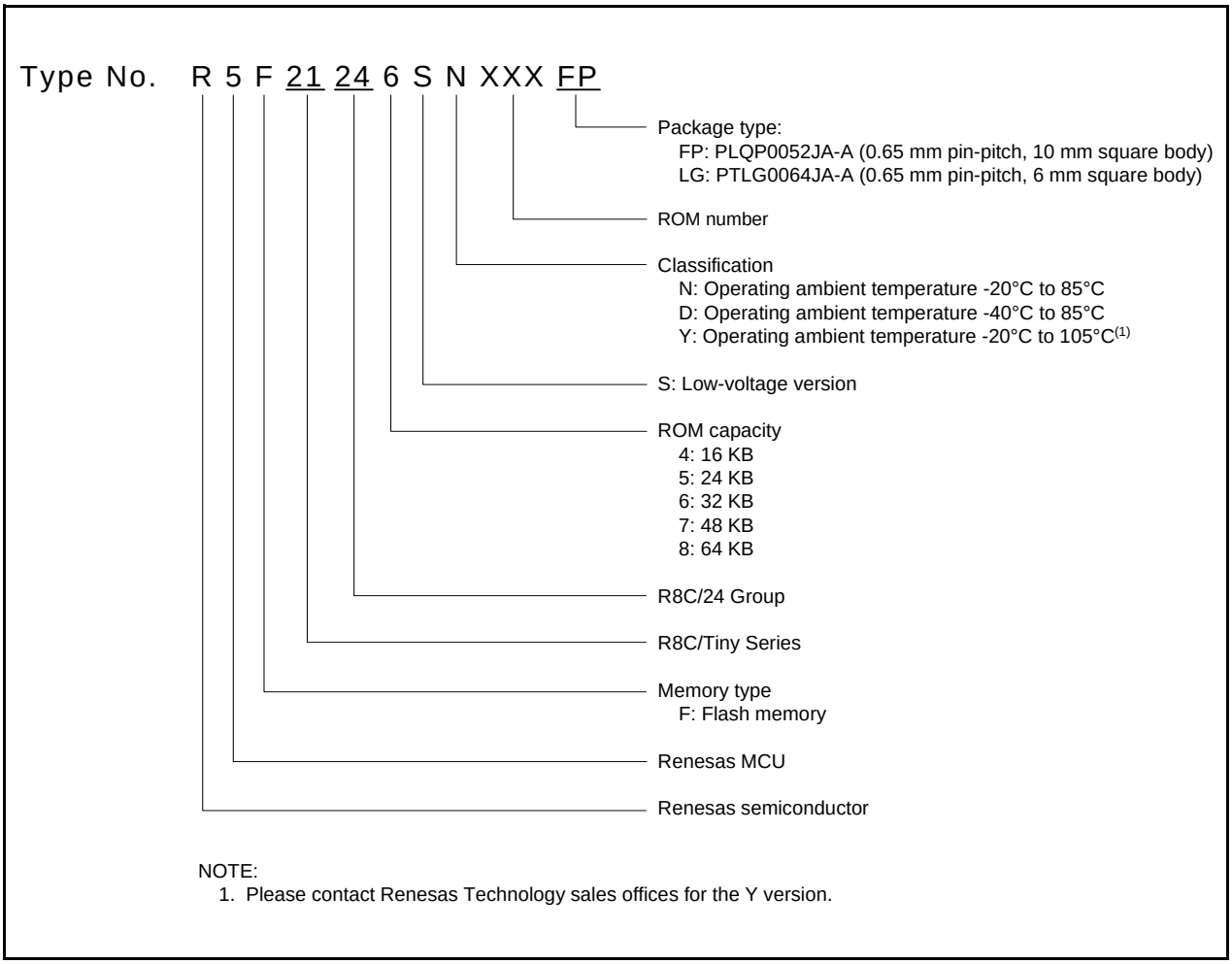

Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C bus Interface	A/D Converter
2		P3_5				SSCK	SCL	
3		P3_3				SSI		
4		P3_4				$\overline{SCS}$	$\overline{SDA}$	
5	MODE							
6	XCIN	P4_3						
7	XCOUT	P4_4						
8	$\overline{RESET}$							
9	XOUT	P4_7						
10	VSS/AVSS							
11	XIN	P4_6						
12	VCC/AVCC							
13		P2_7		TRDIOD1				
14		P2_6		TRDIOC1				
15		P2_5		TRDIOB1				
16		P2_4		TRDIOA1				
17		P2_3		TRDIOD0				
18		P2_2		TRDIOC0				
19		P2_1		TRDIOB0				
20		P2_0		TRDIOA0/TRDCLK				
21		P1_7	$\overline{INT1}$	TRAIO				
22		P1_6			CLK0			
23		P1_5	$\overline{(INT1)}$(1)	(TRAIO)(1)	RXD0			
24		P1_4			TXD0			
25		P1_3	$\overline{KI3}$					AN11
27		P4_5	$\overline{INT0}$	$\overline{INT0}$				
28		P6_6	$\overline{INT2}$		TXD1			
29		P6_7	$\overline{INT3}$		RXD1			
30		P1_2	$\overline{KI2}$					AN10
31		P1_1	$\overline{KI1}$					AN9
32		P1_0	$\overline{KI0}$					AN8
33		P3_1		TRBO				
34		P3_0		TRAO				
35		P6_5			CLK1			
36		P6_4						
37		P6_3						
38		P0_7						AN0
41		P0_6						AN1
42		P0_5						AN2
43		P0_4						AN3
44	VREF	P4_2						
45		P6_0		TREO				
46		P6_2						
47		P6_1						
48		P0_3						AN4
49		P0_2						AN5
50		P0_1						AN6
51		P0_0						AN7
52		P3_7				SSO		

NOTE:
1. Can be assigned to the pin in parentheses by a program.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b[6]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 00100000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[5]	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register[2]	VW0C	0000X000b[3] 0100X001b[4]
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset or the LVD0ON bit in the OFS register is set to 0, and hardware reset.
5. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.3 SFR Information (3)[1]

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H / IIC bus Control Register 1[2]	SSCRH / ICCR1	00h
00B9h	SS Control Register L / IIC bus Control Register 2[2]	SSCRL / ICCR2	01111101b
00BAh	SS Mode Register / IIC bus Mode Register[2]	SSMR / ICMR	00011000b
00BBh	SS Enable Register / IIC bus Interrupt Enable Register[2]	SSER / ICIER	00h
00BCh	SS Status Register / IIC bus Status Register[2]	SSSR / ICSR	00h / 0000X000b
00BDh	SS Mode Register 2 / Slave Address Register[2]	SSMR2 / SAR	00h
00BEh	SS Transmit Data Register / IIC bus Transmit Data Register[2]	SSTDR / ICDRT	FFh
00BFh	SS Receive Data Register / IIC bus Receive Data Register[2]	SSRDR / ICDRR	FFh

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P2 Drive Capacity Control Register	P2DRR	00h
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)[1]

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		-20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

NOTES:
1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

Table 5.16 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA

Table 5.17 Electrical Characteristics (3) [Vcc = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V_{SS}	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4.0	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.2	–	µA
		Increase during A/D converter operation	Without sample & hold	–	2.6	–	mA
			With sample & hold	–	1.6	–	mA
		Stop mode	XIN clock off, T_{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	µA
			XIN clock off, T_{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	µA

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.18 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

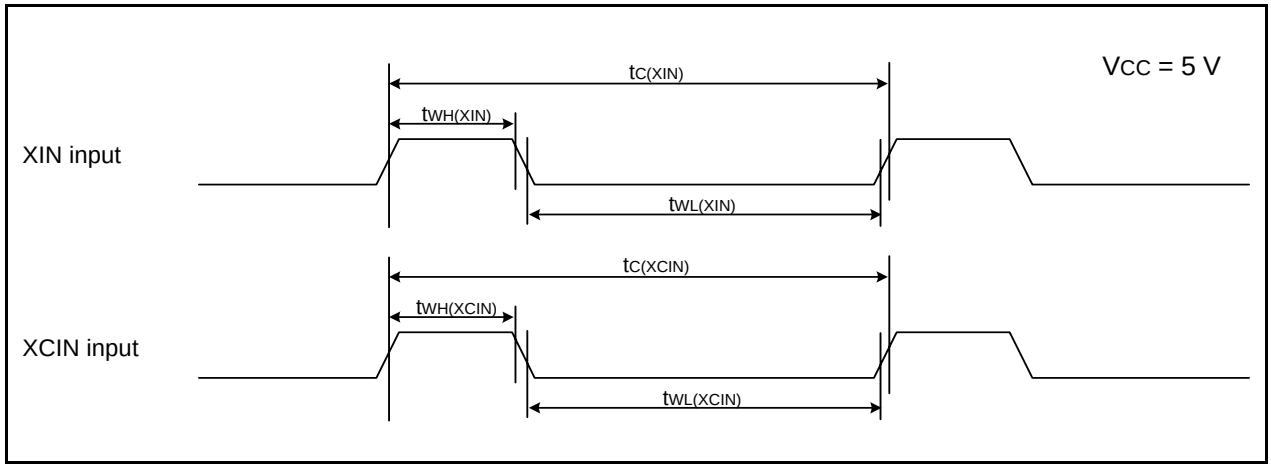

Figure 5.8 XIN Input and XCIN Input Timing Diagram when Vcc = 5 V

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

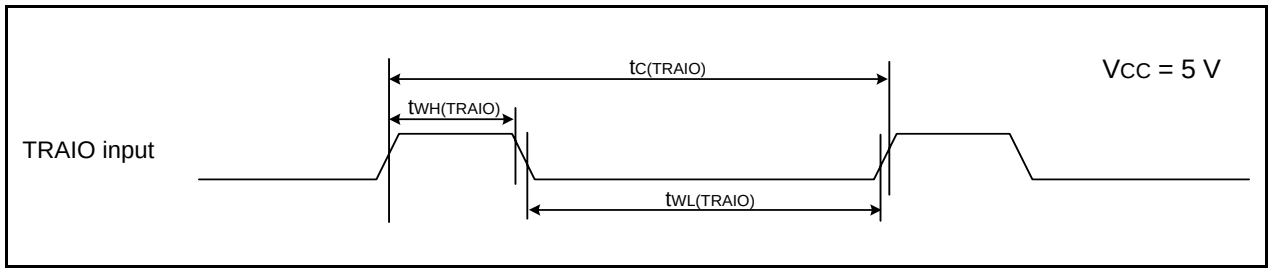

Figure 5.9 TRAIO Input Timing Diagram when Vcc = 5 V

Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at Topr = 25°C) [V_{CC} = 3 V]

Table 5.24 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

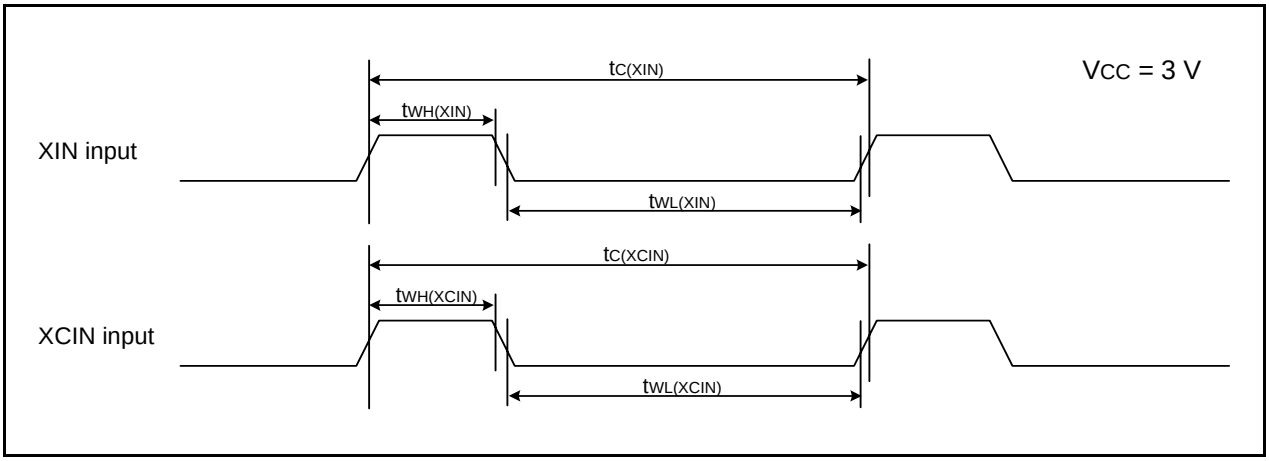

Figure 5.12 XIN Input and XCIN Input Timing Diagram when V_{CC} = 3 V

Table 5.25 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

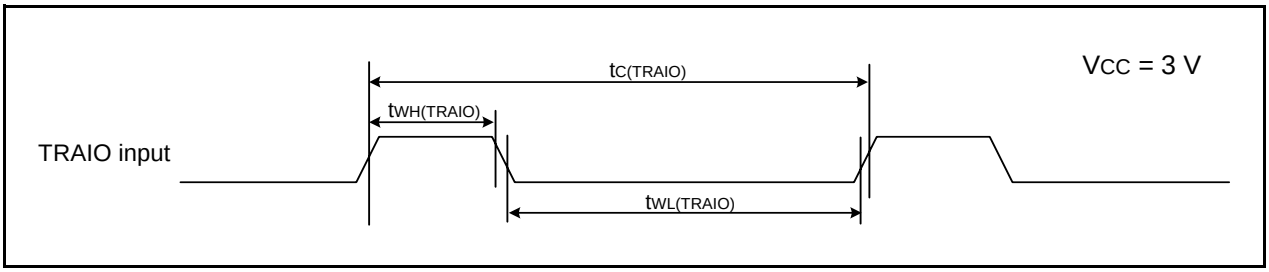

Figure 5.13 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

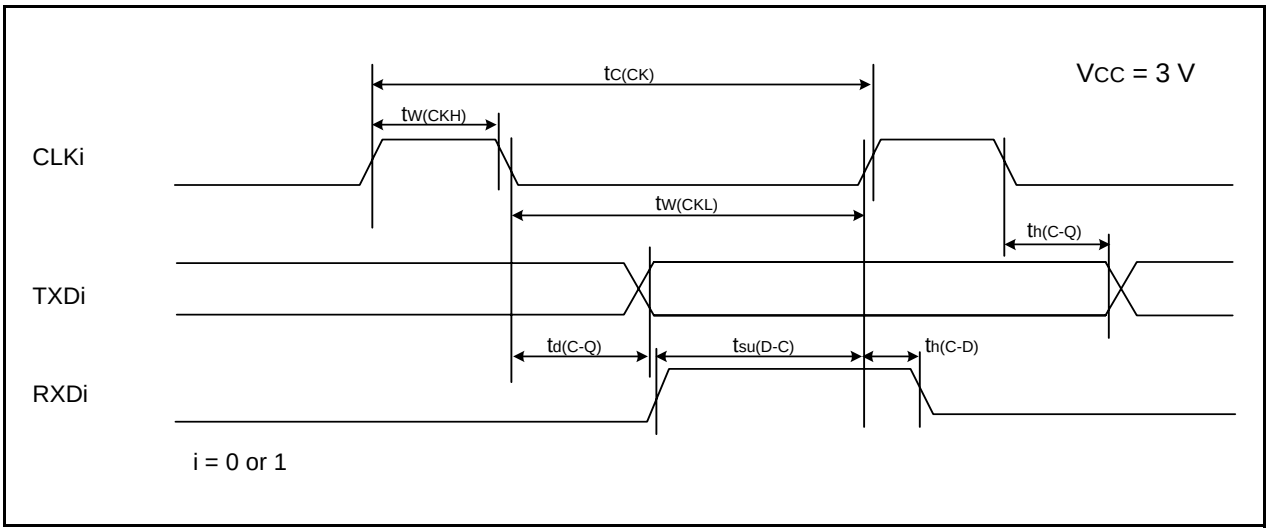

Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

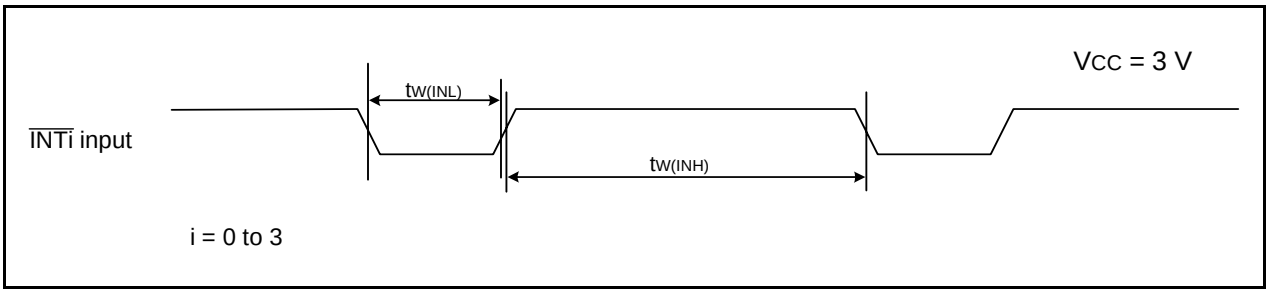

Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V

Table 5.28 Electrical Characteristics (5) [Vcc = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -1 mA		Vcc - 0.5	–	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -2 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -1 mA	Vcc - 0.5	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -50 µA	Vcc - 0.5	–	Vcc	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 2 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.05	0.3	–	V
		$\overline{RESET}$			0.05	0.15	–	V
I_{IH}	Input “H” current		VI = 2.2 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V		100	200	600	kΩ
R_{fXIN}	Feedback resistance	XIN			–	5	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	35	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Feb 24, 2005	1 to 3 5, 6	Pin type changed: 48-pin(under consideration) → 52-pin.
		5 to 7	Package type revised: 48-pin LQFP(under consideration) → PLQP0052JA-A
		8	Table 1.5 TCLK added, VREF revised.
		9	Table 1.6 revised.
		13, 14	Figures 3.1 and 3.2 part number revised.
		15	Tabel 4.1 revised: - 000Fh: 000XXXXXb → 00011111b - 0023h: FR0 → FRA0 - 0024h: FR1 → FRA1 - 0025h: FR2 → FRA2 - 0031h: Voltage Detection A Register 1, VC1 → Voltage Detection Register 1, VCA1 - 0032h: Voltage Detection A Register 2, VC2 → Voltage Detection Register 2, VCA2
		17	Tabel 4.3 Register name and the value after reset at 00B8h to 00BFh revised; NOTE2 added.
		19	Tabel 4.5 revised: - 0107h: LINSR → LINST - 0137h to 013Fh: Register symbol revised
		20	Tabel 4.6 revised: - 0140h to 015Fh: Register symbol revised - 0158h, 0159h: Timer RD General Register → Timer RD General Register A1
0.20	Mar 8, 2005	2, 3 8	Tables 1.1, 1.2 and 1.5 revised: “main clock” → “XIN clock”; “sub clock” → “XCIN clock”
		15	- 0023h to 0025h: 40MHz On-Chip Oscillator Control Register → High-Speed On-Chip Oscillator Control Register
0.30	Sep 01, 2005	2, 3	Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance • Serial Interface revised: - Serial Interface: 2 channels Clock synchronous serial I/O, UART - Clock Synchronous Serial Interface: 1 channel I^2C bus Interface(1), Clock synchronous serial I/O with chip select
		4	Figure 1.1 Block Diagram • UART or Clock Synchronous Serial Interface: “(8 bits × 1 channel)” → “(8 bits × 2 channels)” revised • UART (8 bits × 1 channel) deleted
		5, 6	Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group “Flash Memory Version” → “N Version” revised

Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	19	Tabel 4.5 SFR Information(5) revised: • 0118h : Timer RE Second Data Register/Counter Register → Timer RE Second Data Register/Counter Data Register
		20	Tabel 4.6 SFR Information(6) revised: • 0145h POCR0 → TRDPOCR0 • 0146h, 0147h TRDCNT0 → TRD0 • 0148h, 0149h GRA0 → TRDGRA0 • 014Ah, 014Bh GRB0 → TRDGRB0 • 014Ch, 014Dh GRC0 → TRDGRC0 • 014Eh, 014Fh GRD0 → TRDGRD0 • 0155h POCR1 → TRDPOCR1 • 0156h, 0157h TRDCNT1 → TRD1 • 0158h, 0159h GRA1 → TRDGRA1 • 015Ah, 015Bh GRB1 → TRDGRB1 • 015Ch, 015Dh GRC1 → TRDGRC1 • 015Eh, 015Fh GRD1 → TRDGRD1
		21	Tabel 4.7 SFR Information(7) revised: • 01B5h: 01000101b → 1000000Xb • 01B7h: XX000001b → 00000001b • FFFFh: (Note 2) added
		22 to 44	5. Electrical Characteristics added
0.40	Jan 24, 2006	all pages	• “Preliminary” deleted • Symbol name “TRDMDR” → “TRDMR”, “SSUAIC” → “SSUIC”, and “IIC2AIC” → “IICIC” revised • Pin name “TCLK” → “TRDCLK” revised
		2	Table 1.1 Functions and Specifications for R8C/24 Group revised
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; “Peripheral Functions” added, “System Clock Generation” → “System Clock Generator” revised
		5	Table 1.3 Product Information for R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group revised
		7	Figure 1.4 Pin Assignments (Top View) “TCLK” → “TRDCLK” revised
		8	Table 1.5 Pin Functions “TCLK” → “TRDCLK” revised
		9	Table 1.6 Pin Name Information by Pin Number; “TCLK” → “TRDCLK” revised
		10	Figure 2.1 CPU Registers; “Reserved Area” → “Reserved Bit” revised
		12	2.8.10 Reserved Area; “Reserved Area” → “Reserved bit” revised
		13	Figure 3.1 Memory Map of R8C/24 Group; “Program area” → “program ROM” revised
		14	3.2 R8C/25 Group, Figure 3.2 Memory Map of R8C/25 Group; “Data area” → “data flash”, “Program area” → “program ROM” revised

Rev.	Date	Description	
		Page	Summary
0.40	Jan 24, 2006	15	Table 4.1 SFR Information(1); 0024h: "TBD" → "When shipping" NOTES 3 and 4 revised
		19	Table 4.5 SFR Information (5); 0118h: "Timer RE Second Data Register" → "Timer RE Second Data Register / Counter Data Register" 0119h: "Timer RE Minute Data Register" → "Timer RE Minute Data Register / Compare Data Register" 0138h: "TRDMDR" → "TRDMR" 013Bh: "Timer RD Output Master Enable Register" → "Timer RD Output Master Enable Register 1"
		22	Table 5.1 Absolute Maximum Ratings; "VCC" → "VCC/AVCC" revised Table 5.2 Recommended Operating Conditions revised
		23	Table 5.3 A/D Converter Characteristics revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics revised
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical revised
		26	Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics revised Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics revised Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics revised
		28	Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.13 Power Supply Circuit Timing Characteristics revised
		29	Table 5.14 Timing Requirements of Clock Synchronous Serial I/O with Chip Select revised
		33	Table 5.15 Timing Requirements of I^2C bus Interface NOTE1 revised
		34	Table 5.16 Electrical Characteristics (1) [VCC = 5 V] revised
		35	Table 5.17 Electrical Characteristics (2) [VCC = 5 V] revised
		36	Table 5.18 XIN Input, XCIN Input revised
		37	Table 5.20 Serial Interface revised
		38	Table 5.22 Electrical Characteristics (3) [VCC = 3 V] revised
		39	Table 5.23 Electrical Characteristics (4) [Vcc = 3 V] revised
		40	Table 5.24 XIN Input, XCIN Input revised
		41	Table 5.26 Serial Interface revised
		42	Table 5.28 Electrical Characteristics (5) [VCC = 2.2 V] revised
		43	Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V] revised
		44	Table 5.30 XIN Input, XCIN Input revised Table 5.31 TRAIO Input, $\overline{INT1}$ Input revised
		45	Table 5.32 Serial Interface revised Table 5.33 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Jul 14, 2006	all pages	“PTLG0064JA-A (64F0G)” package added
		1	1. Overview; “... or a 64-pin molded-plastic FLGA.“ added
		2, 3	Table 1.1 Functions and Specifications for R8C/24 Group, Table 1.2 Functions and Specifications for R8C/25 Group; Package: “64-pin molded-plastic FLGA” added
		5	Table 1.3 Product Information for R8C/24 Group, Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group, Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group revised
		7	Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View); NOTE3 revised
		8	Figure 1.5 PTLG0064JA-A Package Pin Assignments added
		14	Figure 3.1 Memory Map of R8C/24 Group revised
		15	Figure 3.2 Memory Map of R8C/25 Group revised
		23	Table 5.1 Absolute Maximum Ratings; NOTE1 added
		47	Package Dimensions; “PTLG0064JA-A (64F0G)” added
3.00	Feb 29, 2008	all pages	Y version added Factory programming product added
		2, 3	Table 1.1, Table 1.2 Clock; “Real-time clock (timer RE)” added
		5, 7	Table 1.3, Table 1.4 revised
		6, 8	Figure 1.2, Figure 1.3; ROM number “XXX” added
		16, 17	Figure 3.1, Figure 3.2; “Expanded area” deleted
		18	Table 4.1 revised
		26	Table 5.2 NOTE2 revised
		32	Table 5.10; revised, NOTE4 added Table 5.11; Oscillation stability time: Condition “V_{CC} = 5.0 V, Topr = 25°C” deleted
		38	Table 5.15; I_{IH}, I_{IL}, R_{PULLUP} Condition: “Vcc = 5V” added
		39	Table 5.16; Condition: High-speed on-chip oscillator mode revised
		40	Table 5.17 added
		41	Figure 5.8 revised
		43	Table 5.22; I_{IH}, I_{IL}, R_{PULLUP} Condition: “Vcc = 3V” added
		44	Table 5.23; Condition “Increase during A/D converter operation” added
		45	Figure 5.12 revised
		48	Table 5.29; Condition “Increase during A/D converter operation” added
		49	Figure 5.16 revised

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