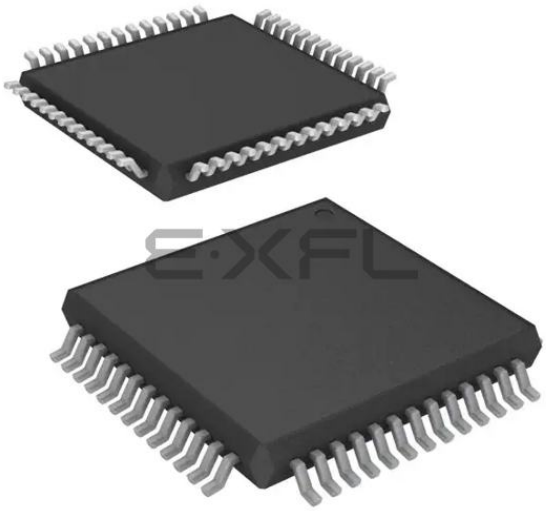

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21257syfp-v2

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1.4 Product Information

Table 1.3 lists the Product Information for R8C/24 Group and Table 1.4 lists the Product Information for R8C/25 Group.

Table 1.3 Product Information for R8C/24 Group **Current of Feb. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21244SNFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21245SNFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	
R5F21244SDFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	D version Blank product
R5F21245SDFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Factory programming product(1)
R5F21245SNXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNXXXLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	
R5F21244SDXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	D version Factory programming product(1)
R5F21245SDXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	

NOTE:
1. The user ROM is programmed before shipment.

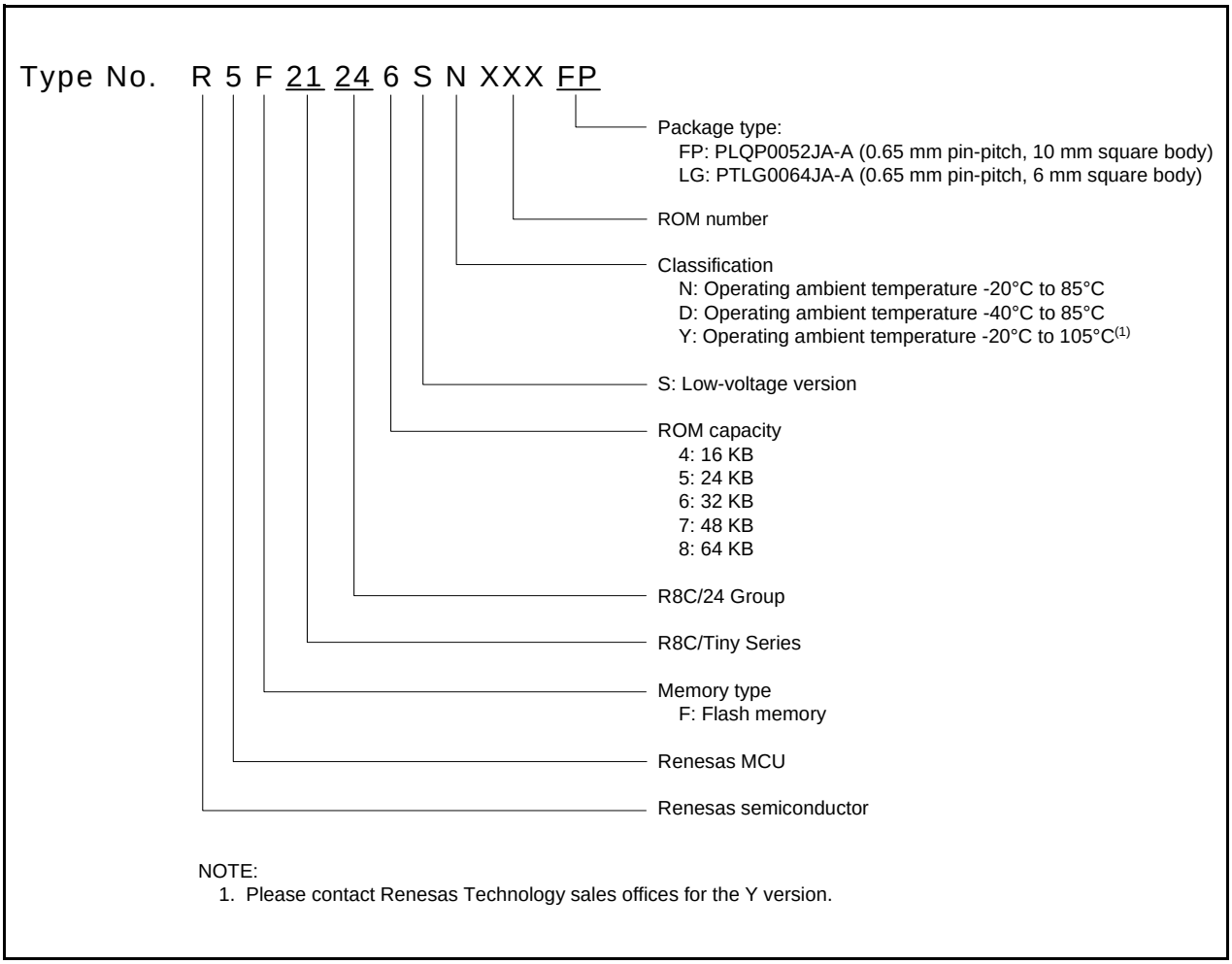


Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group

Table 1.4 Product Information for R8C/25 Group Current of Feb. 2008

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21254SNFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21255SNFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Blank product
R5F21255SDFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Factory programming product(1)
R5F21255SNXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNXXXLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Factory programming product(1)
R5F21255SDXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	

NOTE:
1. The user ROM is programmed before shipment.

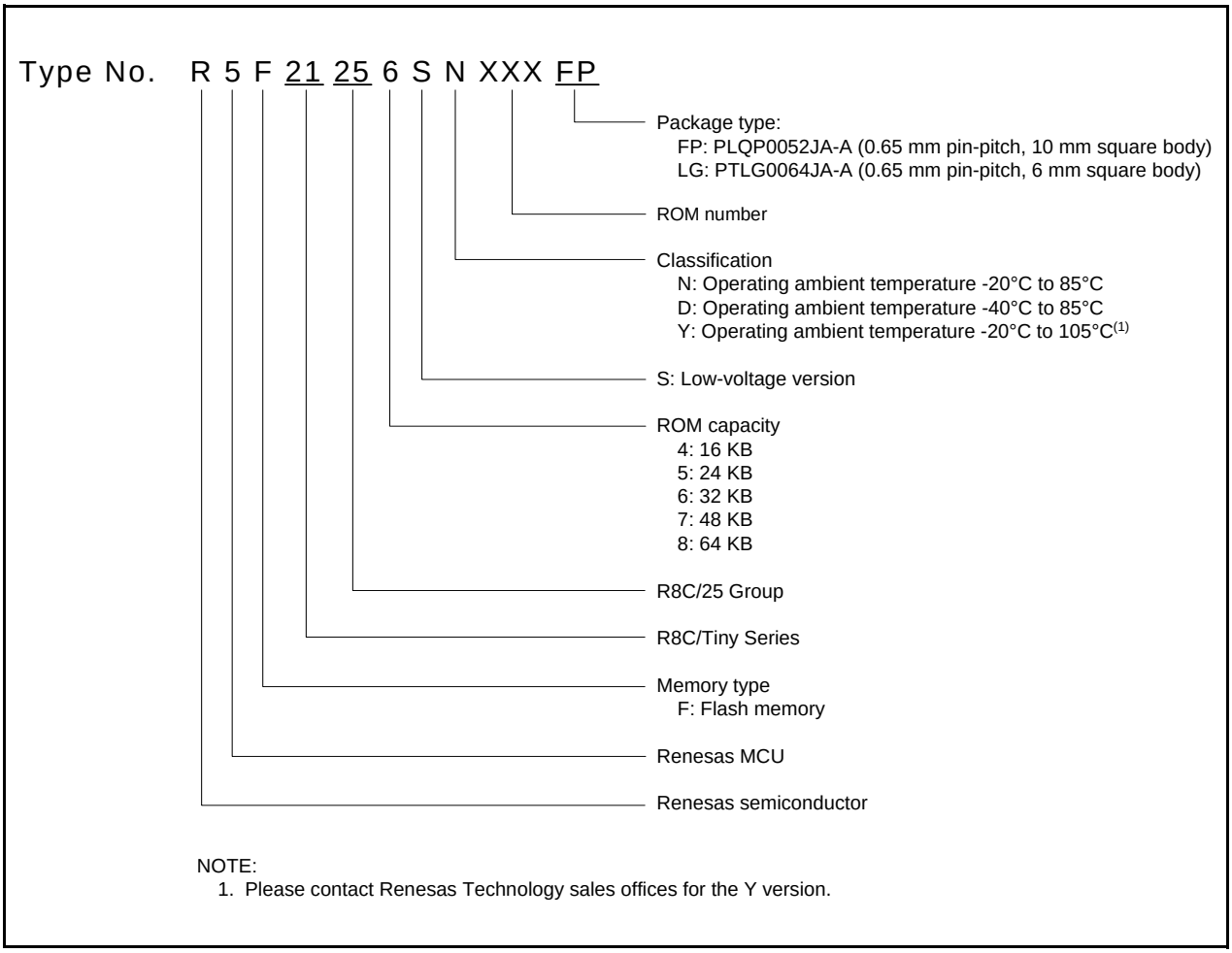
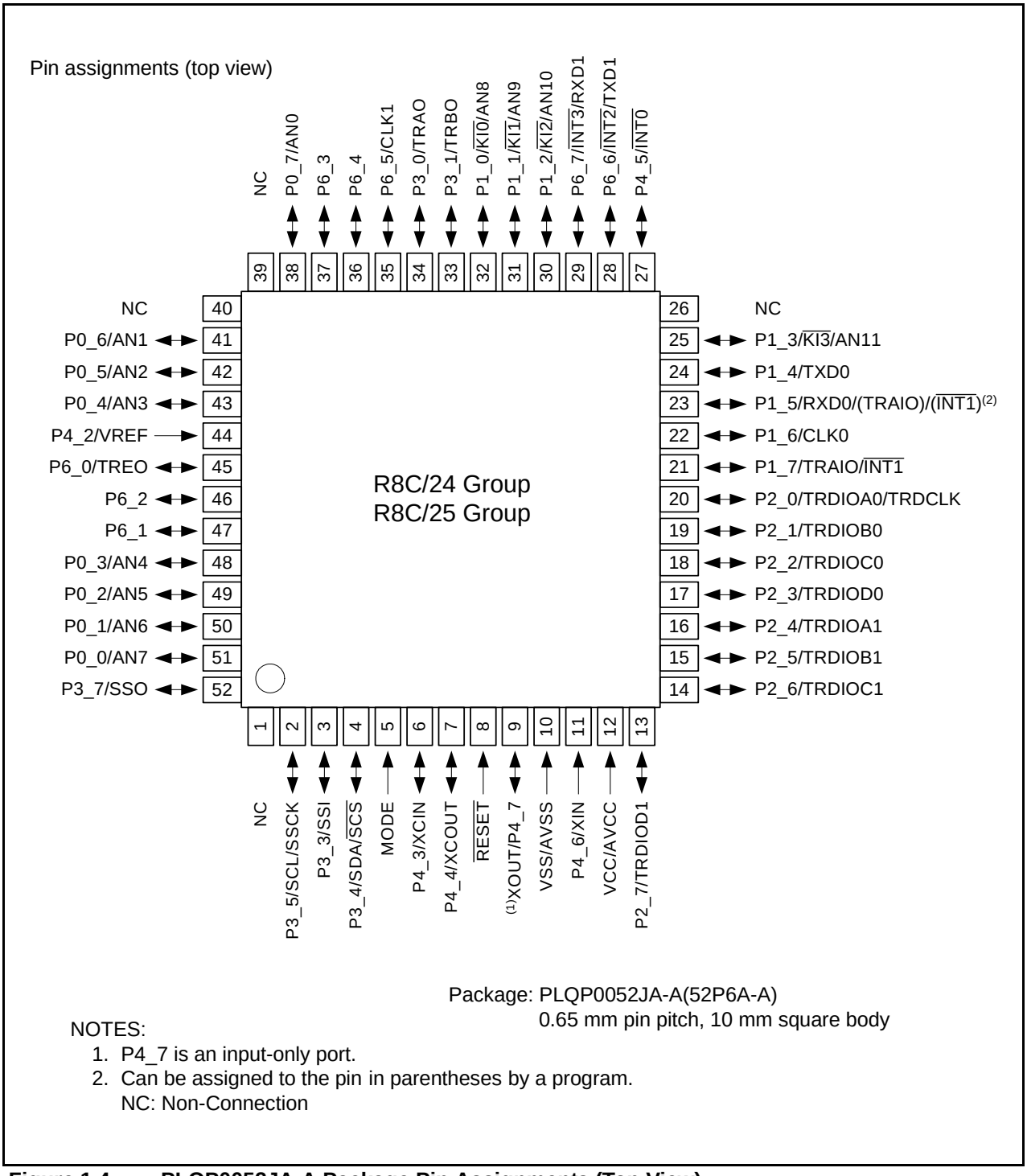


Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group

1.5 Pin Assignments

Figure 1.4 shows PLQP0052JA-A Package Pin Assignments (Top View). Figure 1.5 shows PTLG0064JA-A Package Pin Assignments.



Package: PLQP0052JA-A(52P6A-A)
0.65 mm pin pitch, 10 mm square body

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
   NC: Non-Connection

Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View)

1.6 Pin Functions

Table 1.5 lists Pin Functions.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins. To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RD input pin. $\overline{\text{INT1}}$ is timer RA input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O ports
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Serial interface	CLK0, CLK1	I/O	Transfer clock I/O pin
	RXD0, RXD1	I	Serial data input pins
	TXD0, TXD1	O	Serial data output pins
I^2C bus interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Clock synchronous serial I/O with chip select	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6_0 to P6_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

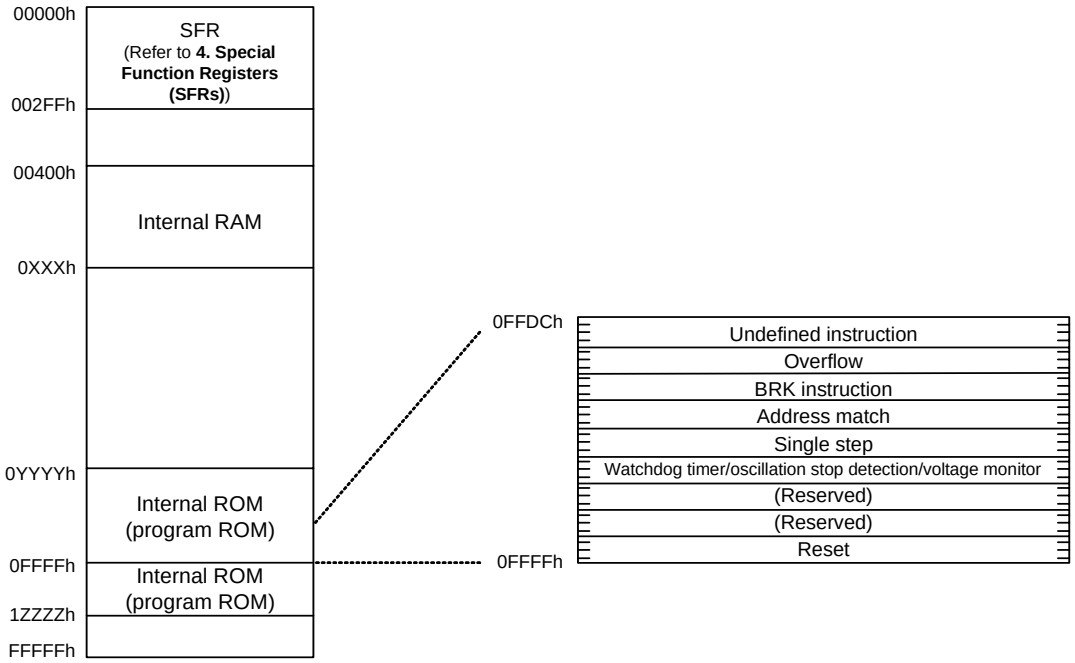
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/24 Group

Figure 3.1 is a Memory Map of R8C/24 Group. The R8C/24 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM area is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



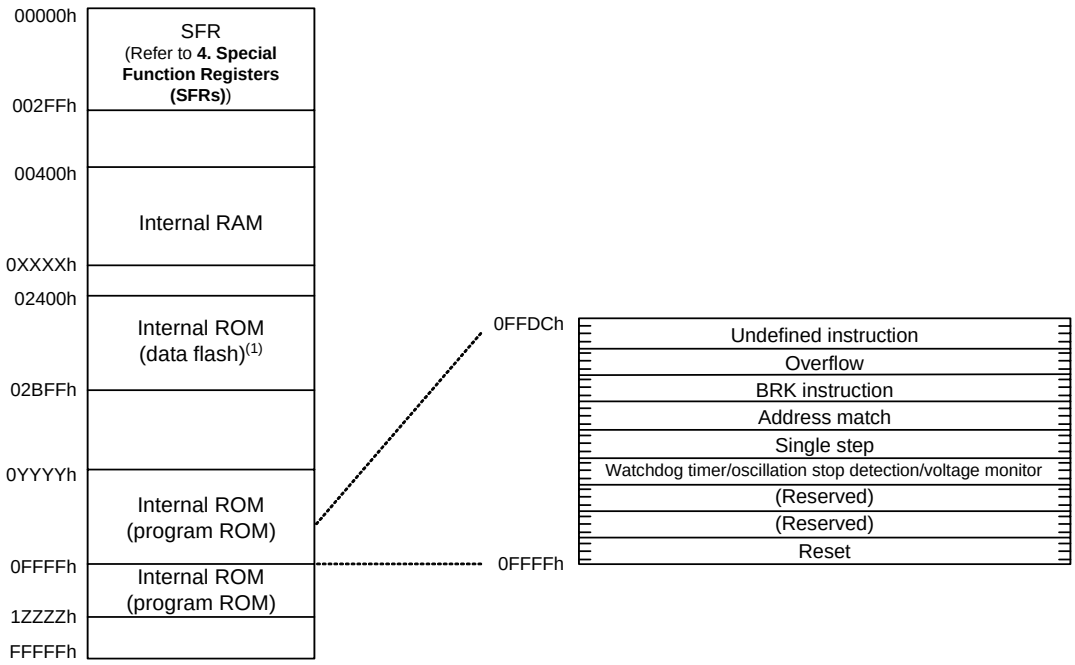
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address 1ZZZZh	Size	Address 0XXXXh
R5F21244SNFP, R5F21244SNXXXFP, R5F21244SDFP, R5F21244SDXXXFP, R5F21244SNLG, R5F21244SNXXXLG	16 Kbytes	0C000h	–	1 Kbyte	007FFh
R5F21245SNFP, R5F21245SNXXXFP, R5F21245SDFP, R5F21245SDXXXFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21246SNFP, R5F21246SNXXXFP, R5F21246SDFP, R5F21246SDXXXFP, R5F21246SNLG, R5F21246SNXXXLG	32 Kbytes	08000h	–	2 Kbytes	00BFFh
R5F21247SNFP, R5F21247SNXXXFP, R5F21247SDFP, R5F21247SDXXXFP	48 Kbytes	04000h	–	2.5 Kbytes	00DFFh
R5F21248SNFP, R5F21248SNXXXFP, R5F21248SDFP, R5F21248SDXXXFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh

Figure 3.1 Memory Map of R8C/24 Group

3.2 R8C/25 Group

Figure 3.2 is a Memory Map of R8C/25 Group. The R8C/25 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address 1ZZZZh	Size	Address 0XXXXh
R5F21254SNFP, R5F21254SNXXXFP, R5F21254SDFP, R5F21254SDXXXFP, R5F21254SNLG, R5F21254SNXXXLG	16 Kbytes	0C000h	–	1 Kbyte	007FFh
R5F21255SNFP, R5F21255SNXXXFP, R5F21255SDFP, R5F21255SDXXXFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21256SNFP, R5F21256SNXXXFP, R5F21256SDFP, R5F21256SDXXXFP, R5F21256SNLG, R5F21256SNXXXLG	32 Kbytes	08000h	–	2 Kbytes	00BFFh
R5F21257SNFP, R5F21257SNXXXFP, R5F21257SDFP, R5F21257SDXXXFP	48 Kbytes	04000h	–	2.5 Kbytes	00DFFh
R5F21258SNFP, R5F21258SNXXXFP, R5F21258SDFP, R5F21258SDXXXFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh

Figure 3.2 Memory Map of R8C/25 Group

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.2	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	-160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$		–	–	-80	mA
$I_{OH(peak)}$	Peak output “H” current	Except P2_0 to P2_7		–	–	-10	mA
		P2_0 to P2_7		–	–	-40	mA
$I_{OH(avg)}$	Average output “H” current	Except P2_0 to P2_7		–	–	-5	mA
		P2_0 to P2_7		–	–	-20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$		–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$		–	–	80	mA
$I_{OL(peak)}$	Peak output “L” current	Except P2_0 to P2_7		–	–	10	mA
		P2_0 to P2_7		–	–	40	mA
$I_{OL(avg)}$	Average output “L” current	Except P2_0 to P2_7		–	–	5	mA
		P2_0 to P2_7		–	–	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency		2.2 V ≤ V_{CC} ≤ 5.5 V	0	–	70	kHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V_{CC} ≤ 5.5 V	–	–	5	MHz

NOTES:
1. V_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		-20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at Topr = 25°C) [V_{CC} = 3 V]

Table 5.24 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

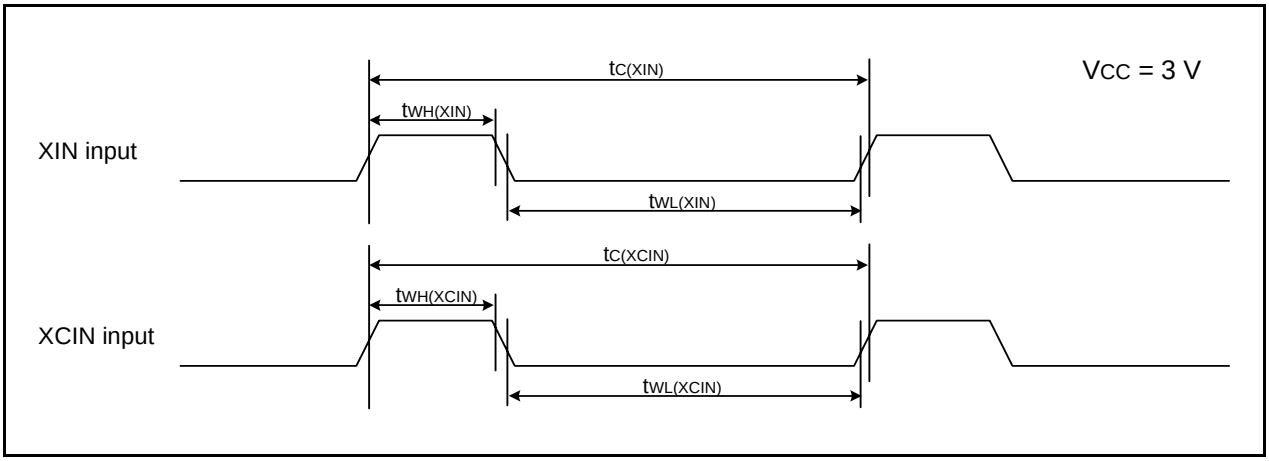


Figure 5.12 XIN Input and XCIN Input Timing Diagram when V_{CC} = 3 V

Table 5.25 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

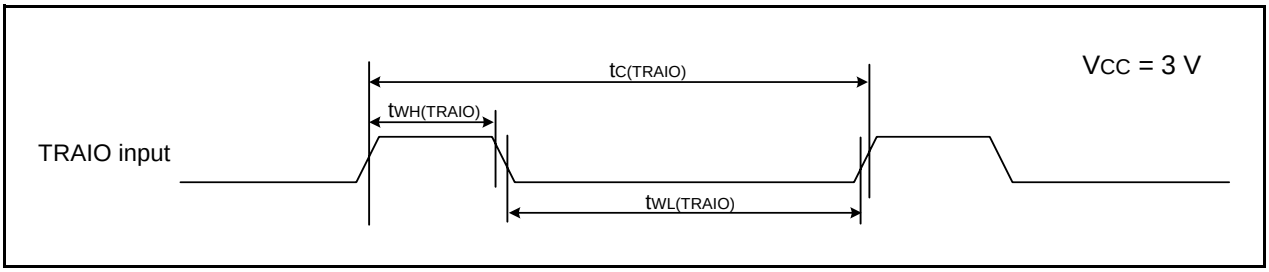


Figure 5.13 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

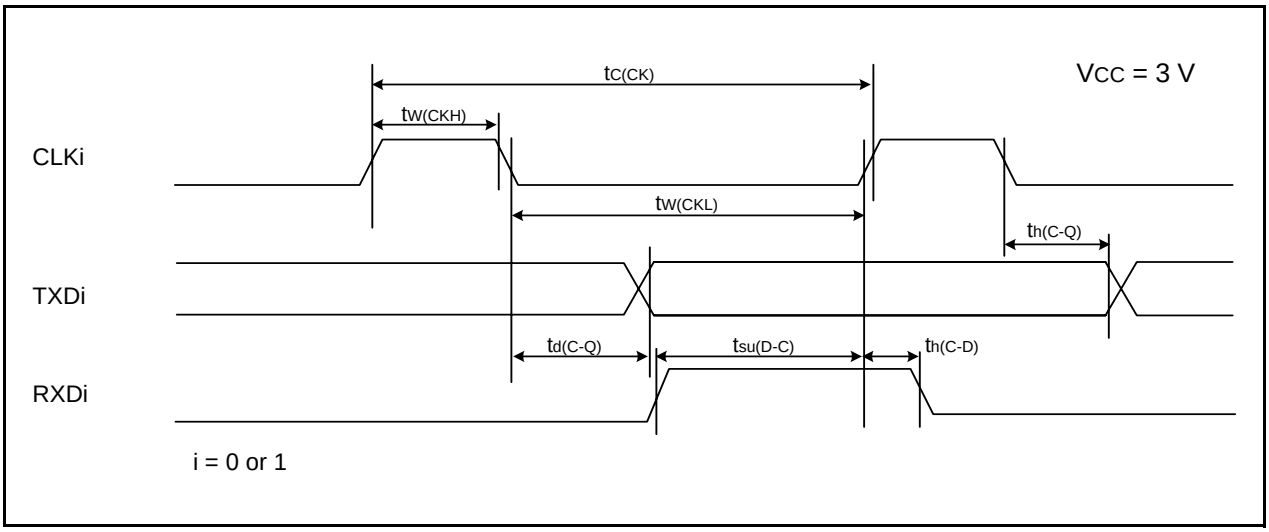


Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

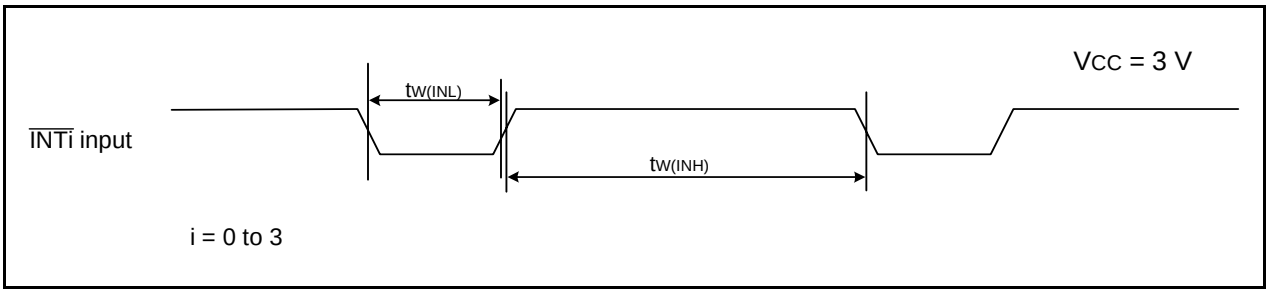


Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

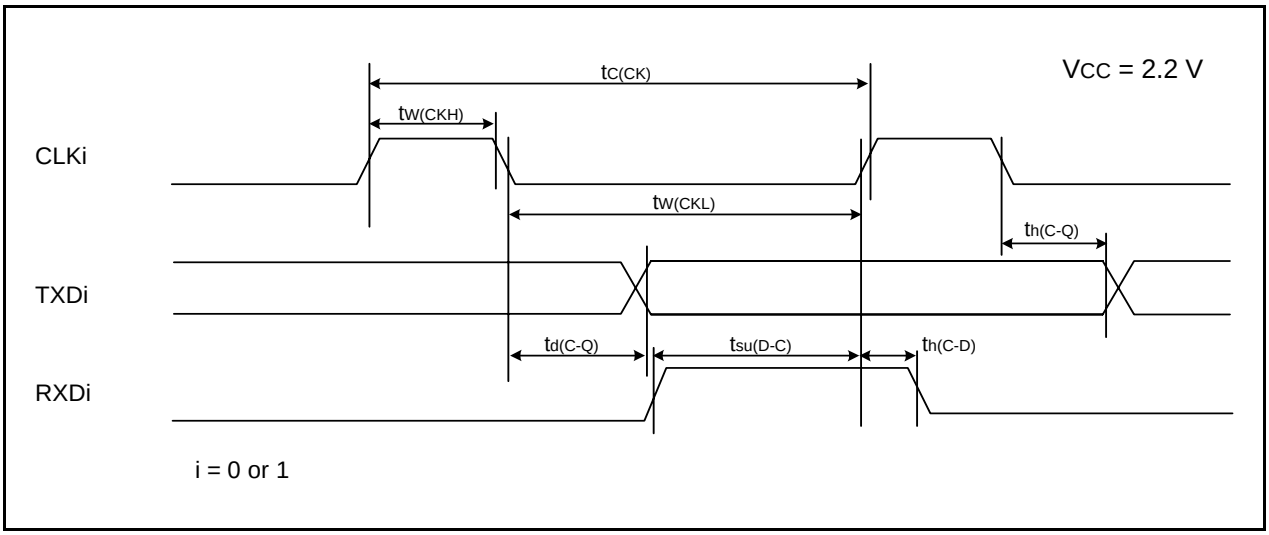


Figure 5.18 Serial Interface Timing Diagram when VCC = 2.2 V

Table 5.33 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	1000(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	1000(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

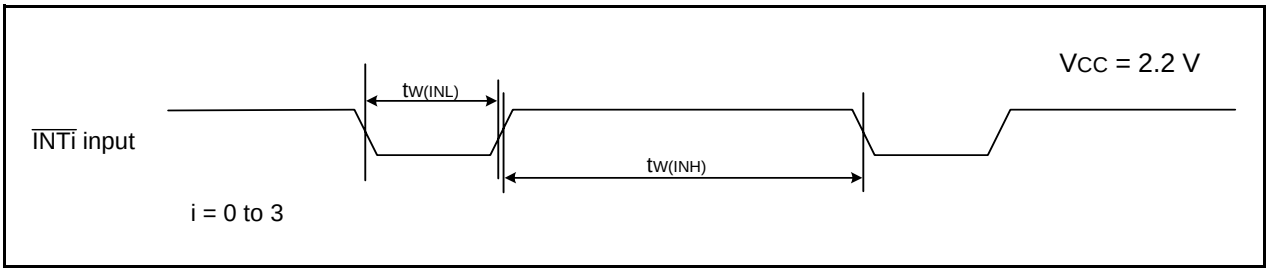


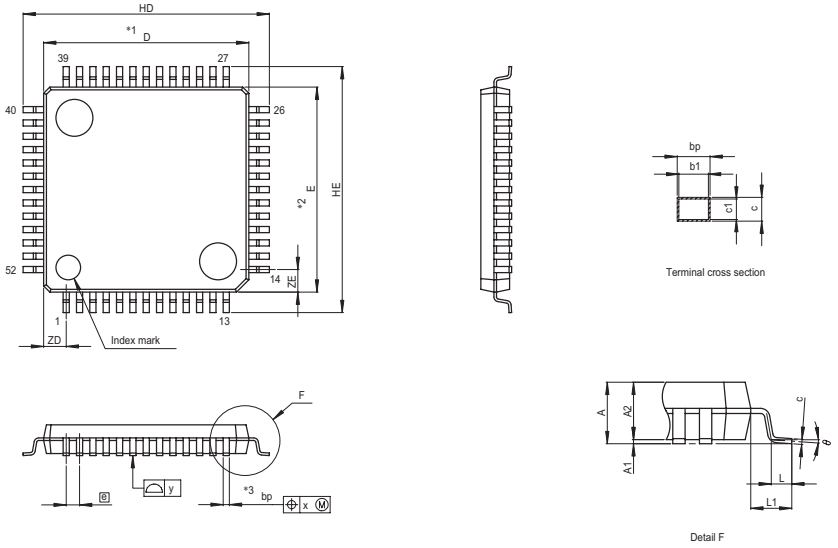
Figure 5.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 2.2 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g

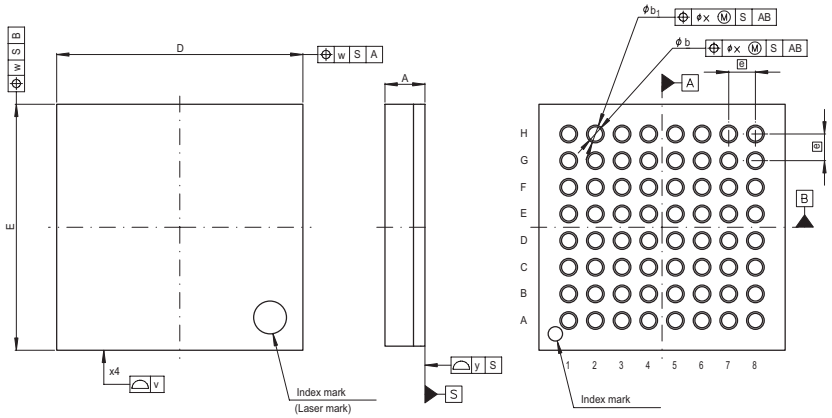
Under development



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	7	Figure 1.4 Pin Assignment • Pin name revised; VSS → VSS/AVSS, VCC → VCC/AVCC, P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$) → P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)(2), P6_6/$\overline{\text{INT2}}$/(TXD1) → P6_6/$\overline{\text{INT2}}$/TXD1, P6_7/$\overline{\text{INT3}}$/(RXD1) → P6_7/$\overline{\text{INT3}}$/RXD1, P6_5 → P6_5/CLK1 • NOTE2 added
		8	Table 1.5 Pin Description • Analog Power Supply Input: line added • $\overline{\text{INT}}$ Interrupt Input: "$\overline{\text{INT0}}$ Timer RD input pins. $\overline{\text{INT1}}$ Timer RA input pins." added • Serial Interface: "CLK1" added • "I2C Bus Interface (IIC)" → "I2C Bus Interface" • "SSU" → "Clock Synchronous Serial I/O with Chip Select"
		9	Table 1.6 Pin Name Information by Pin Number revised • Pin Number 10: "VSS" → "VSS/AVSS" • Pin Number 12: "$\overline{\text{VCC}}$" → "VCC/AVCC" • Pin Number 27: "$\overline{\text{INT0}}$" added • Pin Number 28: "(TXD1)" → "TXD1" • Pin Number 29: "(RXD1)" → "RXD1" • Pin Number 35: "CLK1" added
		15	Tabel 4.1 SFR Information(1) revised: • 0012h: X0h → 00h • 0013h: XXXXXX00b → 00h • 0016h: X0h → 00h • 0036h: Voltage Monitor 1 Control Register(2) → Voltage Monitor 1 Control Register(5) • 0038h: 00001000b(3), 01000001b(4) → 0000X000b(3), 0100X001b(4) • NOTES2, 5: "the voltage monitor 1 reset" added • NOTE3: "voltage monitor 1 reset" → "voltage monitor 0 reset"
		16	Tabel 4.2 SFR Information(2) revised: • 0048h: RD0IC → TRD0IC • 0049h: RD1IC → TRD1IC • 004Ah: REIC → TREIC • 004Fh: SSU/IIC Interrupt Control Register, IIC2AIC → SSU/IIC Interrupt Control Register(2), SSUAIC/IIC2AIC • 0056h: RAIC → TRAIC • 0058h: RBIC → TRBIC • NOTE2 added
		17	Tabel 4.3 SFR Information(3) revised: • 00BCh: 00h → 00h/0000X000b
		18	Tabel 4.4 SFR Information(4) revised: • 00D6h: 00000XXXb → 00h • 00F5h: UART1 Function Select Register, U1SR, XXh added

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

Colophon .7.2