



Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

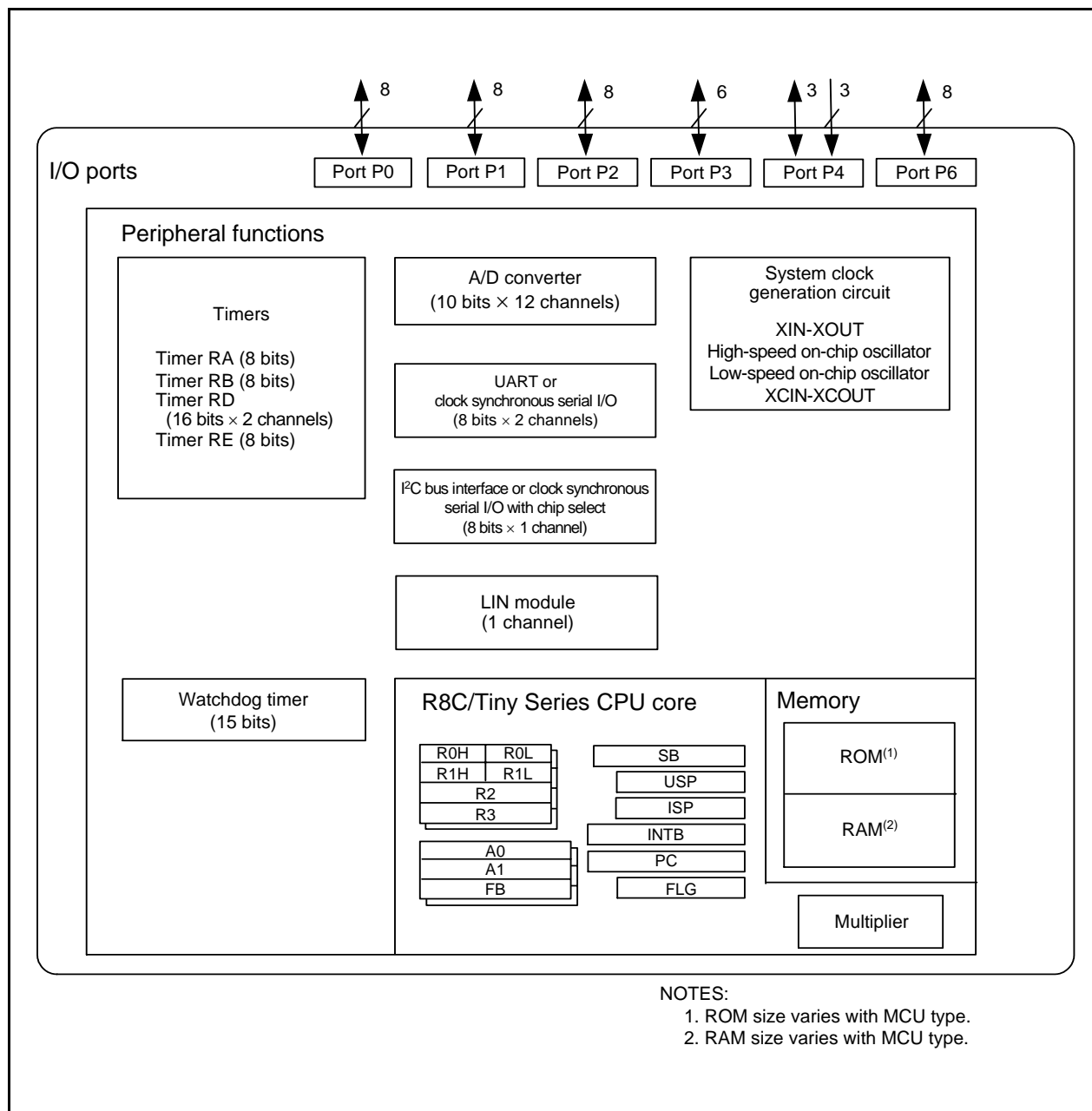
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21258snfp-v2">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21258snfp-v2</a>

### 1.3 Block Diagram

Figure 1.1 shows a Block Diagram.



**Figure 1.1** Block Diagram

## 1.5 Pin Assignments

Figure 1.4 shows PLQP0052JA-A Package Pin Assignments (Top View). Figure 1.5 shows PTLG0064JA-A Package Pin Assignments.

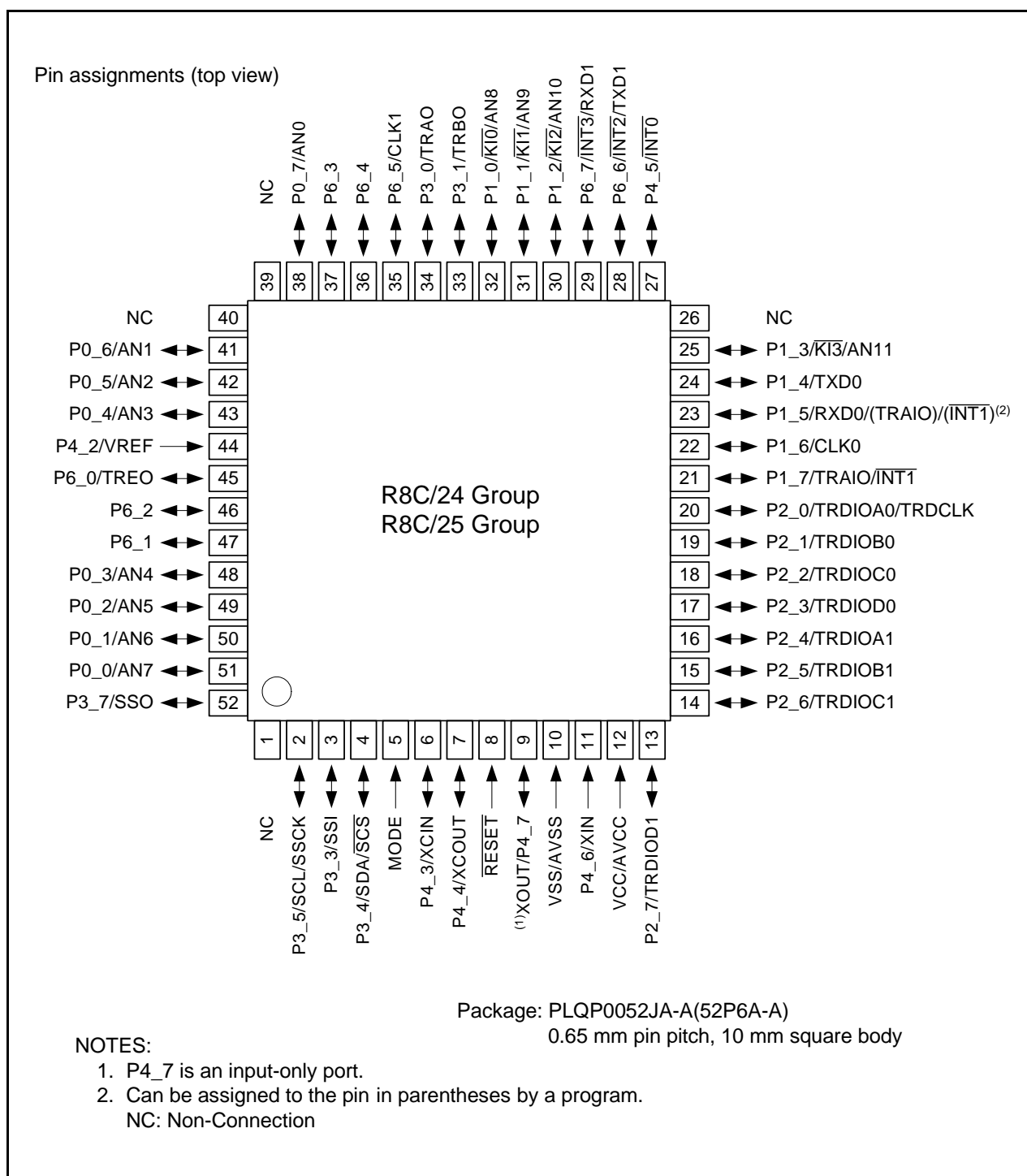


Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View)

## 1.6 Pin Functions

Table 1.5 lists Pin Functions.

**Table 1.5 Pin Functions**

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins. To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RD input pin. $\overline{\text{INT1}}$ is timer RA input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O ports
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Serial interface	CLK0, CLK1	I/O	Transfer clock I/O pin
	RXD0, RXD1	I	Serial data input pins
	TXD0, TXD1	O	Serial data output pins
I <sup>2</sup> C bus interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Clock synchronous serial I/O with chip select	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6_0 to P6_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input      O: Output      I/O: Input and output

**Table 1.6 Pin Name Information by Pin Number**

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I <sup>2</sup> C bus Interface	A/D Converter
2		P3_5				SSCK	SCL	
3		P3_3				SSI		
4		P3_4				SCS	SDA	
5	MODE							
6	XCIN	P4_3						
7	XCOUT	P4_4						
8	RESET							
9	XOUT	P4_7						
10	VSS/AVSS							
11	XIN	P4_6						
12	VCC/AVCC							
13		P2_7		TRDIOD1				
14		P2_6		TRDIOC1				
15		P2_5		TRDIOB1				
16		P2_4		TRDIOA1				
17		P2_3		TRDIOD0				
18		P2_2		TRDIOC0				
19		P2_1		TRDIOB0				
20		P2_0		TRDIOA0/TRDCLK				
21		P1_7	INT1	TRAIO				
22		P1_6			CLK0			
23		P1_5	(INT1) <sup>(1)</sup>	(TRAIO) <sup>(1)</sup>	RXD0			
24		P1_4			TXD0			
25		P1_3	KI3					AN11
27		P4_5	INT0	INT0				
28		P6_6	INT2		TXD1			
29		P6_7	INT3		RXD1			
30		P1_2	KI2					AN10
31		P1_1	KI1					AN9
32		P1_0	KI0					AN8
33		P3_1		TRBO				
34		P3_0		TRA0				
35		P6_5			CLK1			
36		P6_4						
37		P6_3						
38		P0_7						AN0
41		P0_6						AN1
42		P0_5						AN2
43		P0_4						AN3
44	VREF	P4_2						
45		P6_0		TREO				
46		P6_2						
47		P6_1						
48		P0_3						AN4
49		P0_2						AN5
50		P0_1						AN6
51		P0_0						AN7
52		P3_7				SSO		

NOTE:

1. Can be assigned to the pin in parentheses by a program.

**Table 5.2 Recommended Operating Conditions**

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V <sub>CC</sub> /AV <sub>CC</sub>	Supply voltage			2.2	—	5.5	V
V <sub>SS</sub> /AV <sub>SS</sub>	Supply voltage			—	0	—	V
V <sub>IH</sub>	Input "H" voltage			0.8 V <sub>CC</sub>	—	V <sub>CC</sub>	V
V <sub>IL</sub>	Input "L" voltage			0	—	0.2 V <sub>CC</sub>	V
I <sub>OH</sub> (sum)	Peak sum output "H" current	Sum of all pins I <sub>OH</sub> (peak)		—	—	-160	mA
I <sub>OH</sub> (sum)	Average sum output "H" current	Sum of all pins I <sub>OH</sub> (avg)		—	—	-80	mA
I <sub>OH</sub> (peak)	Peak output "H" current	Except P2_0 to P2_7		—	—	-10	mA
		P2_0 to P2_7		—	—	-40	mA
I <sub>OH</sub> (avg)	Average output "H" current	Except P2_0 to P2_7		—	—	-5	mA
		P2_0 to P2_7		—	—	-20	mA
I <sub>OL</sub> (sum)	Peak sum output "L" current	Sum of all pins I <sub>OL</sub> (peak)		—	—	160	mA
I <sub>OL</sub> (sum)	Average sum output "L" current	Sum of all pins I <sub>OL</sub> (avg)		—	—	80	mA
I <sub>OL</sub> (peak)	Peak output "L" current	Except P2_0 to P2_7		—	—	10	mA
		P2_0 to P2_7		—	—	40	mA
I <sub>OL</sub> (avg)	Average output "L" current	Except P2_0 to P2_7		—	—	5	mA
		P2_0 to P2_7		—	—	20	mA
f(XIN)	XIN clock input oscillation frequency		3.0 V ≤ V <sub>CC</sub> ≤ 5.5 V	0	—	20	MHz
			2.7 V ≤ V <sub>CC</sub> < 3.0 V	0	—	10	MHz
			2.2 V ≤ V <sub>CC</sub> < 2.7 V	0	—	5	MHz
f(XCIN)	XCIN clock input oscillation frequency		2.2 V ≤ V <sub>CC</sub> ≤ 5.5 V	0	—	70	kHz
—	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V <sub>CC</sub> ≤ 5.5 V	0	—	20	MHz
			2.7 V ≤ V <sub>CC</sub> < 3.0 V	0	—	10	MHz
			2.2 V ≤ V <sub>CC</sub> < 2.7 V	0	—	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	—	125	—	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V <sub>CC</sub> ≤ 5.5 V	—	—	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V	—	—	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V <sub>CC</sub> ≤ 5.5 V	—	—	5	MHz

## NOTES:

1. V<sub>CC</sub> = 2.2 to 5.5 V at T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

**Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	VCC = 4.75 to 5.25 V 0°C ≤ Topr ≤ 60°C <sup>(2)</sup>	39.2	40	40.8	MHz
		VCC = 4.5 to 5.5 V -20°C ≤ Topr ≤ 85°C	38.8	40	40.8	MHz
		VCC = 4.5 to 5.5 V -40°C ≤ Topr ≤ 85°C	38.4	40	40.8	MHz
		VCC = 3.0 to 5.5 V -20°C ≤ Topr ≤ 85°C <sup>(2)</sup>	38.8	40	41.2	MHz
		VCC = 3.0 to 5.5 V -40°C ≤ Topr ≤ 85°C <sup>(2)</sup>	38.4	40	41.6	MHz
		VCC = 2.7 to 5.5 V -20°C ≤ Topr ≤ 85°C <sup>(2)</sup>	38	40	42	MHz
		VCC = 2.7 to 5.5 V -40°C ≤ Topr ≤ 85°C <sup>(2)</sup>	37.6	40	42.4	MHz
		VCC = 2.2 to 5.5 V -20°C ≤ Topr ≤ 85°C <sup>(3)</sup>	35.2	40	44.8	MHz
		VCC = 2.2 to 5.5 V -40°C ≤ Topr ≤ 85°C <sup>(3)</sup>	34	40	46	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register <sup>(4)</sup>	VCC = 5.0 V, Topr = 25°C	—	36.864	—	MHz
		VCC = 3.0 to 5.5 V -20°C ≤ Topr ≤ 85°C	-3%	—	3%	%
—	Value in FRA1 register after reset		08h	—	F7h	—
—	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	—	+0.3	—	MHz
—	Oscillation stability time		—	10	100	μs
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	—	400	—	μA

NOTES:

1. VCC = 2.2 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Standard values when the FRA1 register value after reset is assumed.
3. Standard values when the corrected value of the FRA6 register has been written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

**Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
—	Oscillation stability time		—	10	100	μs
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	—	15	—	μA

NOTE:

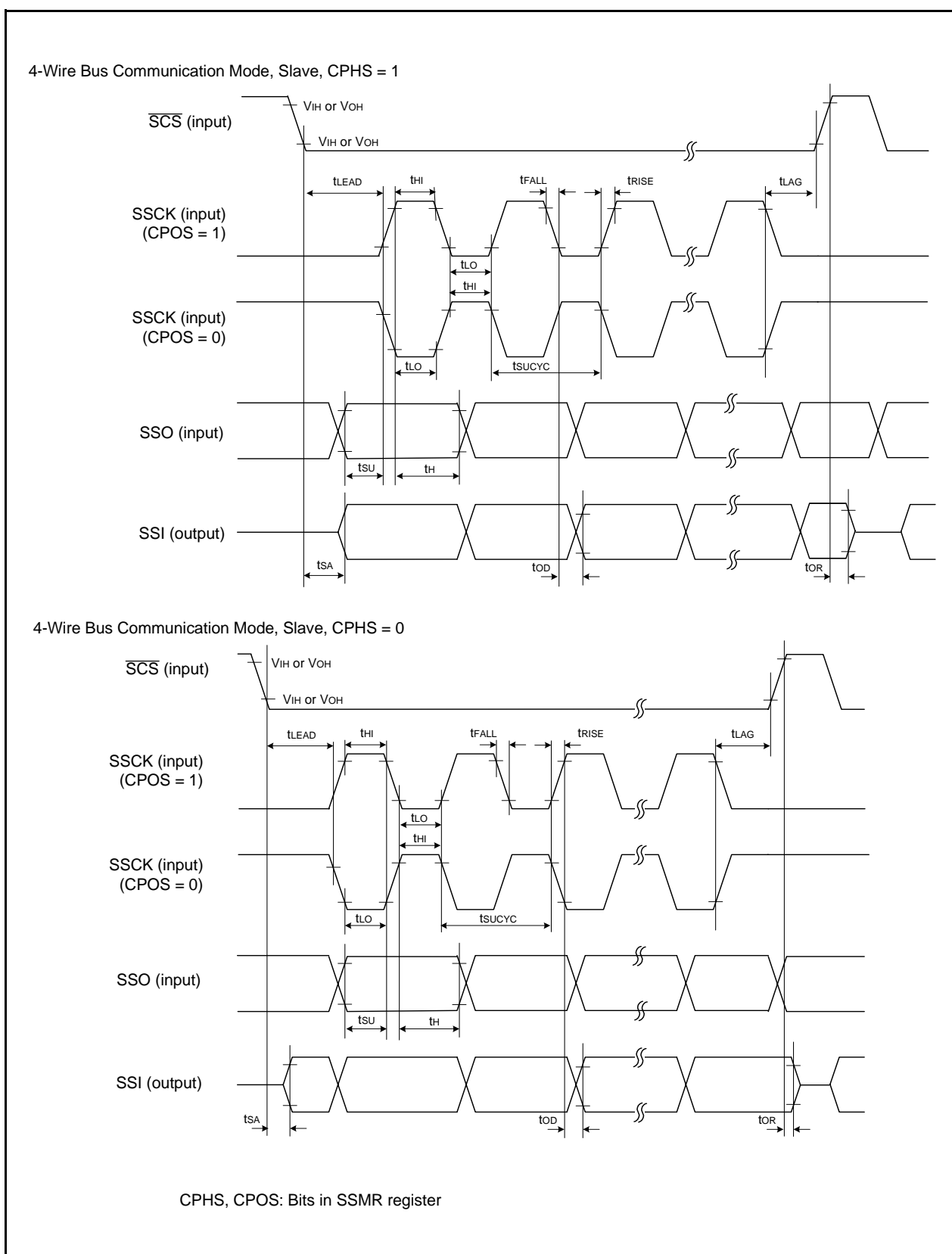
1. VCC = 2.2 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

**Table 5.12 Power Supply Circuit Timing Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on <sup>(2)</sup>		1	—	2000	μs
td(R-S)	STOP exit time <sup>(3)</sup>		—	—	150	μs

NOTES:

1. The measurement condition is VCC = 2.2 to 5.5 V and Topr = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.



**Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)**



**Table 5.16 Electrical Characteristics (2) [V<sub>CC</sub> = 5 V]**  
**(T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

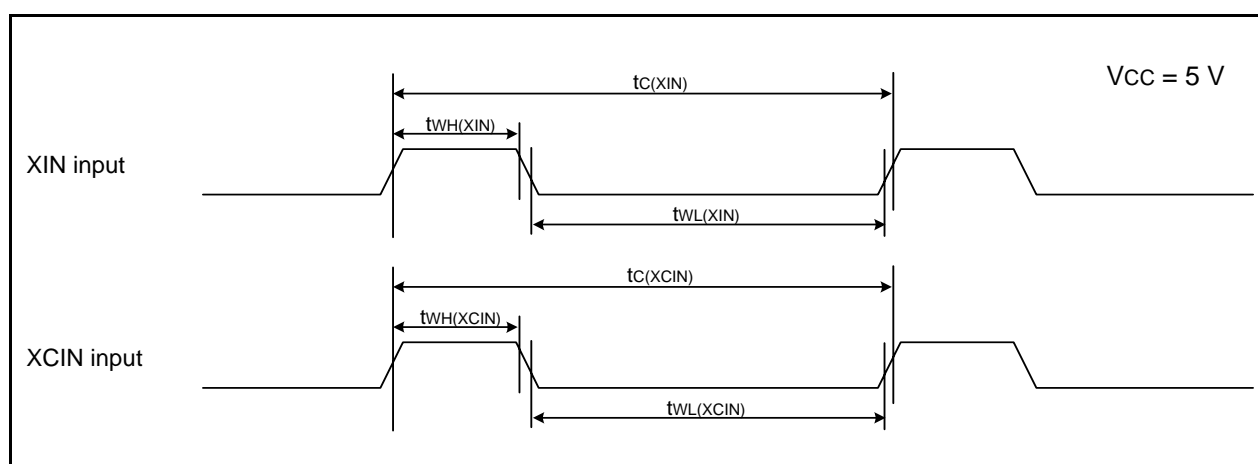
Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	μA

**Table 5.17 Electrical Characteristics (3) [V<sub>CC</sub> = 5 V]**  
**(T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

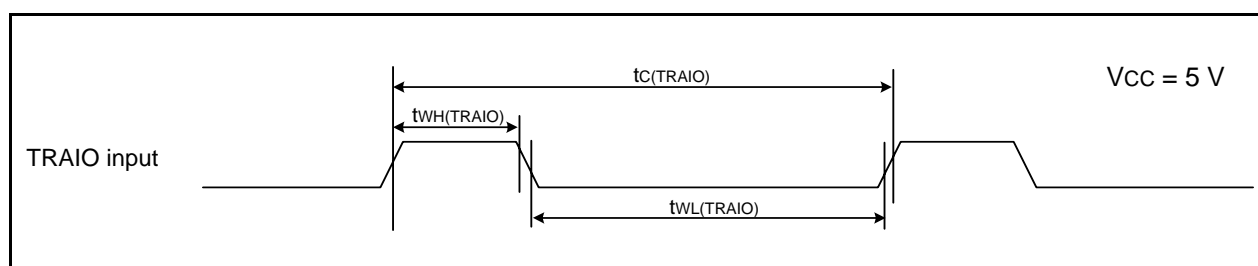
Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4.0	–	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.2	–	μA
		Increase during A/D converter operation	Without sample & hold	–	2.6	–	mA
			With sample & hold	–	1.6	–	mA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	μA

**Timing Requirements****(Unless Otherwise Specified:  $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{op} = 25^{\circ}\text{C}$ ) [ $V_{CC} = 5\text{ V}$ ]****Table 5.18 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	$\mu\text{s}$
$t_{WH(XCIN)}$	XCIN input "H" width	7	–	$\mu\text{s}$
$t_{WL(XCIN)}$	XCIN input "L" width	7	–	$\mu\text{s}$

**Figure 5.8 XIN Input and XCIN Input Timing Diagram when  $V_{CC} = 5\text{ V}$** **Table 5.19 TRAIO Input**

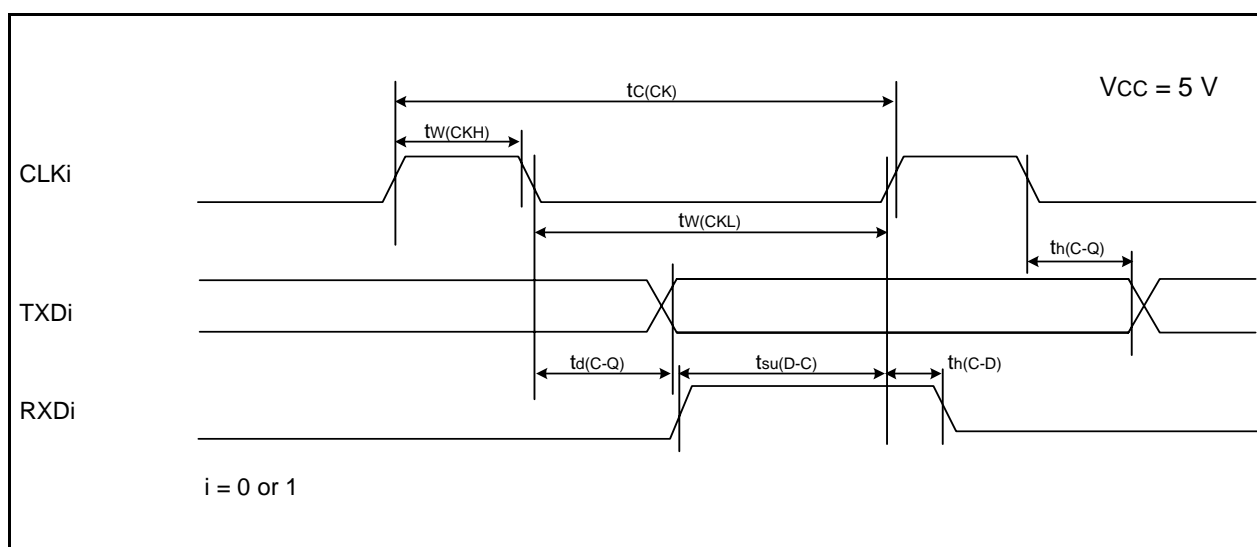
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns

**Figure 5.9 TRAIO Input Timing Diagram when  $V_{CC} = 5\text{ V}$**

**Table 5.20 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

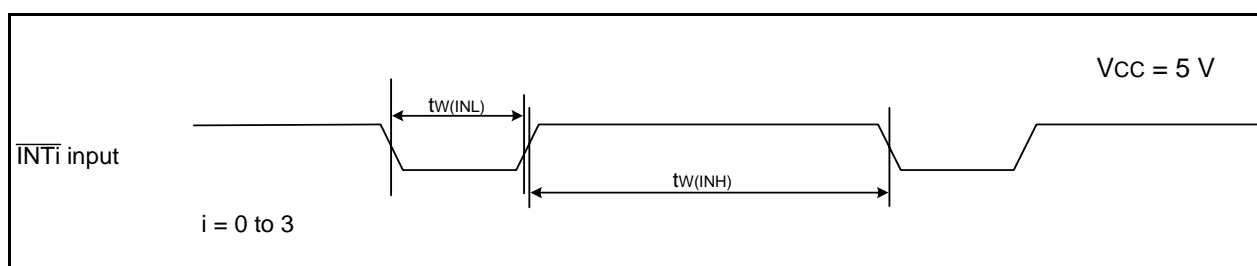
i = 0 or 1

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.21 External Interrupt  $\overline{INTi}$  (i = 0 to 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	250 <sup>(1)</sup>	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	250 <sup>(2)</sup>	—	ns

**NOTES:**

- When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.11 External Interrupt  $\overline{INTi}$  Input Timing Diagram when Vcc = 5 V**

**Table 5.23 Electrical Characteristics (4) [Vcc = 3 V]**  
**(T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I <sub>cc</sub>	Power supply current (V <sub>cc</sub> = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V <sub>ss</sub>	High-speed clock mode	–	6	–	mA
				2	–	mA
		High-speed on-chip oscillator mode	–	5	9	mA
				2	–	mA
		Low-speed on-chip oscillator mode	–	130	300	μA
				130	300	μA
		Wait mode	–	25	70	μA
				23	55	μA
		Increase during A/D converter operation	–	0.9	–	mA
				0.5	–	mA
		Stop mode	–	0.7	3.0	μA
				1.1	–	μA

**Table 5.28 Electrical Characteristics (5) [V<sub>CC</sub> = 2.2 V]**

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V <sub>OH</sub>	Output "H" voltage	Except P2_0 to P2_7, XOUT	I <sub>OH</sub> = -1 mA		V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
		P2_0 to P2_7	Drive capacity HIGH	I <sub>OH</sub> = -2 mA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
			Drive capacity LOW	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
		XOUT	Drive capacity HIGH	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
			Drive capacity LOW	I <sub>OH</sub> = -50 μA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
V <sub>OL</sub>	Output "L" voltage	Except P2_0 to P2_7, XOUT	I <sub>OL</sub> = 1 mA		—	—	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I <sub>OL</sub> = 2 mA	—	—	0.5	V
			Drive capacity LOW	I <sub>OL</sub> = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I <sub>OL</sub> = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I <sub>OL</sub> = 50 μA	—	—	0.5	V
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}}, \overline{\text{INT3}}, \text{KI0}, \text{KI1}, \text{KI2}, \text{KI3}, \text{TRAIO}, \text{RXD0}, \text{RXD1}, \text{CLK0}, \text{CLK1}, \text{SSI}, \text{SCL}, \text{SDA}, \text{SSO}$			0.05	0.3	—	V
		$\overline{\text{RESET}}$			0.05	0.15	—	V
I <sub>IH</sub>	Input "H" current		V <sub>I</sub> = 2.2 V		—	—	4.0	μA
I <sub>IL</sub>	Input "L" current		V <sub>I</sub> = 0 V		—	—	-4.0	μA
R <sub>PULLUP</sub>	Pull-up resistance		V <sub>I</sub> = 0 V		100	200	600	kΩ
R <sub>FXIN</sub>	Feedback resistance	XIN			—	5	—	MΩ
R <sub>FXCIN</sub>	Feedback resistance	XCIN			—	35	—	MΩ
V <sub>RAM</sub>	RAM hold voltage		During stop mode		1.8	—	—	V

## NOTE:

- V<sub>CC</sub> = 2.2 V at T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

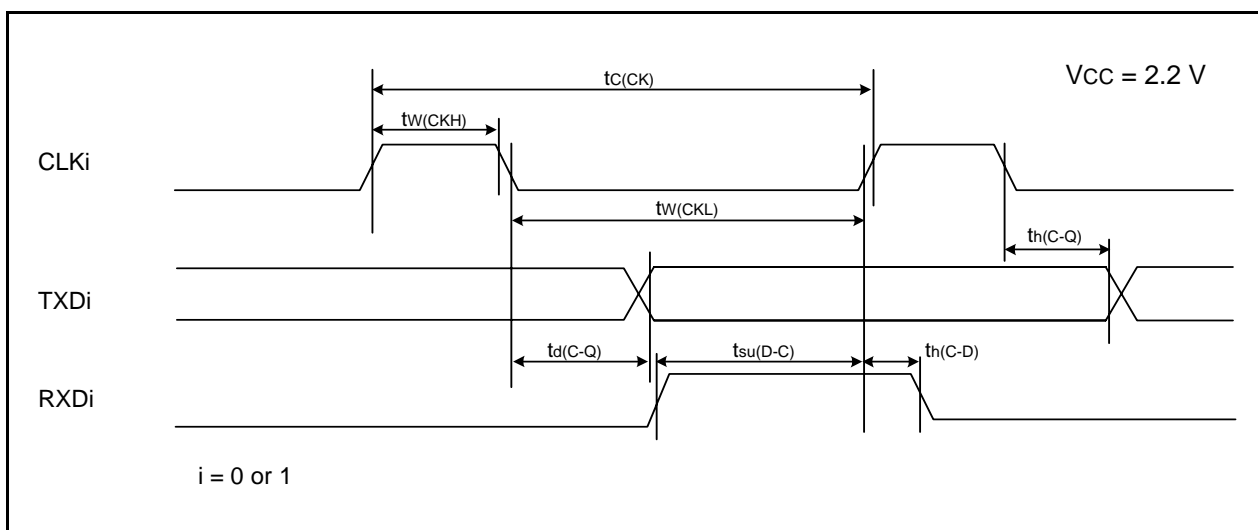
**Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V]  
(T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I <sub>cc</sub>	Power supply current (V <sub>cc</sub> = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V <sub>ss</sub>	High-speed clock mode	-	3.5	-	mA
				1.5	-	mA
		High-speed on-chip oscillator mode	-	3.5	-	mA
				1.5	-	mA
		Low-speed on-chip oscillator mode	-	100	230	μA
				100	230	μA
		Low-speed clock mode	-	25	-	μA
				-	-	μA
		Wait mode	-	22	60	μA
				20	55	μA
				3.0	-	μA
				1.8	-	μA
				-	-	μA
		Increase during A/D converter operation	-	0.4	-	mA
				0.3	-	mA
		Stop mode	-	0.7	3.0	μA
				1.1	-	μA

**Table 5.32 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input “H” width	400	—	ns
$t_{w(CKL)}$	CLKi input “L” width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

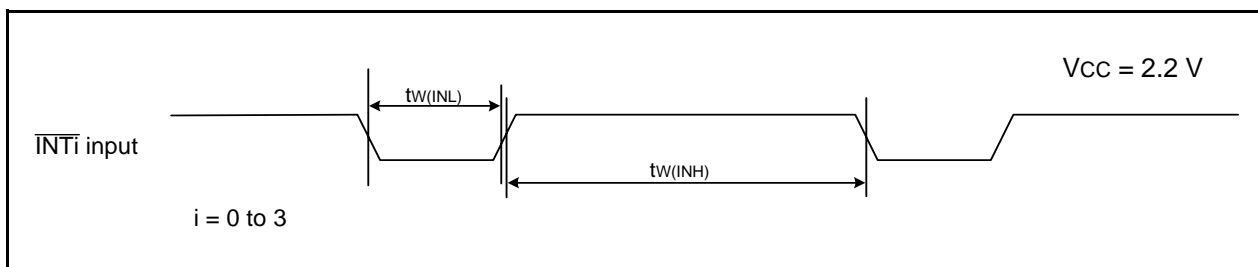
i = 0 or 1

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.33 External Interrupt  $\overline{INTi}$  (i = 0 to 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input “H” width	1000 <sup>(1)</sup>	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input “L” width	1000 <sup>(2)</sup>	—	ns

## NOTES:

1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 External Interrupt  $\overline{INTi}$  Input Timing Diagram when Vcc = 2.2 V**



# REVISION HISTORY

# R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Feb 24, 2005	1 to 3 5, 6	Pin type changed: 48-pin(under consideration) → 52-pin.
		5 to 7	Package type revised: 48-pin LQFP(under consideration) → PLQP0052JA-A
		8	Table 1.5 TCLK added, VREF revised.
		9	Table 1.6 revised.
		13, 14	Figures 3.1 and 3.2 part number revised.
		15	Tabel 4.1 revised: - 000Fh: 000XXXXXb → 00011111b - 0023h: FR0 → FRA0 - 0024h: FR1 → FRA1 - 0025h: FR2 → FRA2 - 0031h: Voltage Detection A Register 1, VC1 → Voltage Detection Register 1, VCA1 - 0032h: Voltage Detection A Register 2, VC2 → Voltage Detection Register 2, VCA2
		17	Tabel 4.3 Register name and the value after reset at 00B8h to 00BFh revised; NOTE2 added.
		19	Tabel 4.5 revised: - 0107h: LINSR → LINST - 0137h to 013Fh: Register symbol revised
		20	Tabel 4.6 revised: - 0140h to 015Fh: Register symbol revised - 0158h, 0159h: Timer RD General Register → Timer RD General Register A1
0.20	Mar 8, 2005	2, 3 8	Tables 1.1, 1.2 and 1.5 revised: "main clock" → "XIN clock"; "sub clock" → "XCIN clock"
		15	- 0023h to 0025h: 40MHz On-Chip Oscillator Control Register → High-Speed On-Chip Oscillator Control Register
0.30	Sep 01, 2005	2, 3	Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance • Serial Interface revised: - Serial Interface: 2 channels Clock synchronous serial I/O, UART - Clock Synchronous Serial Interface: 1 channel I <sup>2</sup> C bus Interface <sup>(1)</sup> , Clock synchronous serial I/O with chip select
		4	Figure 1.1 Block Diagram • UART or Clock Synchronous Serial Interface: "(8 bits × 1 channel)" → "(8 bits × 2 channels)" revised • UART (8 bits × 1 channel) deleted
		5, 6	Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group "Flash Memory Version" → "N Version" revised

# REVISION HISTORY

# R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	7	Figure 1.4 Pin Assignment <ul style="list-style-type: none"> <li>Pin name revised;  VSS → VSS/AVSS,  VCC → VCC/AVCC,  P1_5/RXD0/(TRAIO)/(INT1) → P1_5/RXD0/(TRAIO)/(INT1)<sup>(2)</sup>,  P6_6/INT2/(TXD1) → P6_6/INT2/TXD1,  P6_7/INT3/(RXD1) → P6_7/INT3/RXD1,  P6_5 → P6_5/CLK1</li> <li>NOTE2 added</li> </ul>
		8	Table 1.5 Pin Description <ul style="list-style-type: none"> <li>Analog Power Supply Input: line added</li> <li>INT Interrupt Input: "INT0 Timer RD input pins. INT1 Timer RA input pins." added</li> <li>Serial Interface: "CLK1" added</li> <li>"I<sup>2</sup>C Bus Interface (IIC)" → "I<sup>2</sup>C Bus Interface"</li> <li>"SSU" → "Clock Synchronous Serial I/O with Chip Select"</li> </ul>
		9	Table 1.6 Pin Name Information by Pin Number revised <ul style="list-style-type: none"> <li>Pin Number 10: "VSS" → "VSS/AVSS"</li> <li>Pin Number 12: "VCC" → "VCC/AVCC"</li> <li>Pin Number 27: "INT0" added</li> <li>Pin Number 28: "(TXD1)" → "TXD1"</li> <li>Pin Number 29: "(RXD1)" → "RXD1"</li> <li>Pin Number 35: "CLK1" added</li> </ul>
		15	Tabel 4.1 SFR Information(1) revised: <ul style="list-style-type: none"> <li>0012h: X0h → 00h</li> <li>0013h: XXXXXX00b → 00h</li> <li>0016h: X0h → 00h</li> <li>0036h: Voltage Monitor 1 Control Register<sup>(2)</sup> → Voltage Monitor 1 Control Register<sup>(5)</sup></li> <li>0038h: 00001000b<sup>(3)</sup>, 01000001b<sup>(4)</sup> → 0000X000b<sup>(3)</sup>, 0100X001b<sup>(4)</sup></li> <li>NOTES2, 5: "the voltage monitor 1 reset" added</li> <li>NOTE3: "voltage monitor 1 reset" → "voltage monitor 0 reset"</li> </ul>
		16	Tabel 4.2 SFR Information(2) revised: <ul style="list-style-type: none"> <li>0048h: RD0IC → TRD0IC</li> <li>0049h: RD1IC → TRD1IC</li> <li>004Ah: REIC → TREIC</li> <li>004Fh: SSU/IIC Interrupt Control Register, IIC2AIC → SSU/IIC Interrupt Control Register<sup>(2)</sup>, SSUAIC/IIC2AIC</li> <li>0056h: RAIC → TRAIC</li> <li>0058h: RBIC → TRBIC</li> <li>NOTE2 added</li> </ul>
		17	Tabel 4.3 SFR Information(3) revised: <ul style="list-style-type: none"> <li>00BCh: 00h → 00h/0000X000b</li> </ul>
		18	Tabel 4.4 SFR Information(4) revised: <ul style="list-style-type: none"> <li>00D6h: 00000XXXb → 00h</li> <li>00F5h: UART1 Function Select Register, U1SR, XXh added</li> </ul>

# REVISION HISTORY

# R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.40	Jan 24, 2006	15	Table 4.1 SFR Information(1); 0024h: "TBD" → "When shipping" NOTES 3 and 4 revised
		19	Table 4.5 SFR Information (5); 0118h: "Timer RE Second Data Register" → "Timer RE Second Data Register / Counter Data Register" 0119h: "Timer RE Minute Data Register" → "Timer RE Minute Data Register / Compare Data Register" 0138h: "TRDMDR" → "TRDMR" 013Bh: "Timer RD Output Master Enable Register" → "Timer RD Output Master Enable Register 1"
		22	Table 5.1 Absolute Maximum Ratings; "VCC" → "VCC/AVCC" revised Table 5.2 Recommended Operating Conditions revised
		23	Table 5.3 A/D Converter Characteristics revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics revised
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical revised
		26	Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics revised Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics revised Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics revised
		28	Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.13 Power Supply Circuit Timing Characteristics revised
		29	Table 5.14 Timing Requirements of Clock Synchronous Serial I/O with Chip Select revised
		33	Table 5.15 Timing Requirements of I <sup>2</sup> C bus Interface NOTE1 revised
		34	Table 5.16 Electrical Characteristics (1) [VCC = 5 V] revised
		35	Table 5.17 Electrical Characteristics (2) [VCC = 5 V] revised
		36	Table 5.18 XIN Input, XCIN Input revised
		37	Table 5.20 Serial Interface revised
		38	Table 5.22 Electrical Characteristics (3) [VCC = 3 V] revised
		39	Table 5.23 Electrical Characteristics (4) [Vcc = 3 V] revised
		40	Table 5.24 XIN Input, XCIN Input revised
		41	Table 5.26 Serial Interface revised
		42	Table 5.28 Electrical Characteristics (5) [Vcc = 2.2 V] revised
		43	Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V] revised
		44	Table 5.30 XIN Input, XCIN Input revised Table 5.31 TRAIO Input, INT1 Input revised
		45	Table 5.32 Serial Interface revised Table 5.33 External Interrupt INTi (i = 0, 2, 3) Input

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet
------------------	--------------------------------------

Rev.	Date	Description	
		Page	Summary
0.40	Jan 24, 2006	46	Package Dimensions; “TBD” → “PLQP0052JA-A (52P6A-A)” added
1.00	May 31, 2006	all pages	“Under development” deleted
		1	1. Overview; “data flash ROM” → “data flash” revised
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; “System clock generator” → “System clock generation circuit” revised
		5 to 6	Table 1.3 Product Information for R8C/24 Group and Table 1.4 Product Information for R8C/25 Group; A part of (D) mark is deleted.
		9	Table 1.6 Pin Name Information by Pin Number NOTE1 added
		15	Table 4.1 SFR Information(1); 001Ch: “00h” → “00h, 10000000b” revised 0029h: High-Speed On-Chip Oscillator Control Register 4 FRA4 When shipping added 002Bh: High-Speed On-Chip Oscillator Control Register 6 FRA6 When shipping added NOTE6 added
		19	Table 4.5 SFR Information(5); 0118h: Timer RE Second Data Register / Counter Data Register, 0119h: Timer RE Minute Data Register / Compare Data Register register name revised
		20	Table 4.6 SFR Information(6); 0143h: “11000000b” → “11100000b” revised
		22	Table 5.2 Recommended Operating Conditions revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics revised
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics revised
		26	Figure 5.2 Time delay until Suspend title revised
		27	Table 5.9 Voltage Monitor 0 Reset Electrical Characteristics → Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics revised Table 5.10 Power-on Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 0 Reset) deleted Figure 5.3 Power-on Reset Circuit Electrical Characteristics revised
		28	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised
		35	Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] revised
		39	Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] revised
		43	Table 5.28 Electrical Characteristics (6) [Vcc = 2.2 V] revised
		46	Package Dimensions; “The latest package ... Renesas Technology website.” added

Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
  - (1) artificial life support devices or systems
  - (2) surgical implantations
  - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
  - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



**RENESAS SALES OFFICES**

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

**Renesas Technology America, Inc.**  
450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

**Renesas Technology Hong Kong Ltd.**  
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2377-3473

**Renesas Technology Taiwan Co., Ltd.**  
10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

**Renesas Technology Singapore Pte. Ltd.**  
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**  
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510