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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 6 |
| Program Memory Size | 1KB (512 x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 64 x 8 |
| RAM Size | 64 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-SOIC (0.154", 3.90mm Width) |
| Supplier Device Package | 8-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/attiny13a-ssu |

## Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 120 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Througput at 20 MHz
- High Endurance Non-volatile Memory segments
  - 1K Bytes of In-System Self-programmable Flash program memory
  - 64 Bytes EEPROM
  - 64 Bytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 Years at 85°C/100 Years at 25°C (see page 6)
  - Programming Lock for Self-Programming Flash & EEPROM Data Security
- Peripheral Features
  - One 8-bit Timer/Counter with Prescaler and Two PWM Channels
  - 4-channel, 10-bit ADC with Internal Voltage Reference
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - debugWIRE On-chip Debug System
  - In-System Programmable via SPI Port
  - External and Internal Interrupt Sources
  - Low Power Idle, ADC Noise Reduction, and Power-down Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Brown-out Detection Circuit with Software Disable Function
  - Internal Calibrated Oscillator
- I/O and Packages
  - 8-pin PDIP/SOIC: Six Programmable I/O Lines
  - 10-pad MLF: Six Programmable I/O Lines
  - 20-pad MLF: Six Programmable I/O Lines
- Operating Voltage:
  - 1.8 – 5.5V
- Speed Grade:
  - 0 – 4 MHz @ 1.8 – 5.5V
  - 0 – 10 MHz @ 2.7 – 5.5V
  - 0 – 20 MHz @ 4.5 – 5.5V
- Industrial Temperature Range
- Low Power Consumption
  - Active Mode:
    - 190 µA at 1.8 V and 1 MHz
  - Idle Mode:
    - 24 µA at 1.8 V and 1 MHz

# 8-bit AVR® Microcontroller with 1K Bytes In-System Programmable Flash

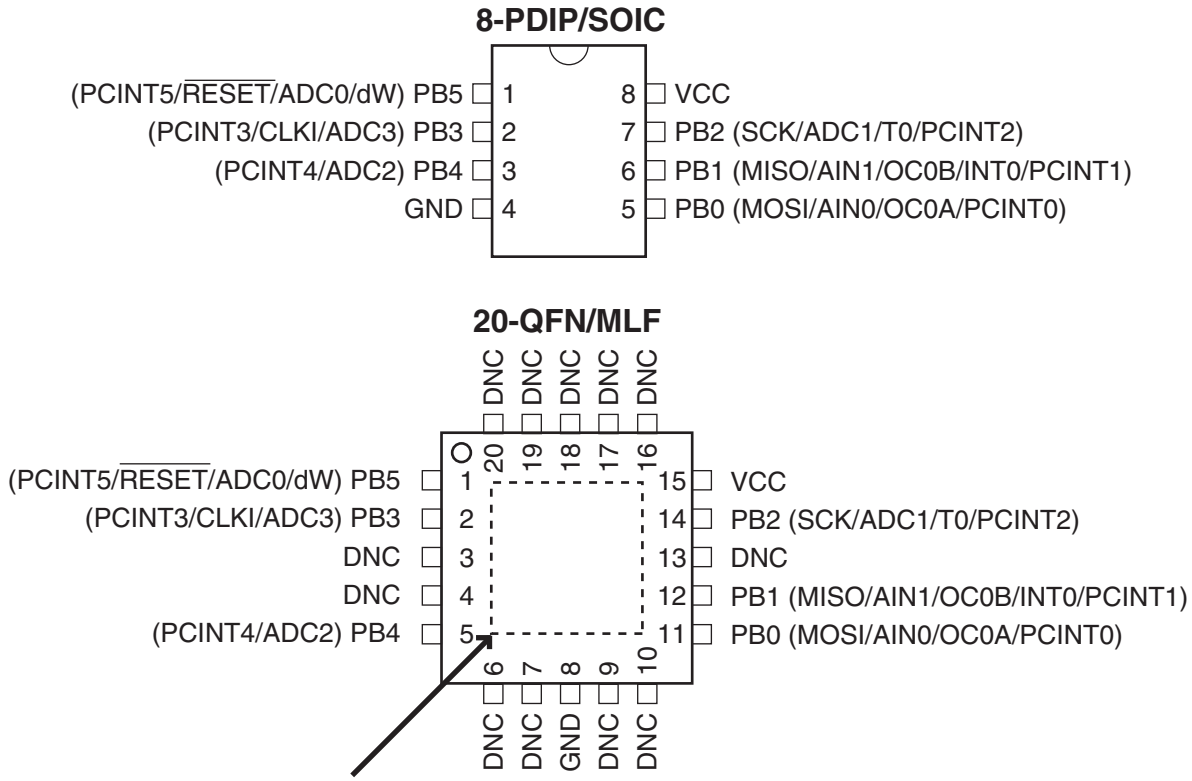
# ATtiny13A

# Summary

Rev. 8126FS–AVR–05/12

# 1. Pin Configurations

**Figure 1-1.** Pinout of ATtiny13A




NOTE: Bottom pad should be soldered to ground.
DNC: Do Not Connect

NOTE: Bottom pad should be soldered to ground.
DNC: Do Not Connect

## 1.1 Pin Description

### 1.1.1 VCC

Supply voltage.

### 1.1.2 GND

Ground.

### 1.1.3 Port B (PB5:PB0)

Port B is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny13A as listed on page 55.

### 1.1.4 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in Table 18-4 on page 120. Shorter pulses are not guaranteed to generate a reset.

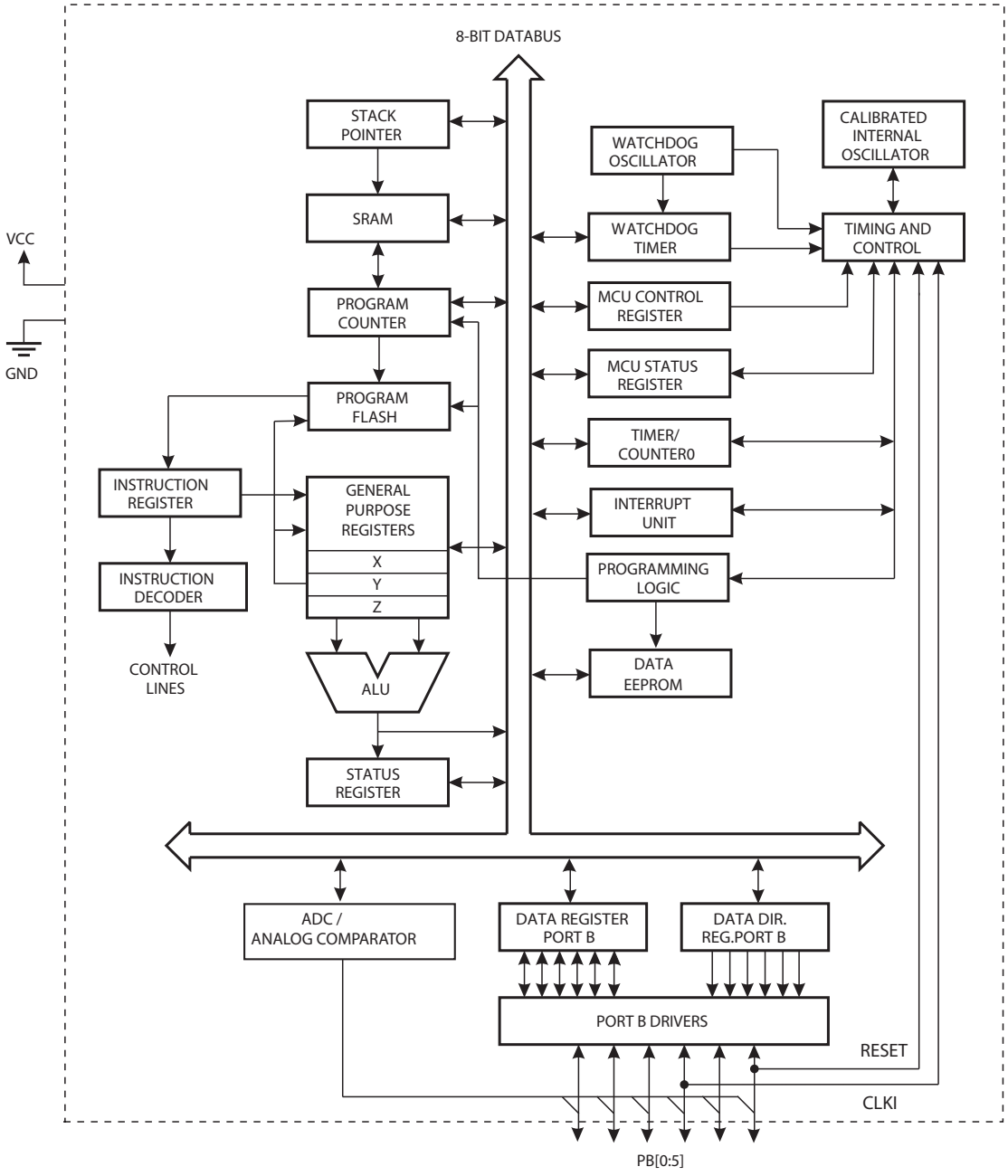
The reset pin can also be used as a (weak) I/O pin.

# 2. Overview

The ATtiny13A is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny13A achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

## 2.1 Block Diagram

**Figure 2-1.** Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny13A provides the following features: 1K byte of In-System Programmable Flash, 64 bytes EEPROM, 64 bytes SRAM, 6 general purpose I/O lines, 32 general purpose working registers, one 8-bit Timer/Counter with compare modes, Internal and External Interrupts, a 4-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. The Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core.

The ATtiny13A AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, and Evaluation kits.

# 3. About

## 3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at http://www.atmel.com/avr.

## 3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

## 3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

# 4. Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x3F | SREG | I | T | H | S | V | N | Z | C | page 9 |
| 0x3E | Reserved | – | – | – | – | – | – | – | – | |
| 0x3D | SPL | SP[7:0] | | | | | | | | page 11 |
| 0x3C | Reserved | – | – | – | – | – | – | – | – | |
| 0x3B | GIMSK | – | INT0 | PCIE | – | – | – | – | – | page 47 |
| 0x3A | GIFR | – | INTF0 | PCIF | – | – | – | – | – | page 48 |
| 0x39 | TIMSK0 | – | – | – | – | OCIE0B | OCIE0A | TOIE0 | – | page 75 |
| 0x38 | TIFR0 | – | – | – | – | OCF0B | OCF0A | TOV0 | – | page 76 |
| 0x37 | SPMCSR | – | – | – | CTPB | RFLB | PGWRT | PGERS | SELFPR- | page 98 |
| 0x36 | OCR0A | Timer/Counter – Output Compare Register A | | | | | | | | page 75 |
| 0x35 | MCUCR | – | PUD | SE | SM1 | SM0 | – | ISC01 | ISC00 | pages 33, 47, 57 |
| 0x34 | MCUSR | – | – | – | – | WDRF | BORF | EXTRF | PORF | page 42 |
| 0x33 | TCCR0B | FOC0A | FOC0B | – | – | WGM02 | CS02 | CS01 | CS00 | page 73 |
| 0x32 | TCNT0 | Timer/Counter (8-bit) | | | | | | | | page 74 |
| 0x31 | OSCCAL | Oscillator Calibration Register | | | | | | | | page 27 |
| 0x30 | BODCR | – | – | – | – | – | – | BODS | BODSE | page 33 |
| 0x2F | TCCR0A | COM0A1 | COM0A0 | COM0B1 | COM0B0 | – | – | WGM01 | WGM00 | page 70 |
| 0x2E | DWDR | DWDR[7:0] | | | | | | | | page 97 |
| 0x2D | Reserved | – | | | | | | | | |
| 0x2C | Reserved | – | | | | | | | | |
| 0x2B | Reserved | – | | | | | | | | |
| 0x2A | Reserved | – | | | | | | | | |
| 0x29 | OCR0B | Timer/Counter – Output Compare Register B | | | | | | | | page 75 |
| 0x28 | GTCCR | TSM | – | – | – | – | – | – | PSR10 | page 78 |
| 0x27 | Reserved | – | | | | | | | | |
| 0x26 | CLKPR | CLKPCE | – | – | – | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | page 28 |
| 0x25 | PRR | – | – | – | – | – | – | PRTIM0 | PRADC | page 34 |
| 0x24 | Reserved | – | | | | | | | | |
| 0x23 | Reserved | – | | | | | | | | |
| 0x22 | Reserved | – | | | | | | | | |
| 0x21 | WDTCR | WDTIF | WDTIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | page 42 |
| 0x20 | Reserved | – | | | | | | | | |
| 0x1F | Reserved | – | | | | | | | | |
| 0x1E | EEARL | – | – | EEPROM Address Register | | | | | | page 20 |
| 0x1D | EEDR | EEPROM Data Register | | | | | | | | page 20 |
| 0x1C | EECR | – | – | EEPM1 | EEPM0 | EERIE | EEMPE | EEPE | EERE | page 21 |
| 0x1B | Reserved | – | | | | | | | | |
| 0x1A | Reserved | – | | | | | | | | |
| 0x19 | Reserved | – | | | | | | | | |
| 0x18 | PORTB | – | – | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | page 57 |
| 0x17 | DDRB | – | – | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | page 57 |
| 0x16 | PINB | – | – | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | page 58 |
| 0x15 | PCMSK | – | – | PCINT5 | PCINT4 | PCINT3 | PCINT2 | PCINT1 | PCINT0 | page 48 |
| 0x14 | DIDR0 | – | – | ADC0D | ADC2D | ADC3D | ADC1D | AIN1D | AIN0D | pages 81, 95 |
| 0x13 | Reserved | – | | | | | | | | |
| 0x12 | Reserved | – | | | | | | | | |
| 0x11 | Reserved | – | | | | | | | | |
| 0x10 | Reserved | – | | | | | | | | |
| 0x0F | Reserved | – | | | | | | | | |
| 0x0E | Reserved | – | | | | | | | | |
| 0x0D | Reserved | – | | | | | | | | |
| 0x0C | Reserved | – | | | | | | | | |
| 0x0B | Reserved | – | | | | | | | | |
| 0x0A | Reserved | – | | | | | | | | |
| 0x09 | Reserved | – | | | | | | | | |
| 0x08 | ACSR | ACD | ACBG | ACO | ACI | ACIE | – | ACIS1 | ACIS0 | page 80 |
| 0x07 | ADMUX | – | REFS0 | ADLAR | – | – | – | MUX1 | MUX0 | page 92 |
| 0x06 | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | page 93 |
| 0x05 | ADCH | ADC Data Register High Byte | | | | | | | | page 94 |
| 0x04 | ADCL | ADC Data Register Low Byte | | | | | | | | page 94 |
| 0x03 | ADCSRB | – | ACME | – | – | – | ADTS2 | ADTS1 | ADTS0 | pages 80, 95 |
| 0x02 | Reserved | – | | | | | | | | |
| 0x01 | Reserved | – | | | | | | | | |
| 0x00 | Reserved | – | | | | | | | | |

Notes: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.ome of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

# 5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ADD | Rd, Rr | Add two Registers | Rd ← Rd + Rr | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | Rd ← Rd + Rr + C | Z,C,N,V,H | 1 |
| ADIW | Rdl,K | Add Immediate to Word | Rdh:Rdl ← Rdh:Rdl + K | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | Rd ← Rd - Rr | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | Rd ← Rd - K | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | Rd ← Rd - Rr - C | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | Rd ← Rd - K - C | Z,C,N,V,H | 1 |
| SBIW | Rdl,K | Subtract Immediate from Word | Rdh:Rdl ← Rdh:Rdl - K | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | Rd ← Rd • Rr | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | Rd ← Rd • K | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | Rd ← Rd v Rr | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | Rd ← Rd v K | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | Rd ← Rd ⊕ Rr | Z,N,V | 1 |
| COM | Rd | One’s Complement | Rd ← 0xFF – Rd | Z,C,N,V | 1 |
| NEG | Rd | Two’s Complement | Rd ← 0x00 – Rd | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | Rd ← Rd v K | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | Rd ← Rd • (0xFF - K) | Z,N,V | 1 |
| INC | Rd | Increment | Rd ← Rd + 1 | Z,N,V | 1 |
| DEC | Rd | Decrement | Rd ← Rd – 1 | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | Rd ← Rd • Rd | Z,N,V | 1 |
| CLR | Rd | Clear Register | Rd ← Rd ⊕ Rd | Z,N,V | 1 |
| SER | Rd | Set Register | Rd ← 0xFF | None | 1 |
| BRANCH INSTRUCTIONS | | | | | |
| RJMP | k | Relative Jump | PC ← PC + k + 1 | None | 2 |
| IJMP | | Indirect Jump to (Z) | PC ← Z | None | 2 |
| RCALL | k | Relative Subroutine Call | PC ← PC + k + 1 | None | 3 |
| ICALL | | Indirect Call to (Z) | PC ← Z | None | 3 |
| RET | | Subroutine Return | PC ← STACK | None | 4 |
| RETI | | Interrupt Return | PC ← STACK | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) PC ← PC + 2 or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | Rd – Rr | Z, N,V,C,H | 1 |
| CPC | Rd,Rr | Compare with Carry | Rd – Rr – C | Z, N,V,C,H | 1 |
| CPI | Rd,K | Compare Register with Immediate | Rd – K | Z, N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then PC←PC+k + 1 | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then PC←PC+k + 1 | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N ⊕ V= 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N ⊕ V= 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if ( I = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if ( I = 0) then PC ← PC + k + 1 | None | 1/2 |
| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
| SBI | P,b | Set Bit in I/O Register | I/O(P,b) ← 1 | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | I/O(P,b) ← 0 | None | 2 |
| LSL | Rd | Logical Shift Left | Rd(n+1) ← Rd(n), Rd(0) ← 0 | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | Rd(n) ← Rd(n+1), Rd(7) ← 0 | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7) | Z,C,N,V | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| ROR | Rd | Rotate Right Through Carry | Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0) | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | Rd(n) ← Rd(n+1), n=0..6 | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0) | None | 1 |
| BSET | s | Flag Set | SREG(s) ← 1 | SREG(s) | 1 |
| BCLR | s | Flag Clear | SREG(s) ← 0 | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | T ← Rr(b) | T | 1 |
| BLD | Rd, b | Bit load from T to Register | Rd(b) ← T | None | 1 |
| SEC | | Set Carry | C ← 1 | C | 1 |
| CLC | | Clear Carry | C ← 0 | C | 1 |
| SEN | | Set Negative Flag | N ← 1 | N | 1 |
| CLN | | Clear Negative Flag | N ← 0 | N | 1 |
| SEZ | | Set Zero Flag | Z ← 1 | Z | 1 |
| CLZ | | Clear Zero Flag | Z ← 0 | Z | 1 |
| SEI | | Global Interrupt Enable | I ← 1 | I | 1 |
| CLI | | Global Interrupt Disable | I ← 0 | I | 1 |
| SES | | Set Signed Test Flag | S ← 1 | S | 1 |
| CLS | | Clear Signed Test Flag | S ← 0 | S | 1 |
| SEV | | Set Twos Complement Overflow. | V ← 1 | V | 1 |
| CLV | | Clear Twos Complement Overflow | V ← 0 | V | 1 |
| SET | | Set T in SREG | T ← 1 | T | 1 |
| CLT | | Clear T in SREG | T ← 0 | T | 1 |
| SEH | | Set Half Carry Flag in SREG | H ← 1 | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | H ← 0 | H | 1 |
| DATA TRANSFER INSTRUCTIONS | | | | | |
| MOV | Rd, Rr | Move Between Registers | Rd ← Rr | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | Rd+1:Rd ← Rr+1:Rr | None | 1 |
| LDI | Rd, K | Load Immediate | Rd ← K | None | 1 |
| LD | Rd, X | Load Indirect | Rd ← (X) | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | Rd ← (X), X ← X + 1 | None | 2 |
| LD | Rd, - X | Load Indirect and Pre-Dec. | X ← X - 1, Rd ← (X) | None | 2 |
| LD | Rd, Y | Load Indirect | Rd ← (Y) | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | Rd ← (Y), Y ← Y + 1 | None | 2 |
| LD | Rd, - Y | Load Indirect and Pre-Dec. | Y ← Y - 1, Rd ← (Y) | None | 2 |
| LDD | Rd,Y+q | Load Indirect with Displacement | Rd ← (Y + q) | None | 2 |
| LD | Rd, Z | Load Indirect | Rd ← (Z) | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | Rd ← (Z), Z ← Z+1 | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | Z ← Z - 1, Rd ← (Z) | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | Rd ← (Z + q) | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | Rd ← (k) | None | 2 |
| ST | X, Rr | Store Indirect | (X) ← Rr | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | (X) ← Rr, X ← X + 1 | None | 2 |
| ST | - X, Rr | Store Indirect and Pre-Dec. | X ← X - 1, (X) ← Rr | None | 2 |
| ST | Y, Rr | Store Indirect | (Y) ← Rr | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | (Y) ← Rr, Y ← Y + 1 | None | 2 |
| ST | - Y, Rr | Store Indirect and Pre-Dec. | Y ← Y - 1, (Y) ← Rr | None | 2 |
| STD | Y+q,Rr | Store Indirect with Displacement | (Y + q) ← Rr | None | 2 |
| ST | Z, Rr | Store Indirect | (Z) ← Rr | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | (Z) ← Rr, Z ← Z + 1 | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | Z ← Z - 1, (Z) ← Rr | None | 2 |
| STD | Z+q,Rr | Store Indirect with Displacement | (Z + q) ← Rr | None | 2 |
| STS | k, Rr | Store Direct to SRAM | (k) ← Rr | None | 2 |
| LPM | | Load Program Memory | R0 ← (Z) | None | 3 |
| LPM | Rd, Z | Load Program Memory | Rd ← (Z) | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | Rd ← (Z), Z ← Z+1 | None | 3 |
| SPM | | Store Program Memory | (z) ← R1:R0 | None | |
| IN | Rd, P | In Port | Rd ← P | None | 1 |
| OUT | P, Rr | Out Port | P ← Rr | None | 1 |
| PUSH | Rr | Push Register on Stack | STACK ← Rr | None | 2 |
| POP | Rd | Pop Register from Stack | Rd ← STACK | None | 2 |
| MCU CONTROL INSTRUCTIONS | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/Timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

## 6. Ordering Information

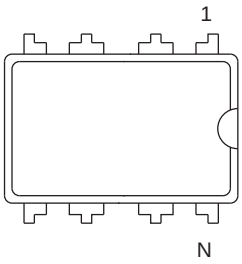
| Speed (MHz) | Power Supply (V) | Ordering Code[1] | Package[2] | Operation Range |
|---|---|---|---|---|
| 20 | 1.8 - 5.5 | ATtiny13A-PU<br>ATtiny13A-SU<br>ATtiny13A-SUR<br>ATtiny13A-SH<br>ATtiny13A-SHR<br>ATtiny13A-SSU<br>ATtiny13A-SSUR<br>ATtiny13A-SSH<br>ATtiny13A-SSHR<br>ATtiny13A-MU<br>ATtiny13A-MUR<br>ATtiny13A-MMU[3]<br>ATtiny13A-MMUR[3] | 8P3<br>8S2<br>8S2<br>8S2<br>8S2<br>8S1<br>8S1<br>8S1<br>8S1<br>20M1<br>20M1<br>10M1[3]<br>10M1[3] | Industrial<br>(-40°C to +85°C)[4] |
| | | ATtiny13A-SN<br>ATtiny13A-SNR<br>ATtiny13A-SS7<br>ATtiny13A-SS7R | 8S2<br>8S2<br>8S1<br>8S1 | Industrial<br>(-40°C to +105°C)[5] |
| | | ATtiny13A-SF<br>ATtiny13A-SFR<br>ATtiny13A-MMF<br>ATtiny13A-MMFR | 8S2<br>8S2<br>10M1[3]<br>10M1[3] | Industrial<br>(-40°C to +125°C)[6] |

Notes:
1. Code indicators:
   - H or 7: NiPdAu lead finish
   - U, N or F: matte tin
   - R: tape & reel
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. Topside marking for ATtiny13A:
   - 1st Line: T13
   - 2nd Line: Axx
   - 3rd Line: xxx
4. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
5. For typical and Electrical characteristics for this device please consult Appendix A, ATtiny13A Specification at 105°C.
6. For typical and Electrical characteristics for this device please consult Appendix B, ATtiny13A Specification at 125°C.

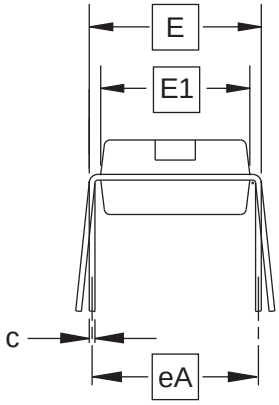
| Package Type | |
|---|---|
| **8P3** | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| **8S2** | 8-lead, 0.209" Wide, Plastic Small Outline Package (EIAJ SOIC) |
| **8S1** | 8-lead, 0.150" Wide, Plastic Gull-Wing Small Outline (JEDEC SOIC) |
| **20M1** | 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF) |
| **10M1** | 10-pad, 3 x 3 x 1 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF) |

# 7. Packaging Information

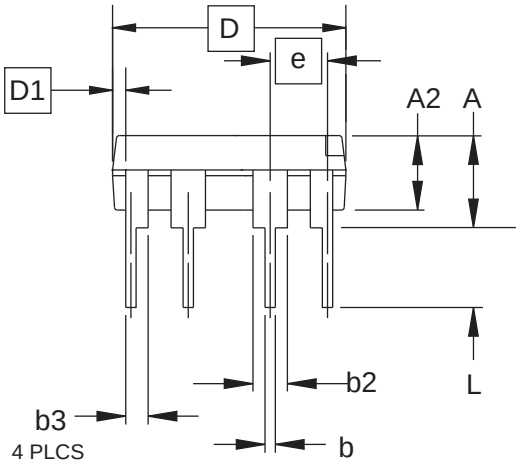
## 7.1 8P3




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = inches)

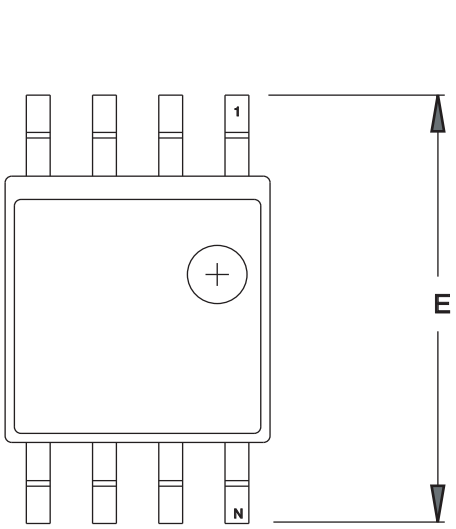
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | | | 0.210 | 2 |
| A2 | 0.115 | 0.130 | 0.195 | |
| b | 0.014 | 0.018 | 0.022 | 5 |
| b2 | 0.045 | 0.060 | 0.070 | 6 |
| b3 | 0.030 | 0.039 | 0.045 | 6 |
| c | 0.008 | 0.010 | 0.014 | |
| D | 0.355 | 0.365 | 0.400 | 3 |
| D1 | 0.005 | | | 3 |
| E | 0.300 | 0.310 | 0.325 | 4 |
| E1 | 0.240 | 0.250 | 0.280 | 3 |
| e | 0.100 BSC | | | |
| eA | 0.300 BSC | | | 4 |
| L | 0.115 | 0.130 | 0.150 | 2 |

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

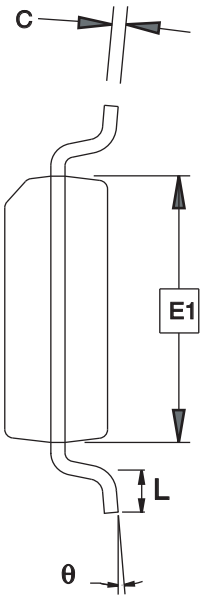
01/09/02

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP) | 8P3 | B |

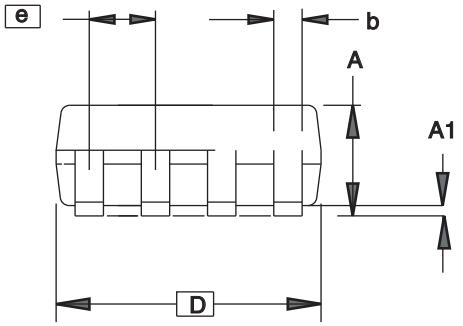
## 7.2 8S2




TOP VIEW




END VIEW




SIDE VIEW

**COMMON DIMENSIONS**
(Unit of Measure = mm)

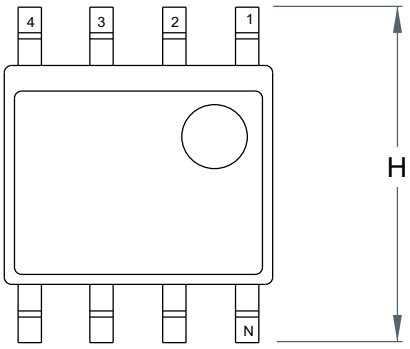
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 1.70 | | 2.16 | |
| A1 | 0.05 | | 0.25 | |
| b | 0.35 | | 0.48 | 4 |
| C | 0.15 | | 0.35 | 4 |
| D | 5.13 | | 5.35 | |
| E1 | 5.18 | | 5.40 | 2 |
| E | 7.70 | | 8.26 | |
| L | 0.51 | | 0.85 | |
| θ | 0° | | 8° | |
| e | 1.27 BSC | | | 3 |

Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

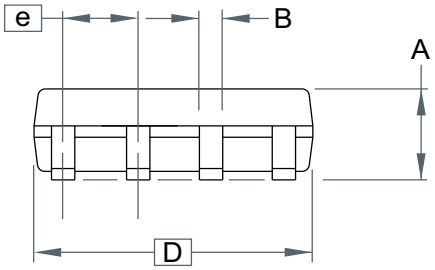
4/15/08

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| **Package Drawing Contact:** packagedrawings@atmel.com | **8S2,** 8-lead, 0.208” Body, Plastic Small Outline Package (EIAJ) | STN | 8S2 | F |

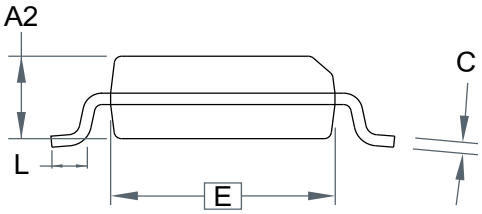
## 7.3 8S1




Top View




Side View




End View

**COMMON DIMENSIONS**
(Unit of Measure = mm)

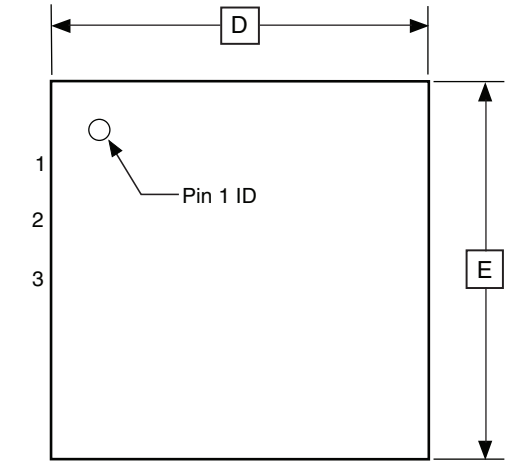
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.75 | |
| B | – | – | 0.51 | |
| C | – | – | 0.25 | |
| D | – | – | 5.00 | |
| E | – | – | 4.00 | |
| e | | 1.27 BSC | | |
| H | – | – | 6.20 | |
| L | – | – | 1.27 | |

Note: This drawing is for general information only. Refer to JEDEC Drawing MS-012 for proper dimensions, tolerances, datums, etc.

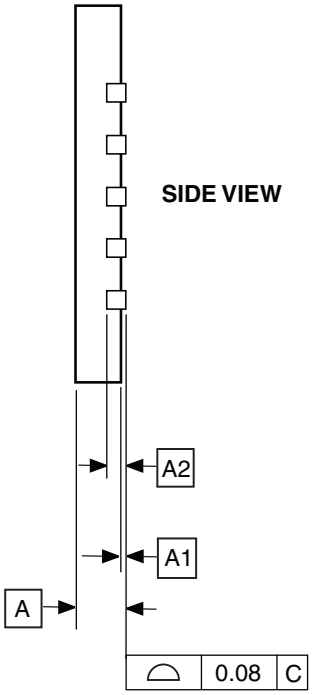
2010-10-20

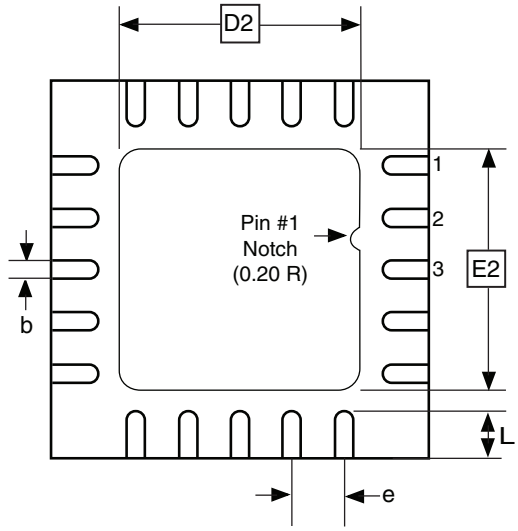
| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC) | 8S1 | B |

## 7.4 20M1




TOP VIEW




BOTTOM VIEW

**COMMON DIMENSIONS**
(Unit of Measure = mm)

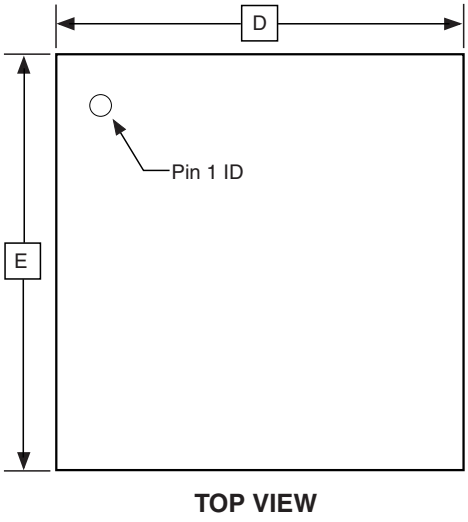
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 | |
| A1 | – | 0.01 | 0.05 | |
| A2 | | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | | 4.00 BSC | | |
| D2 | 2.45 | 2.60 | 2.75 | |
| E | | 4.00 BSC | | |
| E2 | 2.45 | 2.60 | 2.75 | |
| e | | 0.50 BSC | | |
| L | 0.35 | 0.40 | 0.55 | |

Note: Reference JEDEC Standard MO-220, Fig. 1 (SAW Singulation) WGGD-5.

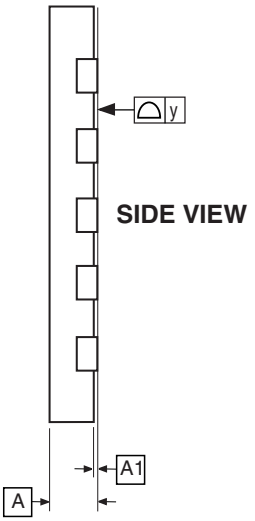
10/27/04

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **20M1**, 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm,<br>2.6 mm Exposed Pad, Micro Lead Frame Package (MLF) | 20M1 | B |

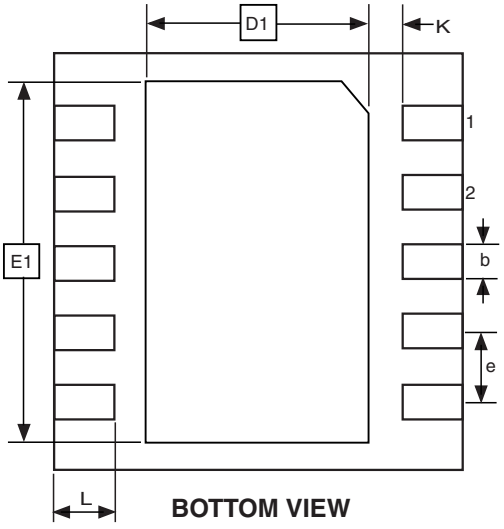
## 7.5 10M1




TOP VIEW




SIDE VIEW




BOTTOM VIEW

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| b | 0.18 | 0.25 | 0.30 | |
| D | 2.90 | 3.00 | 3.10 | |
| D1 | 1.40 | – | 1.75 | |
| E | 2.90 | 3.00 | 3.10 | |
| E1 | 2.20 | – | 2.70 | |
| e | | 0.50 | | |
| L | 0.30 | – | 0.50 | |
| y | – | – | 0.08 | |
| K | 0.20 | – | – | |

Notes: 1. This package conforms to JEDEC reference MO-229C, Variation VEED-5.
2. The terminal #1 ID is a Lasser-marked Feature.

7/7/06

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **10M1,** 10-pad, 3 x 3 x 1.0 mm Body, Lead Pitch 0.50 mm,<br>1.64 x 2.60 mm Exposed Pad, Micro Lead Frame Package | 10M1 | A |

# 8. Errata

The revision letters in this section refer to the revision of the ATtiny13A device.

## 8.1 ATtiny13A Rev. G – H

- **EEPROM can not be written below 1.9 Volt**

1. **EEPROM can not be written below 1.9 Volt**
   Writing the EEPROM at $V_{CC}$ below 1.9 volts might fail.

   **Problem Fix/Workaround**
   Do not write the EEPROM when $V_{CC}$ is below 1.9 volts.

## 8.2 ATtiny13A Rev. E – F

These device revisions were not sampled.

## 8.3 ATtiny13 Rev. A – D

These device revisions were referred to as ATtiny13/ATtiny13V.

# 9. Datasheet Revision History

Please note that page numbers in this section refer to the current version of this document and may not apply to previous versions.

## 9.1 Rev. 8126F – 05/12

1. Updated Table 10-5 on page 57.
2. Updated order codes on page 11.

## 9.2 Rev. 8126E – 07/10

1. Updated description in Section 6.4.2 “CLKPR – Clock Prescale Register” on page 28.
2. Adjusted notes in Table 18-1, “DC Characteristics, TA = -40°C to +85°C,” on page 117.
3. Updated plot order in Section 19. “Typical Characteristics” on page 124, added some plots, also some headers and figure titles adjusted.
4. Updated Section 6. “Ordering Information” on page 11, added extended temperature part numbers, as well tape & reel part numbers. Notes adjusted.
5. Updated bit syntax throughout the datasheet, e.g. from CS02:0 to CS0[2:0].

## 9.3 Rev. 8126D – 11/09

1. Added note “If the RSTDISPL fuse is programmed...” in Startup-up Times Table 6-5 and Table 6-6 on page 26.
2. Added addresses in all Register Description tables and cross-references to Register Summary.
3. Updated naming convention for -COM bits in tables from Table 11-2 on page 70 to Table 11-7 on page 72.
4. Updated value for $t_{WD\_ERASE}$ in Table 17-8, “Minimum Wait Delay Before Writing the Next Flash or EEPROM Location,” on page 108.
5. Added NiPdAU note for -SH and -SSH in Section 6. “Ordering Information” on page 11.

## 9.4 Rev. 8126C – 09/09

1. Added EEPROM errata for rev. G - H on page 17.
2. Added a note about topside marking in Section 6. “Ordering Information” on page 11.

## 9.5 Rev. 8126B – 11/08

1. Updated order codes on page 11 to reflect changes in material composition.
2. Updated sections:
   – “DIDR0 – Digital Input Disable Register 0” on page 81
   – “DIDR0 – Digital Input Disable Register 0” on page 95
3. Updated “Register Summary” on page 7.

## 9.6 Rev. 8126A – 05/08

1. Initial revision, created from document 2535I – 04/08.
2. Updated characteristic plots of section “Typical Characteristics” , starting on page 124.
3. Updated “Ordering Information” on page 11.
4. Updated section:
   – “Speed” on page 118

5. Update tables:
   - “DC Characteristics, TA = -40°C to +85°C” on page 117
   - “Calibration Accuracy of Internal RC Oscillator” on page 119
   - “Reset, Brown-out, and Internal Voltage Characteristics” on page 120
   - “ADC Characteristics, Single Ended Channels. TA = -40°C to +85°C” on page 121
   - “Serial Programming Characteristics, TA = -40°C to +85°C” on page 122
6. Added description of new function, “Power Reduction Register”:
   - Added functional description on page 31
   - Added bit description on page 34
   - Added section “Supply Current of I/O Modules” on page 124
   - Updated Register Summary on page 7
7. Added description of new function, “Software BOD Disable”:
   - Added functional description on page 31
   - Updated section on page 32
   - Added register description on page 33
   - Updated Register Summary on page 7
8. Added description of enhanced function, “Enhanced Power-On Reset”:
   - Updated Table 18-4 on page 120, and Table 18-5 on page 120

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