Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 58x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk20fn1m0vlq12

- Communication interfaces
  - USB high-/full-/low-speed On-the-Go controller with ULPI interface
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - USB Device Charger detect (USBDCD)
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital Host Controller (SDHC)
  - Two I2S modules

Field	Description	Values
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm)
CC	Maximum CPU frequency (MHz)	• 12 = 120 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK20FN1M0VLQ12

3 Terminology and guidelines

3.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 70°C • @ 105°C	—	7.08	10.74	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.03	4.48	mA	5
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.58	4.96	mA	5
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	0.64	4.29	mA	5
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.22	0.38	mA	
	• @ 70°C	—	0.78	1.33	mA	
	• @ 105°C	—	2.18	3.56	mA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.22	0.37	mA	
	• @ 70°C	—	0.78	1.33	mA	
	• @ 105°C	—	2.16	3.52	mA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ –40 to 25°C	—	4.09	5.58	µA	
	• @ 70°C	—	20.98	28.93	µA	
	• @ 105°C	—	84.95	111.15	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	2.68	4.22	µA	
	• @ 70°C	—	8.8	10.74	µA	
	• @ 105°C	—	37.28	43.61	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	2.46	4.02	µA	
	• @ 70°C	—	7.04	8.99	µA	
	• @ 105°C	—	30.68	37.04	µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V					6
	• @ –40 to 25°C	—	0.89	1.10	µA	
	• @ 70°C	—	1.28	1.85	µA	
	• @ 105°C	—	3.10	4.30	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus, 30 MHz FlexBus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus, 30 MHz FlexBus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz FlexBus and flash clock. MCG configured for FEI mode.

5. 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
6. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies. MCG in PEE mode at greater than 100 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

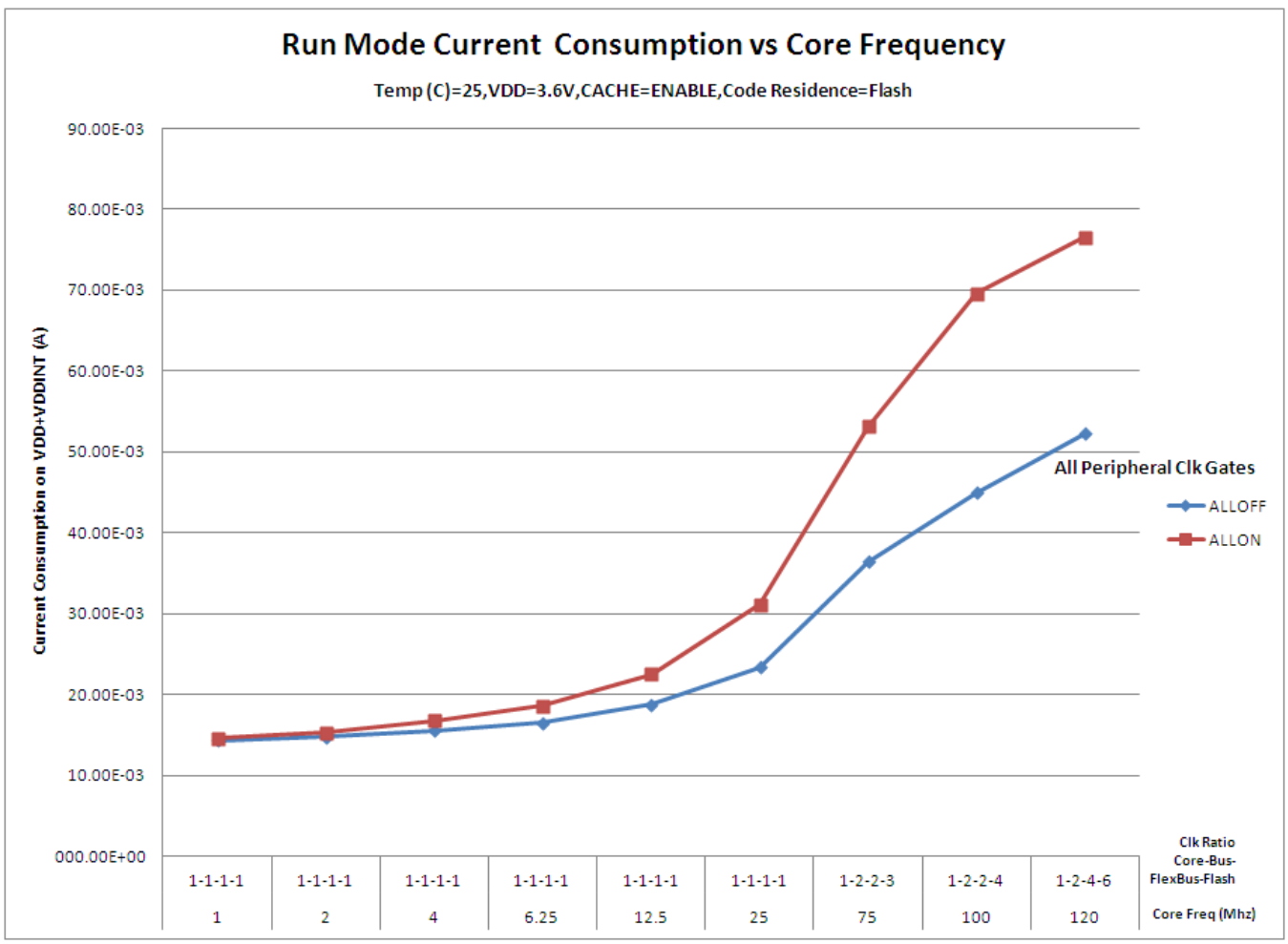

Figure 3. Run mode supply current vs. core frequency

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
t_{io50}	Port rise and fall time (low drive strength)				7
	• Slew disabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	18	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	9	ns	—
	• Slew enabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	48	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	24	ns	—
t_{io60}	Port rise and fall time (high drive strength)				6
	• Slew disabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	6	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	3	ns	—
	• Slew enabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	28	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	14	ns	—
t_{io60}	Port rise and fall time (low drive strength)				7
	• Slew disabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	18	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	6	ns	—
	• Slew enabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	48	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	24	ns	—

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load
6. 25 pF load
7. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature[1]	–40	105	°C

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA}$ x chip power dissipation

5.4.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	50	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	30	°C/W	1, 2, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	36	41	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	30	27	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	17	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	10	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	6

NOTES:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug trace timing specifications

Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns

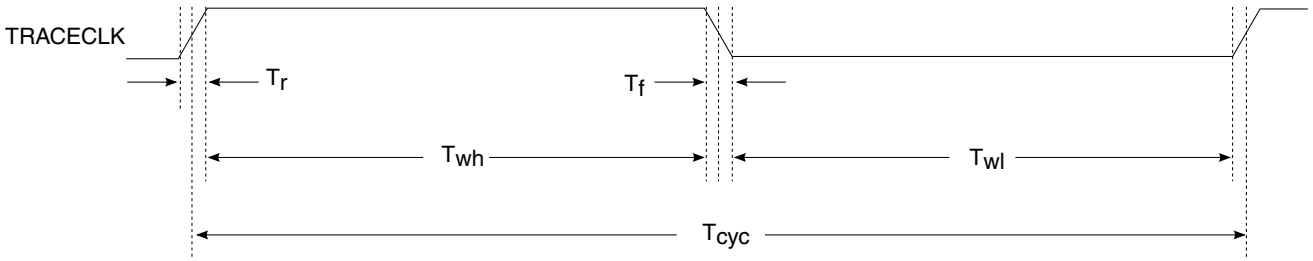

Figure 5. TRACE_CLKOUT specifications

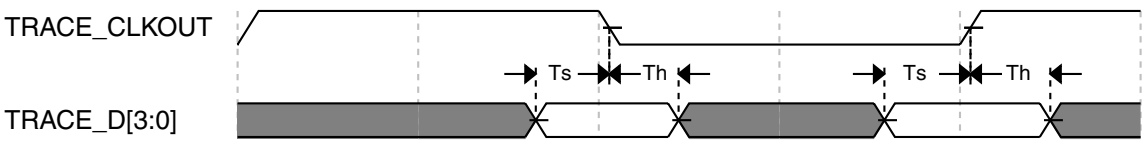

Figure 6. Trace data specifications

6.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.4	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
PLL0,1							
f_{pll_ref}	PLL reference frequency range		8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency		180	—	360	MHz	
f_{vcoclk}	PLL output frequency		90	—	180	MHz	
f_{vcoclk_90}	PLL quadrature output frequency		90	—	180	MHz	
I_{pll}	PLL0 operating current • VCO @ 184 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 23)		—	2.8	—	mA	
I_{pll}	PLL0 operating current • VCO @ 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)		—	4.7	—	mA	7
I_{pll}	PLL1 operating current • VCO @ 184 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 23)		—	2.3	—	mA	7
I_{pll}	PLL1 operating current • VCO @ 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)		—	3.6	—	mA	7
t_{pll_lock}	Lock detector detection time		—	—	100×10^{-6} + 1075(1/f_{pll_ref})	s	8
J_{cyc_pll}	PLL period jitter (RMS)						9

Table continues on the next page...

Table 29. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	3.0 4.4	5.2 6.2	7.3 9.5	MHz MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — — 	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current

Table continues on the next page...

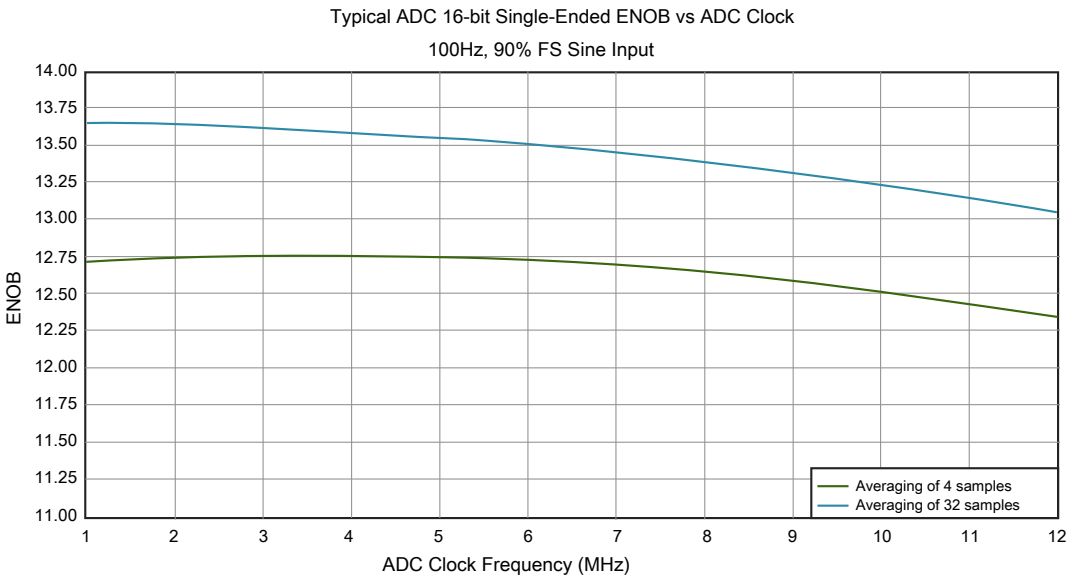

Figure 22. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.1.3 16-bit ADC with PGA operating conditions

Table 30. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V_{REFPGA}	PGA ref voltage		VREF_OUT	VREF_OUT	VREF_OUT	V	2, 3
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	
V_{CM}	Input Common Mode range		V_{SSA}	—	V_{DDA}	V	
R_{PGAD}	Differential input impedance	Gain = 1, 2, 4, 8	—	128	—	kΩ	IN+ to IN-[4]
		Gain = 16, 32	—	64	—		
		Gain = 64	—	32	—		
R_{AS}	Analog source resistance		—	100	—	Ω	5
T_S	ADC sampling time		1.25	—	—	μs	6
C_{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	18.484	—	450	Ksps	7
		16 bit modes	37.037	—	250	Ksps	8

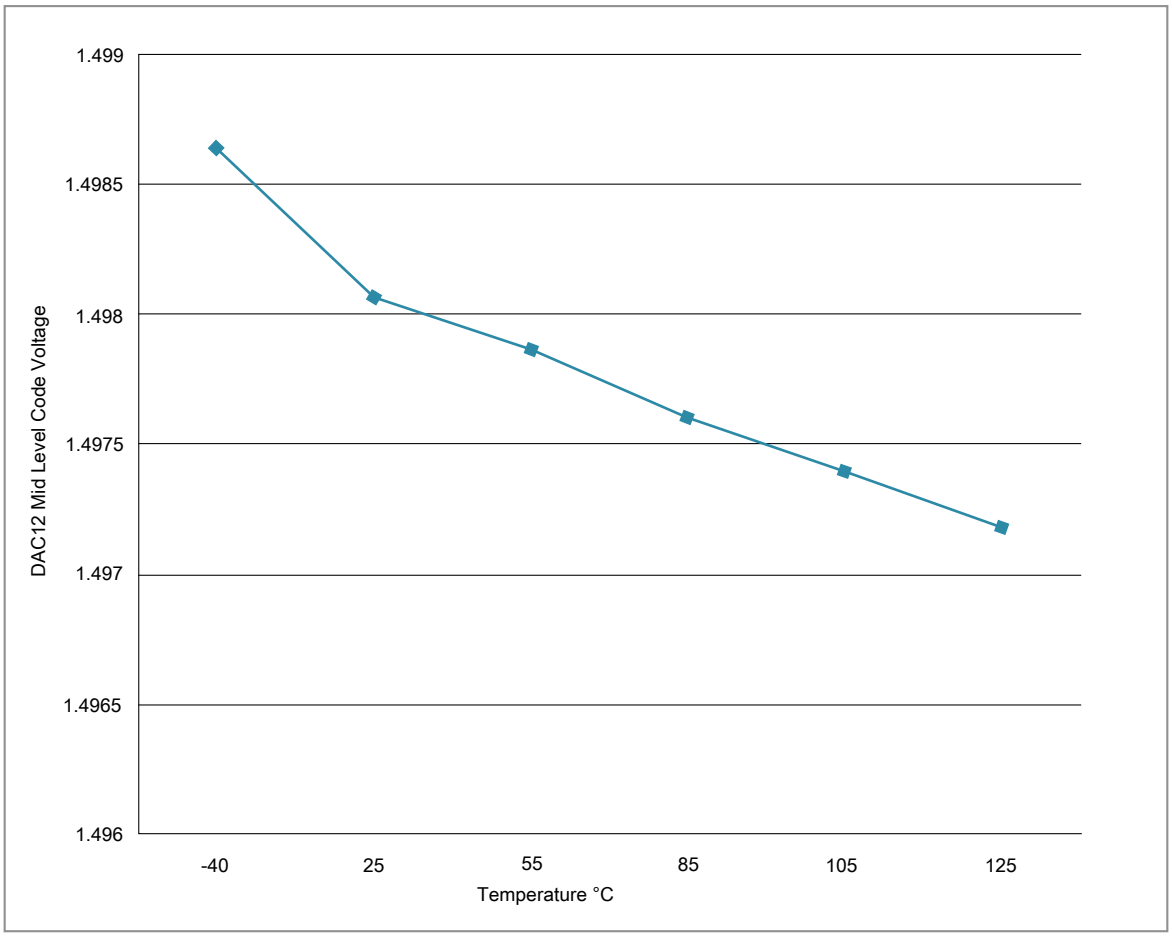

Figure 26. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 35. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

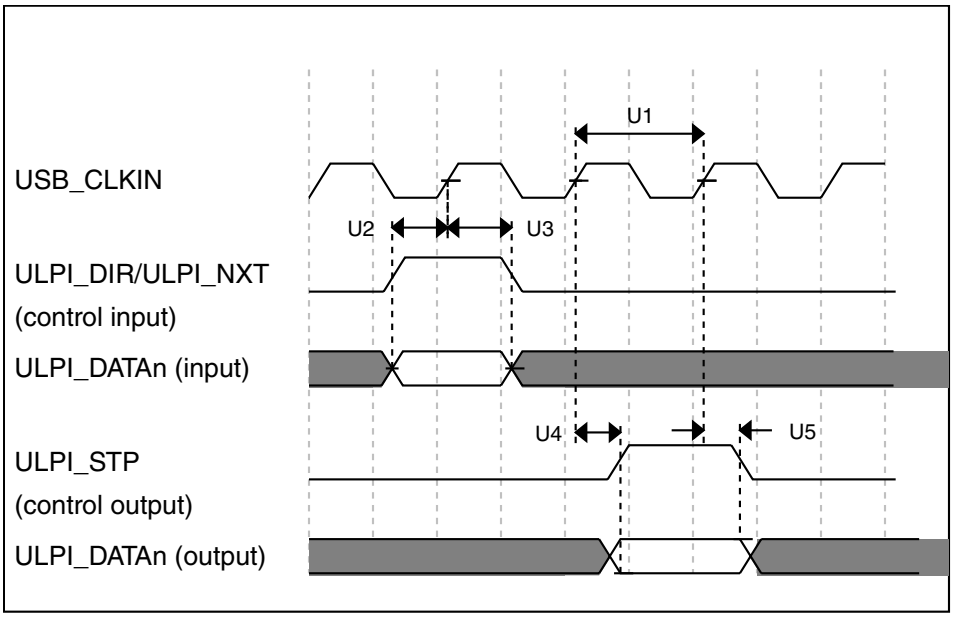

Figure 27. ULPI timing diagram

6.8.5 CAN switching specifications

See General switching specifications.

6.8.6 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 42. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	

Table continues on the next page...

Table 42. Master mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

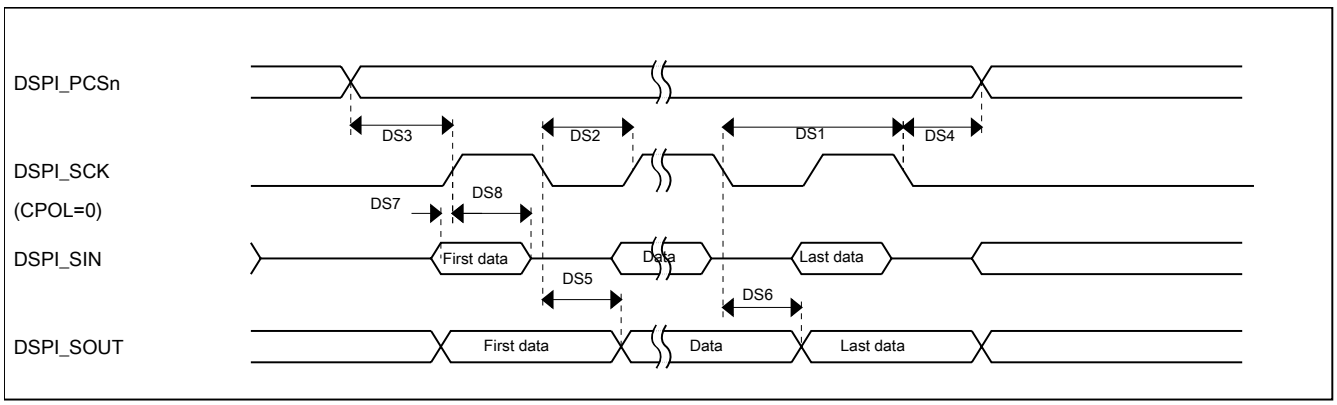

Figure 28. DSPI classic SPI timing — master mode

Table 43. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

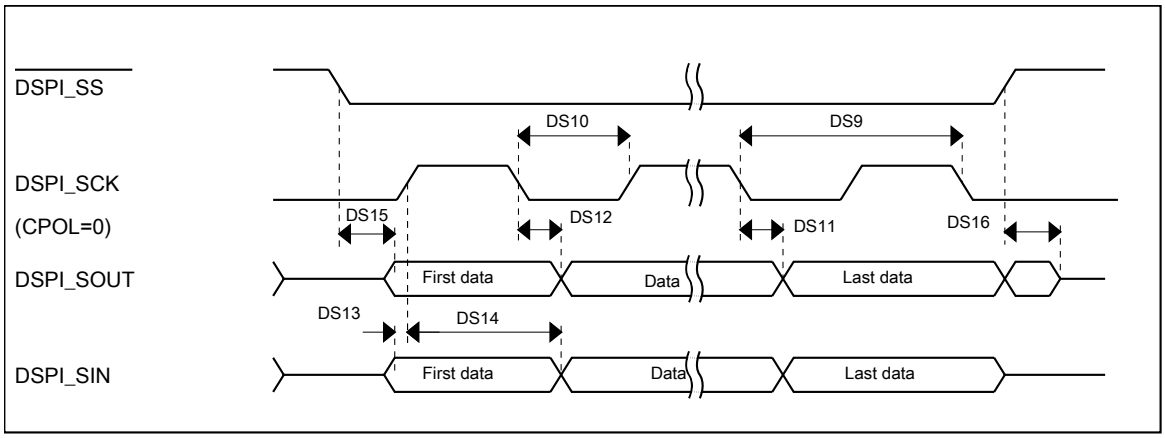

Figure 29. DSPI classic SPI timing — slave mode

6.8.7 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 44. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

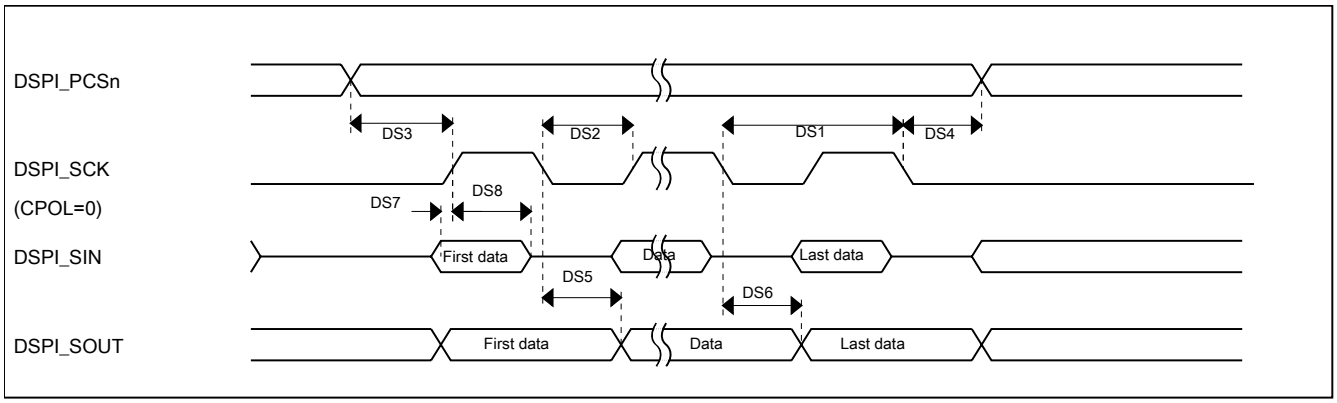

Figure 30. DSPI classic SPI timing — master mode

Table 45. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

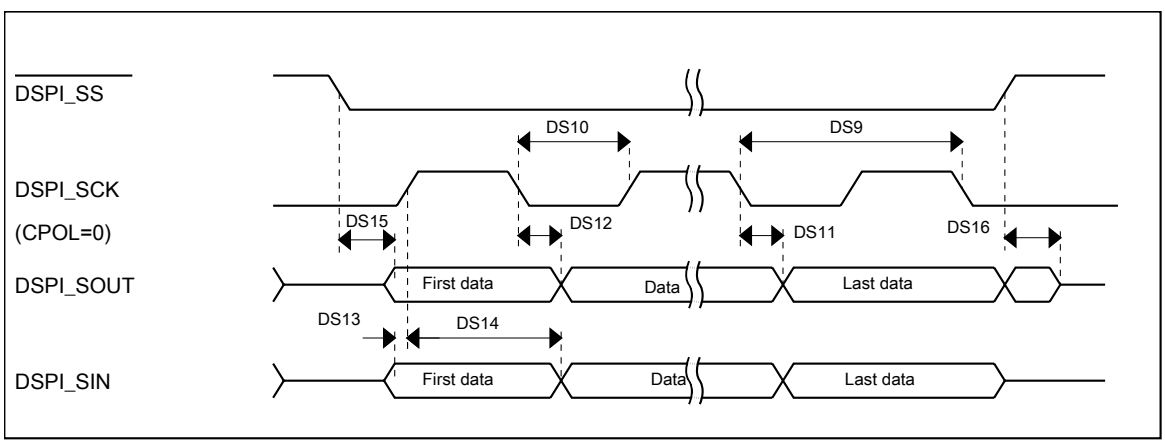

Figure 31. DSPI classic SPI timing — slave mode

Table 54. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

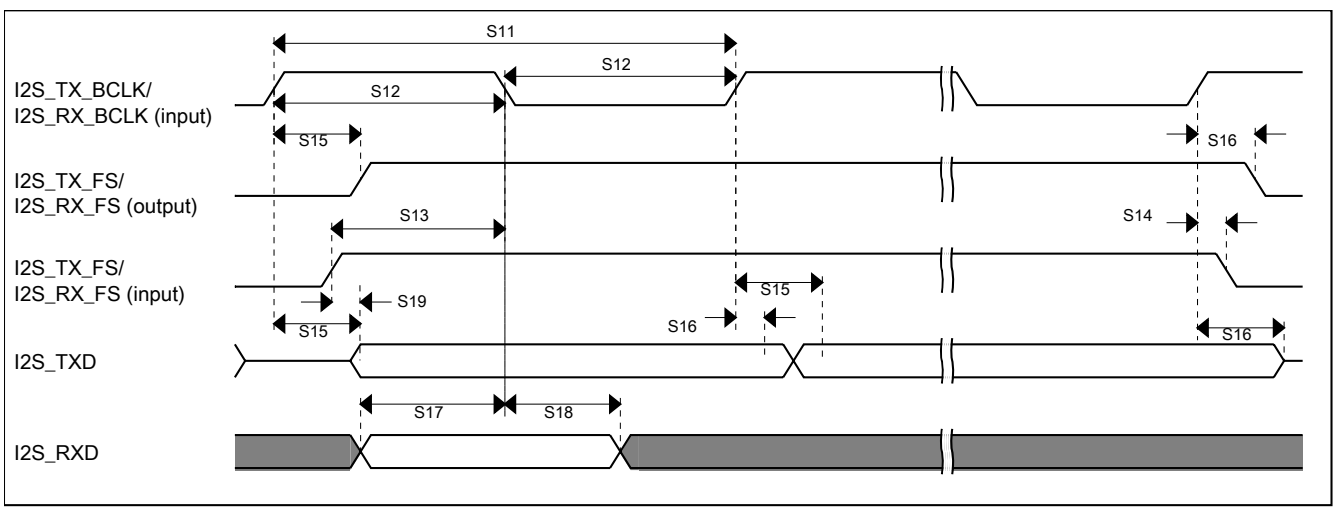

Figure 39. I2S/SAI timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 55. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f_{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4

Table continues on the next page...

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
71	G8	VSS	VSS	VSS								
72	M12	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
73	M11	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1		
74	L12	RESET_b	RESET_b	RESET_b								
75	K12	PTA24	CMP3_IN4	CMP3_IN4	PTA24	ULPI_DATA2				FB_A29		
76	J12	PTA25	CMP3_IN5	CMP3_IN5	PTA25	ULPI_DATA3				FB_A28		
77	J11	PTA26	ADC2_SE15	ADC2_SE15	PTA26	ULPI_DATA4				FB_A27		
78	J10	PTA27	ADC2_SE14	ADC2_SE14	PTA27	ULPI_DATA5				FB_A26		
79	H12	PTA28	ADC2_SE13	ADC2_SE13	PTA28	ULPI_DATA6				FB_A25		
80	H11	PTA29	ADC2_SE12	ADC2_SE12	PTA29	ULPI_DATA7				FB_A24		
81	H10	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ ADC2_SE8/ ADC3_SE8/ TSI0_CH0	ADC0_SE8/ ADC1_SE8/ ADC2_SE8/ ADC3_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		
82	H9	PTB1	ADC0_SE9/ ADC1_SE9/ ADC2_SE9/ ADC3_SE9/ TSI0_CH6	ADC0_SE9/ ADC1_SE9/ ADC2_SE9/ ADC3_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB		
83	G12	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_ RTS_b			FTM0_FLT3		
84	G11	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_ CTS_b/ UART0_ COL_b			FTM0_FLT0		
85	G10	PTB4	ADC1_SE10	ADC1_SE10	PTB4					FTM1_FLT0		
86	G9	PTB5	ADC1_SE11	ADC1_SE11	PTB5					FTM2_FLT0		
87	F12	PTB6	ADC1_SE12	ADC1_SE12	PTB6				FB_AD23			
88	F11	PTB7	ADC1_SE13	ADC1_SE13	PTB7				FB_AD22			
89	F10	PTB8	DISABLED		PTB8		UART3_ RTS_b		FB_AD21			
90	F9	PTB9	DISABLED		PTB9	SPI1_PCS1	UART3_ CTS_b		FB_AD20			
91	E12	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX	I2S1_TX_ BCLK	FB_AD19	FTM0_FLT1		
92	E11	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX	I2S1_TX_FS	FB_AD18	FTM0_FLT2		
93	H7	VSS	VSS	VSS								
94	F5	VDD	VDD	VDD								
95	E10	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX	I2S1_TXD0	FB_AD17	EWM_IN		
96	E9	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX	I2S1_TXD1	FB_AD16	EWM_OUT_b		
97	D12	PTB18	TSI0_CH11	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK	FB_AD15	FTM2_QD_ PHA		
98	D11	PTB19	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_ PHB		

Table 57. Revision History (continued)

Rev. No.	Date	Substantial Changes
4	10/2012	Replaced TBDs throughout.
5	10/2013	Changes for 4N96B mask set: • Min VDD operating requirement specification updated to support operation down to 1.71V. New specifications: • Updated Vdd_ddr min specification. • Added Vodpu specification. • Removed Ioz, Ioz_ddr, and Ioz_tamper Hi-Z leakage specfications. They have been replaced by new Iina, Iind, and Zind specifications. • Fpll_ref_acc specification has been added. • I^2C module was previously covered by the general switching specifications. To provide more detail on I^2C operation a dedicated Inter-Integrated Circuit Interface (I^2C) timing section has been added. Modified specifications: • Vref_ddr max spec has been updated. • Tpor spec has been split into two specifications based on VDD slew rate. • Trd1allx and Trd1alln max have been updated. • 16-bit ADC Temp sensor slope and Temp sensor voltage (Vtemp25) have been modified. The typical values that were listed previously have been updated, and min and max specifications have been added. Corrections: • Some versions of the datasheets listed incorrect clock mode information in the "Diagram: Typical IDD_RUN operating behavior section." These errors have been corrected. • Fintf_ft specification was previously shown as a max value. It has been corrected to be shown as a typical value as originally intended. • Corrected DDR write and read timing diagrams to show the correct location of the Tcmv specification. • SDHC peripheral 50MHz high speed mode options were left out of the last datasheet. These have been added to the SDHC specifications section.
6	09/2015	• Updated the footnotes of Thermal Attributes table • Removed Power Sequencing section • Added footnote to ambient temperature specification of Thermal Operating requirements • Removed "USB HS/LS/FS on-the-go controller with on-chip high speed transceiver" from features section • Updated Terminology and guidelines section • Updated the footnotes and the values of Power consumption operating behaviors table • Added Notes in USB electrical specification section • Updated I2C timing table

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number K20P144M120SF3
Revision 6, 09/2015