NXP USA Inc. - PK20FX512VLQ12 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 45x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pk20fx512vlq12

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4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage[1]	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL0/XTAL0, and EXTAL1/XTAL1) [2]	–0.3	5.5	V
V_{AIO}	Analog[3], $\overline{\text{RESET}}$, EXTAL0/XTAL0, and EXTAL1/XTAL1 input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB1_DP}	USB1_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{USB1_DM}	USB1_DM input voltage	–0.3	3.63	V
VREGIN	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. It applies for all port pins.

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Output high voltage — low drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	V_{DD} – 0.5	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
I_{OHT_io60}	Output high current total for fast digital ports	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 5 mA	—	—	0.5	V	
	Output low voltage — low drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1 mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{OLT_io60}	Output low current total for fast digital ports	—	—	100	mA	
I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs • V_{SS} ≤ V_{IN} ≤ V_{DD}					1, 2
	• All pins except EXTAL32, XTAL32, EXTAL, XTAL	—	0.002	0.5	μA	
	• EXTAL (PTA18) and XTAL (PTA19)	—	0.004	1.5	μA	
	• EXTAL32, XTAL32	—	0.075	10	μA	
I_{IND}	Input leakage current, digital pins • V_{SS} ≤ V_{IN} ≤ V_{IL}					2, 3
	• All digital pins	—	0.002	0.5	μA	
	• V_{IN} = V_{DD}					
	• All digital pins except PTD7	—	0.002	0.5	μA	
	• PTD7	—	0.004	1	μA	
I_{IND}	Input leakage current, digital pins • V_{IL} < V_{IN} < V_{DD}					2, 3, 4
	• V_{DD} = 3.6 V	—	18	26	μA	
	• V_{DD} = 3.0 V	—	12	19	μA	
	• V_{DD} = 2.5 V	—	8	13	μA	
	• V_{DD} = 1.7 V	—	3	6	μA	
I_{IND}	Input leakage current, digital pins					2, 3
	• V_{DD} < V_{IN} < 5.5 V	—	1	50	μA	
Z_{IND}	Input impedance examples, digital pins	—	—	48	kΩ	2, 5

Table continues on the next page...

5. 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
6. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies. MCG in PEE mode at greater than 100 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

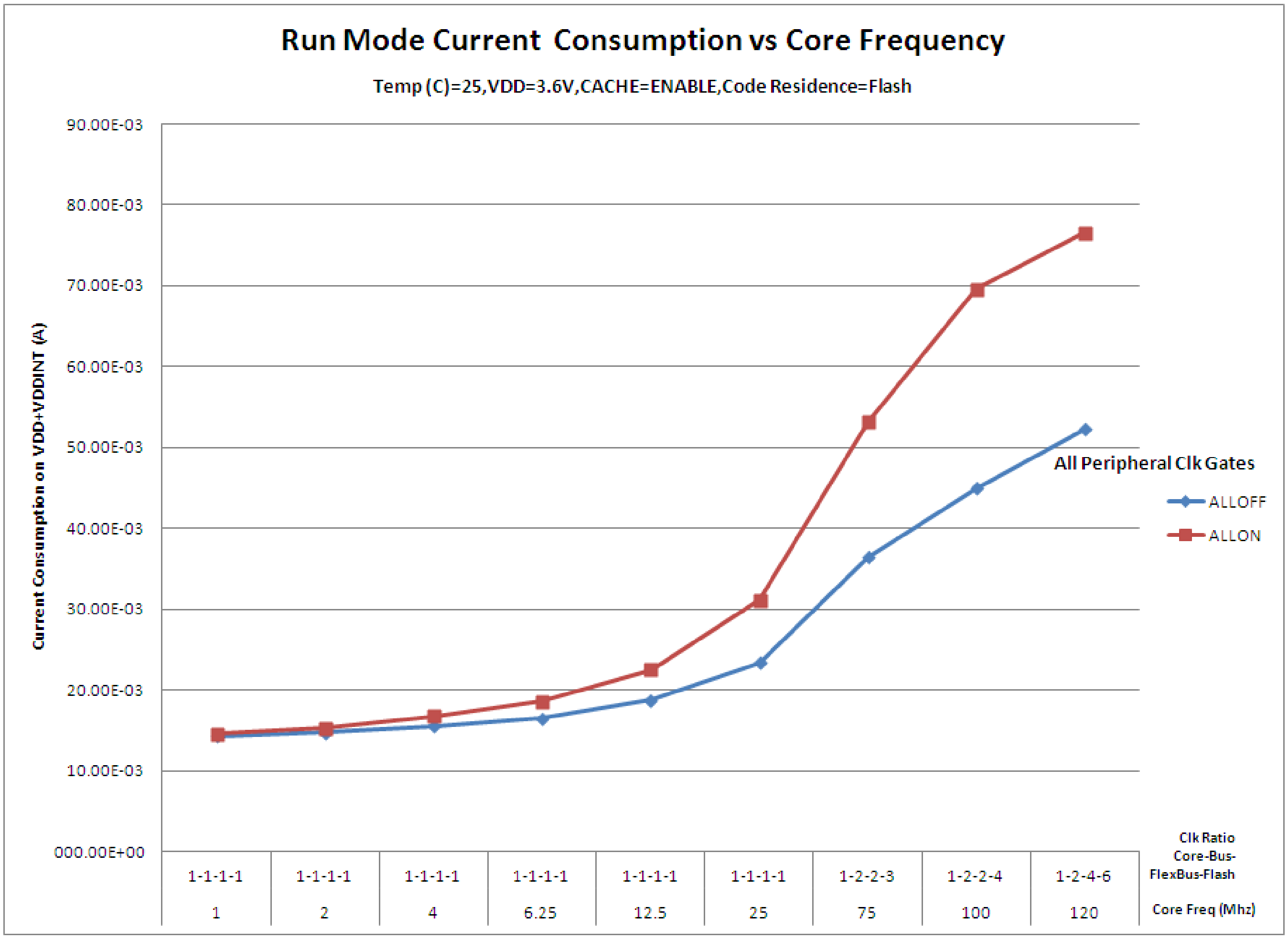


Figure 3. Run mode supply current vs. core frequency

Table 15. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• f_{VCO} = 180 MHz	—	100	—	ps	
	• f_{VCO} = 360 MHz	—	75	—	ps	
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS)					10
	• f_{VCO} = 180 MHz	—	600	—	ps	
	• f_{VCO} = 360 MHz	—	300	—	ps	

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. Accumulated jitter depends on VCO frequency and VDIV.

6.3.2 Oscillator electrical specifications

6.3.2.1 Oscillator DC electrical specifications

Table 16. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
		—	400	—	μA	

Table continues on the next page...

6.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	1
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	60	MHz	2, 3
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	4, 5
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	500	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Frequencies less than 8 MHz are not in the PLL range.
2. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
3. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz oscillator electrical characteristics

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk128k}$	• 128 KB data flash	—	—	0.5	ms	
$t_{rd1blk256k}$	• 256 KB program flash 256 KB data flash	—	—	1.0	ms	
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	μs	1
t_{pgmchk}	Program Check execution time	—	—	80	μs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	μs	1
t_{pgm8}	Program Phrase execution time	—	70	150	μs	
	Erase Flash Block execution time					2
$t_{ersblk128k}$	• 128 KB data flash	—	110	925	ms	
$t_{ersblk256k}$	• 256 KB program flash 256 KB data flash	—	220	1850	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec4k}$	Program Section execution time (4KB flash)	—	20	—	ms	
	Read 1s All Blocks execution time					
$t_{rd1allx}$	• FlexNVM devices	—	—	3.4	ms	
$t_{rd1alln}$	• Program flash only devices	—	—	3.4	ms	
t_{rdonce}	Read Once execution time	—	—	30	μs	1
$t_{pgmonce}$	Program Once execution time	—	70	—	μs	
t_{ersall}	Erase All Blocks execution time	—	650	5600	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	μs	
$t_{swapx02}$	• control code 0x02	—	70	150	μs	
$t_{swapx04}$	• control code 0x04	—	70	150	μs	
$t_{swapx08}$	• control code 0x08	—	—	30	μs	
	Program Partition for EEPROM execution time					
$t_{pgmpart64k}$	• 64 KB EEPROM backup	—	235	—	ms	
$t_{pgmpart256k}$	• 256 KB EEPROM backup	—	240	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	205	—	μs	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.6	2.5	ms	
$t_{setram128k}$	• 128 KB EEPROM backup	—	2.7	3.8	ms	
$t_{setram256k}$	• 256 KB EEPROM backup	—	4.8	6.2	ms	
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	140	225	μs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b64k}$		—	400	1700	μs	

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{eewr8b128k}$	• 64 KB EEPROM backup	—	450	1800	μs	
$t_{eewr8b256k}$	• 128 KB EEPROM backup	—	525	2000	μs	
	• 256 KB EEPROM backup					
$t_{eewr16bers}$	16-bit write to erased FlexRAM location execution time	—	140	225	μs	
	16-bit write to FlexRAM execution time:					
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	400	1700	μs	
$t_{eewr16b128k}$	• 128 KB EEPROM backup	—	450	1800	μs	
$t_{eewr16b256k}$	• 256 KB EEPROM backup	—	525	2000	μs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	180	275	μs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	475	1850	μs	
$t_{eewr32b128k}$	• 128 KB EEPROM backup	—	525	2000	μs	
$t_{eewr32b256k}$	• 256 KB EEPROM backup	—	600	2200	μs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	

Table continues on the next page...

- T_H is the flash clock high time and
- T_L is flash clock low time,

which are defined as:

$$T_{NFC} = T_L + T_H = \frac{T_{\text{input clock}}}{\text{SCALER}}$$

The SCALER value is derived from the fractional divider specified in the SIM's CLKDIV4 register:

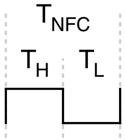
$$\text{SCALER} = \frac{\text{SIM\_CLKDIV4[NFCFRAC]} + 1}{\text{SIM\_CLKDIV4[NFCDIV]} + 1}$$

In case the reciprocal of SCALER is an integer, the duty cycle of NFC clock is 50%, means $T_H = T_L$. In case the reciprocal of SCALER is not an integer:

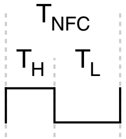
$$T_L = (1 + \text{SCALER} / 2) \times \frac{T_{NFC}}{2}$$

$$T_H = (1 - \text{SCALER} / 2) \times \frac{T_{NFC}}{2}$$

For example, if SCALER is 0.2, then $T_H = T_L = T_{NFC}/2$.



However, if SCALER is 0.667, then $T_L = 2/3 \times T_{NFC}$ and $T_H = 1/3 \times T_{NFC}$.



NOTE

The reciprocal of SCALER must be a multiple of 0.5. For example, 1, 1.5, 2, 2.5, etc.

Table 25. NFC specifications

Num	Description	Min.	Max.	Unit
t_{CLS}	NFC_CLE setup time	$2T_H + T_L - 1$	—	ns
t_{CLH}	NFC_CLE hold time	$T_H + T_L - 1$	—	ns
t_{CS}	$\overline{\text{NFC\_CEn}}$ setup time	$2T_H + T_L - 1$	—	ns
t_{CH}	$\overline{\text{NFC\_CEn}}$ hold time	$T_H + T_L$	—	ns

Table continues on the next page...

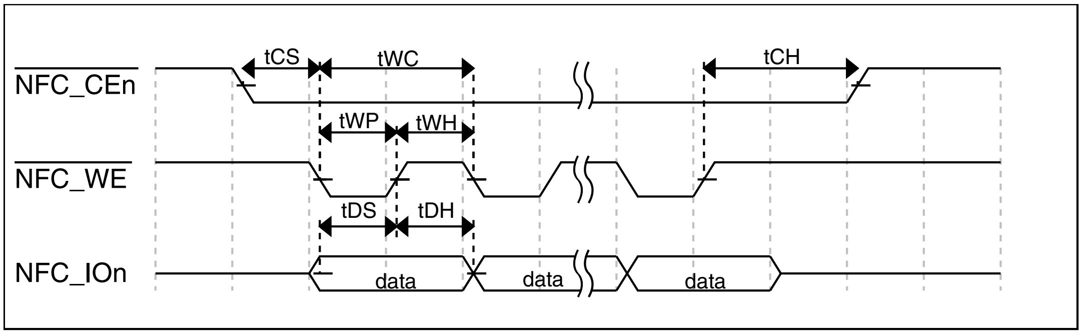


Figure 15. Write data latch cycle timing

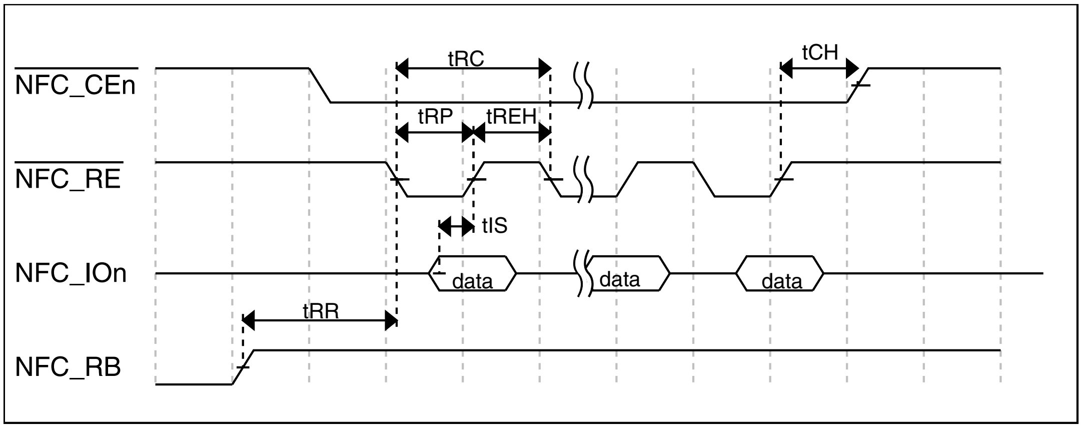


Figure 16. Read data latch cycle timing in non-fast mode

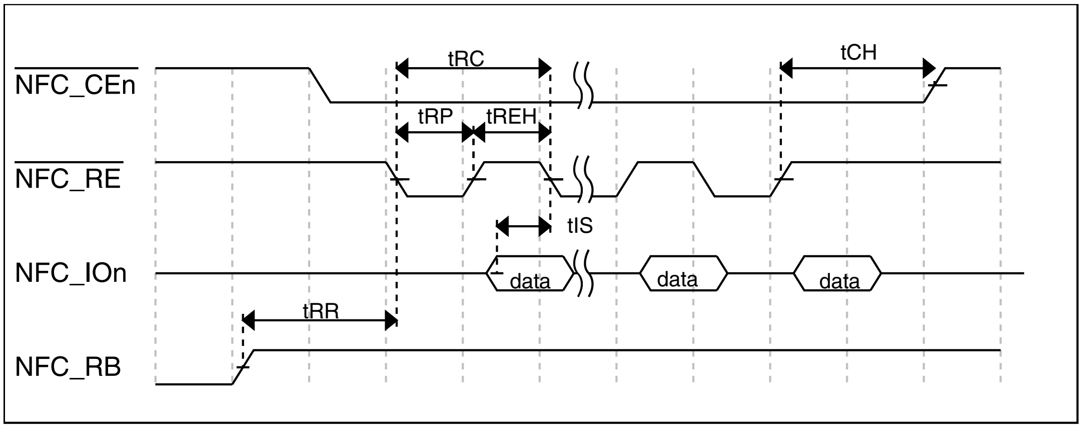


Figure 17. Read data latch cycle timing in fast mode

6.4.4 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 26. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and FB_TA input setup	8.5	—	ns	2
FB5	Data and FB_TA input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

Table 27. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and FB_TA input setup	13.7	—	ns	2
FB5	Data and FB_TA input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

Table 29. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	3.0 4.4	5.2 6.2	7.3 9.5	MHz MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	82 78	95 90	— —	dB dB	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current

Table continues on the next page...

Table 49. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

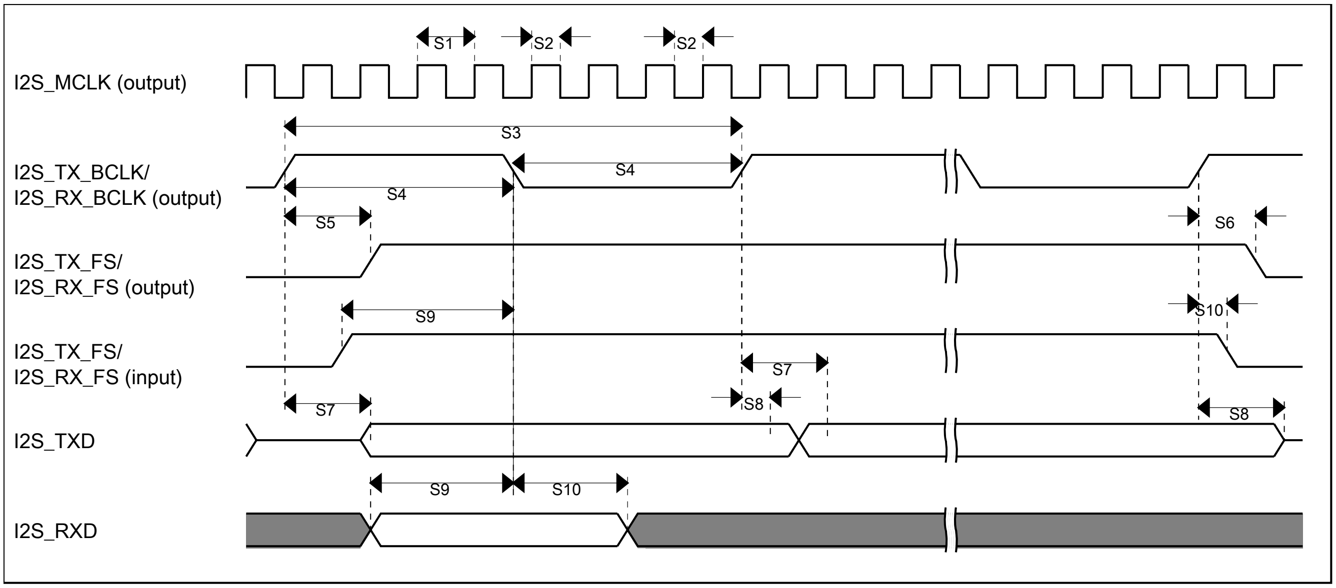


Figure 34. I2S/SAI timing — master modes

Table 50. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period

Table continues on the next page...

Table 54. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

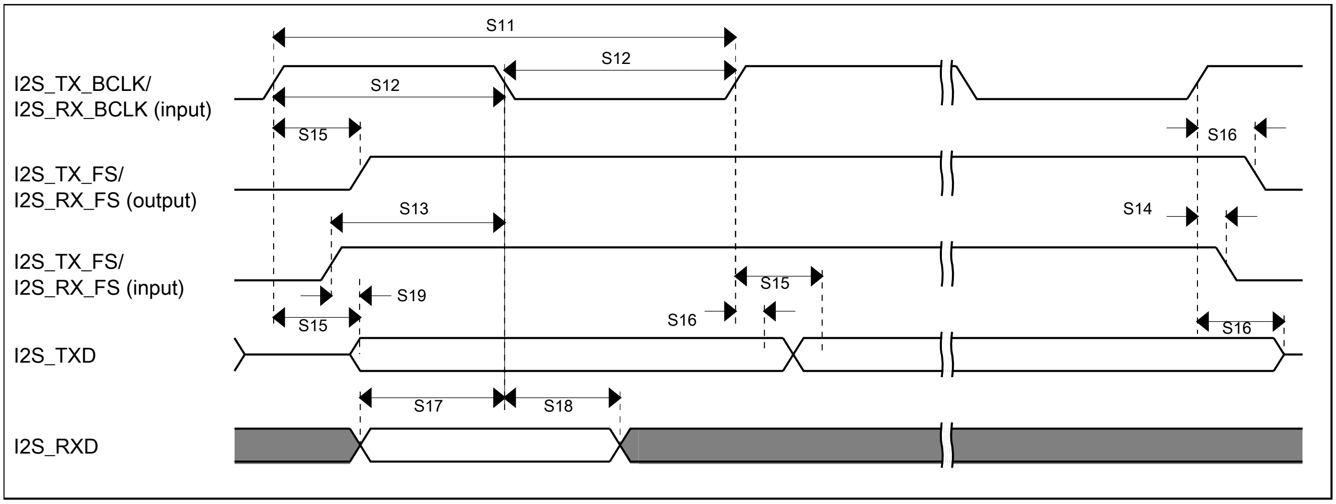


Figure 39. I2S/SAI timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 55. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f_{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4

Table continues on the next page...

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
144-pin MAPBGA	98ASA00222D

8 Pinout

8.1 Pins with active pull control after reset

The following pins are actively pulled up or down after reset:

Table 56. Pins with active pull control after reset

Pin	Active pull direction after reset
PTA0	pulldown
PTA1	pullup
PTA3	pullup
PTA4	pullup
RESET_b	pullup

8.2 K20 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
—	L5	RTC_ WAKEUP_B	RTC_ WAKEUP_B	RTC_ WAKEUP_B								
—	M5	NC	NC	NC								
—	A10	NC	NC	NC								
—	B10	NC	NC	NC								

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
48	J4	PTE27	ADC3_SE4b	ADC3_SE4b	PTE27		UART4_RTS_b	I2S1_MCLK				
49	H4	PTE28	ADC3_SE7a	ADC3_SE7a	PTE28							
50	J5	PTA0	JTAG_TCLK/SWD_CLK/EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_b/UART0_COL_b	FTM0_CH5				JTAG_TCLK/SWD_CLK	EZP_CLK
51	J6	PTA1	JTAG_TDI/EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/TRACE_SWO/EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/TRACE_SWO	EZP_DO
53	K7	PTA3	JTAG_TMS/SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/SWD_DIO	
54	L7	PTA4/LLWU_P3	NMI_b/EZP_CS_b	TSI0_CH5	PTA4/LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
55	M8	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2		CMP2_OUT	I2S0_TX_BCLK	JTAG_TRST_b	
56	E7	VDD	VDD	VDD								
57	G7	VSS	VSS	VSS								
58	J7	PTA6	ADC3_SE6a	ADC3_SE6a	PTA6	ULPI_CLK	FTM0_CH3	I2S1_RXD0	CLKOUT		TRACE_CLKOUT	
59	J8	PTA7	ADC0_SE10	ADC0_SE10	PTA7	ULPI_DIR	FTM0_CH4	I2S1_RX_BCLK			TRACE_D3	
60	K8	PTA8	ADC0_SE11	ADC0_SE11	PTA8	ULPI_NXT	FTM1_CH0	I2S1_RX_FS		FTM1_QD_PHA	TRACE_D2	
61	L8	PTA9	ADC3_SE5a	ADC3_SE5a	PTA9	ULPI_STP	FTM1_CH1			FTM1_QD_PHB	TRACE_D1	
62	M9	PTA10	ADC3_SE4a	ADC3_SE4a	PTA10	ULPI_DATA0	FTM2_CH0			FTM2_QD_PHA	TRACE_D0	
63	L9	PTA11	ADC3_SE15	ADC3_SE15	PTA11	ULPI_DATA1	FTM2_CH1			FTM2_QD_PHB		
64	K9	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0			I2S0_TXD0	FTM1_QD_PHA	
65	J9	PTA13/LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/LLWU_P4	CAN0_RX	FTM1_CH1			I2S0_TX_FS	FTM1_QD_PHB	
66	L10	PTA14	CMP3_IN0	CMP3_IN0	PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_BCLK	I2S0_TXD1	
67	L11	PTA15	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
68	K10	PTA16	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_CTS_b/UART0_COL_b			I2S0_RX_FS	I2S0_RXD1	
69	K11	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b			I2S0_MCLK		
70	E8	VDD	VDD	VDD								

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
122	—	VDD	VDD	VDD								
123	A6	PTC16	DISABLED		PTC16	CAN1_RX	UART3_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b	NFC_RB		
124	D5	PTC17	DISABLED		PTC17	CAN1_TX	UART3_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b	NFC_CE0_b		
125	C5	PTC18	DISABLED		PTC18		UART3_RTS_b		FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b	NFC_CE1_b		
126	B5	PTC19	DISABLED		PTC19		UART3_CTS_b		FB_CS3_b/ FB_BE7_0_b	FB_TA_b		
127	A5	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b	I2S1_RXD1		
128	D4	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b	FTM3_CH1	FB_CS0_b	I2S1_RXD0		
129	C4	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4	I2S1_RX_FS		
130	B4	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3	I2S1_RX_BCLK		
131	A4	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2/ NFC_DATA1	EWM_IN		
132	A3	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5	FB_AD1/ NFC_DATA0	EWM_OUT_b		
133	A2	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
134	M10	VSS	VSS	VSS								
135	F8	VDD	VDD	VDD								
136	A1	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
137	C9	PTD8	DISABLED		PTD8	I2C0_SCL	UART5_RX			FB_A16/ NFC_CLE		
138	B9	PTD9	DISABLED		PTD9	I2C0_SDA	UART5_TX			FB_A17/ NFC_ALE		
139	B3	PTD10	DISABLED		PTD10		UART5_RTS_b			FB_A18/ NFC_RE		
140	B2	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_CTS_b	SDHC0_CLKIN		FB_A19		
141	B1	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	SDHC0_D4		FB_A20		
142	C3	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21		
143	C2	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22		
144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		

8.3 K20 pinouts

The figure below shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

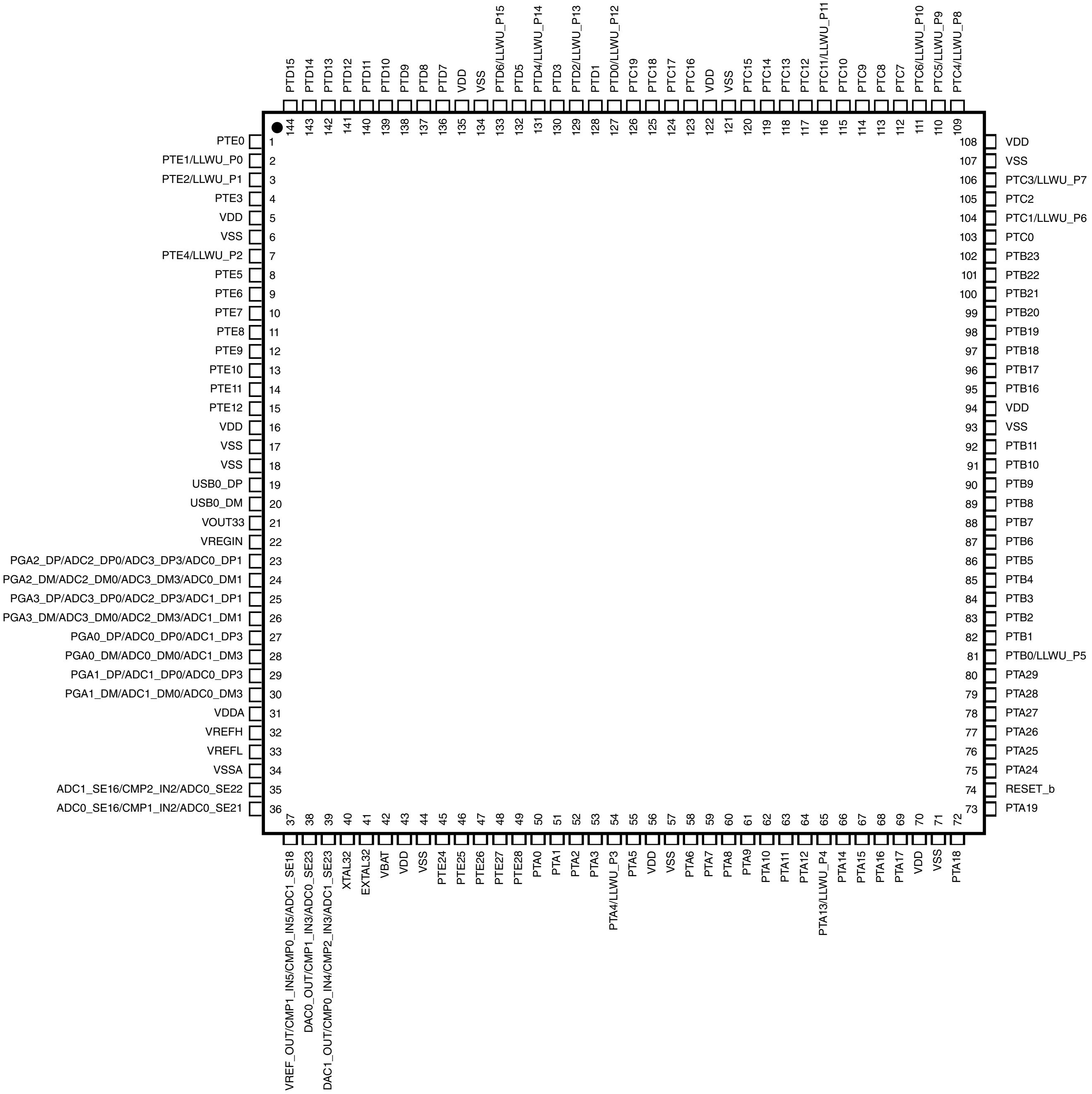


Figure 40. K20 144 LQFP Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	
A	PTD7	PTD6/ LLWU_P15	PTD5	PTD4/ LLWU_P14	PTD0/ LLWU_P12	PTC16	PTC12	PTC8	PTC4/ LLWU_P8	NC	PTC3/ LLWU_P7	PTC2	A
B	PTD12	PTD11	PTD10	PTD3	PTC19	PTC15	PTC11/ LLWU_P11	PTC7	PTD9	NC	PTC1/ LLWU_P6	PTC0	B
C	PTD15	PTD14	PTD13	PTD2/ LLWU_P13	PTC18	PTC14	PTC10	PTC6/ LLWU_P10	PTD8	NC	PTB23	PTB22	C
D	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	PTD1	PTC17	PTC13	PTC9	PTC5/ LLWU_P9	PTB21	PTB20	PTB19	PTB18	D
E	PTE6	PTE5	PTE4/ LLWU_P2	PTE3	VDD	VDD	VDD	VDD	PTB17	PTB16	PTB11	PTB10	E
F	PTE10	PTE9	PTE8	PTE7	VDD	VSS	VSS	VDD	PTB9	PTB8	PTB7	PTB6	F
G	VOUT33	VREGIN	PTE12	PTE11	VREFH	VREFL	VSS	VSS	PTB5	PTB4	PTB3	PTB2	G
H	USB0_DP	USB0_DM	VSS	PTE28	VDDA	VSSA	VSS	VSS	PTB1	PTB0/ LLWU_P5	PTA29	PTA28	H
J	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	PTE27	PTA0	PTA1	PTA6	PTA7	PTA13/ LLWU_P4	PTA27	PTA26	PTA25	J
K	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	PTE26	PTE25	PTA2	PTA3	PTA8	PTA12	PTA16	PTA17	PTA24	K
L	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	RTC_ WAKEUP_B	VBAT	PTA4/ LLWU_P3	PTA9	PTA11	PTA14	PTA15	RESET_b	L
M	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	PTE24	NC	EXTAL32	XTAL32	PTA5	PTA10	VSS	PTA19	PTA18	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 41. K20 144 MAPBGA Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 57. Revision History

Rev. No.	Date	Substantial Changes
3	3/2012	Initial public release

Table continues on the next page...

Table 57. Revision History (continued)

Rev. No.	Date	Substantial Changes
4	10/2012	Replaced TBDs throughout.
5	10/2013	Changes for 4N96B mask set: • Min VDD operating requirement specification updated to support operation down to 1.71V. New specifications: • Updated Vdd_ddr min specification. • Added Vodpu specification. • Removed Ioz, Ioz_ddr, and Ioz_tamper Hi-Z leakage specfications. They have been replaced by new Iina, Iind, and Zind specifications. • Fpll_ref_acc specification has been added. • I^2C module was previously covered by the general switching specifications. To provide more detail on I^2C operation a dedicated Inter-Integrated Circuit Interface (I^2C) timing section has been added. Modified specifications: • Vref_ddr max spec has been updated. • Tpor spec has been split into two specifications based on VDD slew rate. • Trd1allx and Trd1alln max have been updated. • 16-bit ADC Temp sensor slope and Temp sensor voltage (Vtemp25) have been modified. The typical values that were listed previously have been updated, and min and max specifications have been added. Corrections: • Some versions of the datasheets listed incorrect clock mode information in the "Diagram: Typical IDD_RUN operating behavior section." These errors have been corrected. • Fintf_ft specification was previously shown as a max value. It has been corrected to be shown as a typical value as originally intended. • Corrected DDR write and read timing diagrams to show the correct location of the Tcmv specification. • SDHC peripheral 50MHz high speed mode options were left out of the last datasheet. These have been added to the SDHC specifications section.
6	09/2015	• Updated the footnotes of Thermal Attributes table • Removed Power Sequencing section • Added footnote to ambient temperature specification of Thermal Operating requirements • Removed "USB HS/LS/FS on-the-go controller with on-chip high speed transceiver" from features section • Updated Terminology and guidelines section • Updated the footnotes and the values of Power consumption operating behaviors table • Added Notes in USB electrical specification section • Updated I2C timing table