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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8241lvr200d

- Write buffering for PCI and processor accesses
- Normal parity, read-modify-write (RMW), or ECC
- Data-path buffering between memory interface and processor
- Low-voltage TTL logic (LVTTL) interfaces
- 272 Mbytes of base and extended ROM/Flash/PortX space
- Base ROM space for 8-bit data path or same size as the SDRAM data path (32- or 64-bit)
- Extended ROM space for 8-, 16-, 32-bit gathering data path, 32- or 64-bit (wide) data path
- PortX: 8-, 16-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing, data ready input signal ($\overline{\text{DRDY}}$), and 4 chip selects

— 32-bit PCI interface
- Operates up to 66 MHz
- PCI 2.2-compatible
- PCI 5.0-V tolerance
- Dual address cycle (DAC) for 64-bit PCI addressing (master only)
- PCI locked accesses to memory
- Accesses to PCI memory, I/O, and configuration spaces
- Selectable big- or little endian operation
- Store gathering of processor-to-PCI write and PCI-to-memory write accesses
- Memory prefetching of PCI read accesses
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)
- PCI agent mode capability
- Address translation with two inbound and outbound units (ATU)
- Internal configuration registers accessible from PCI

— Two-channel integrated DMA controller (writes to ROM/PortX not supported)
- Direct mode or chaining mode (automatic linking of DMA transfers)
- Scatter gathering—read or write discontinuous memory
- 64-byte transfer queue per channel
- Interrupt on completed segment, chain, and error
- Local-to-local memory
- PCI-to-PCI memory
- Local-to-PCI memory
- PCI memory-to-local memory

— Message unit
- Two doorbell registers
- Two inbound and two outbound messaging registers
- I_2O message interface

Table 3. DC Electrical Specifications (continued)

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Capacitance	V_{in} = 0 V, f = 1 MHz	C_{in}	—	16.0	pF	

Notes:
1. See Table 16 for pins with internal pull-up resistors.
2. All grounded pins are connected together.
3. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} or both GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} must vary in the same direction.
4. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 16.

4.2.1 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 16. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8241 Output Pins [5, 6]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20 (default)	GV_{DD}_OV_{DD} = 3.3 V	36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)		89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) where table entry voltage = GV_{DD}_OV_{DD} – PCI V_{OH}.
2. For all others with GV_{DD}_ OV_{DD} = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = GV_{DD}_OV_{DD} – V_{OH}.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.
4. For all others with GV_{DD}_OV_{DD} = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4-V table entry.
5. See driver bit details for output driver control register (0x73) in the *MPC8245 Integrated Processor Reference Manual*.
6. See Chip Errata No. 19 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*.

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 through 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines,* for details on MPC8241 memory clock design.
7. Rise and fall times for the OSC_IN input are guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram, and Figure 7 through Figure 10 show the DLL locking range loop delay versus frequency of operation.

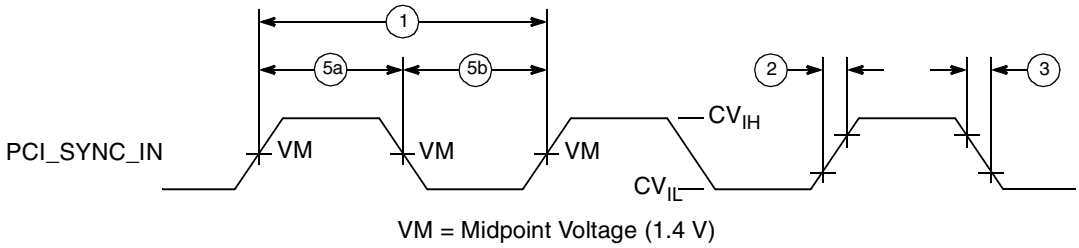


Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

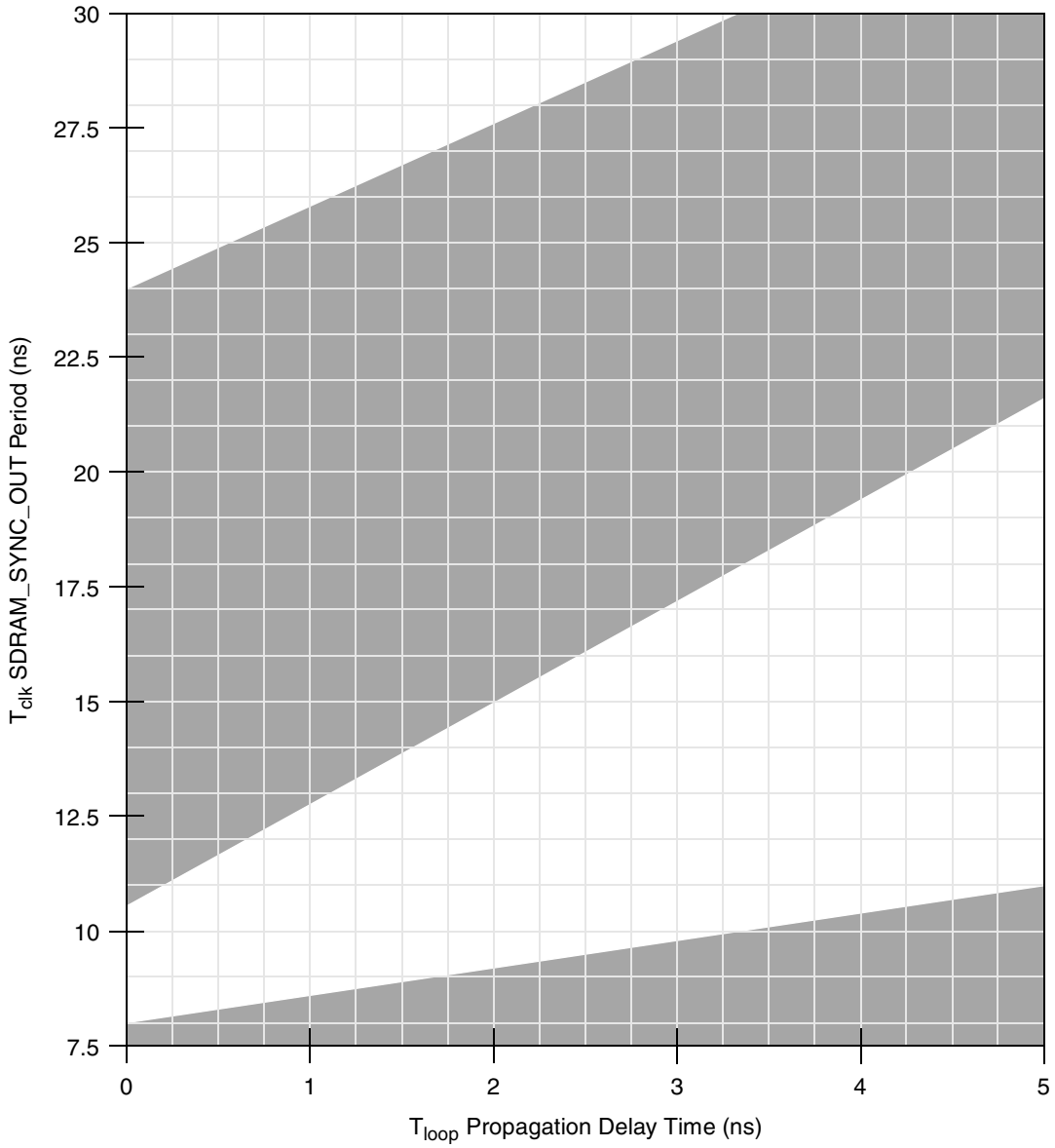


Figure 8. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=1 and Normal Tap Delay

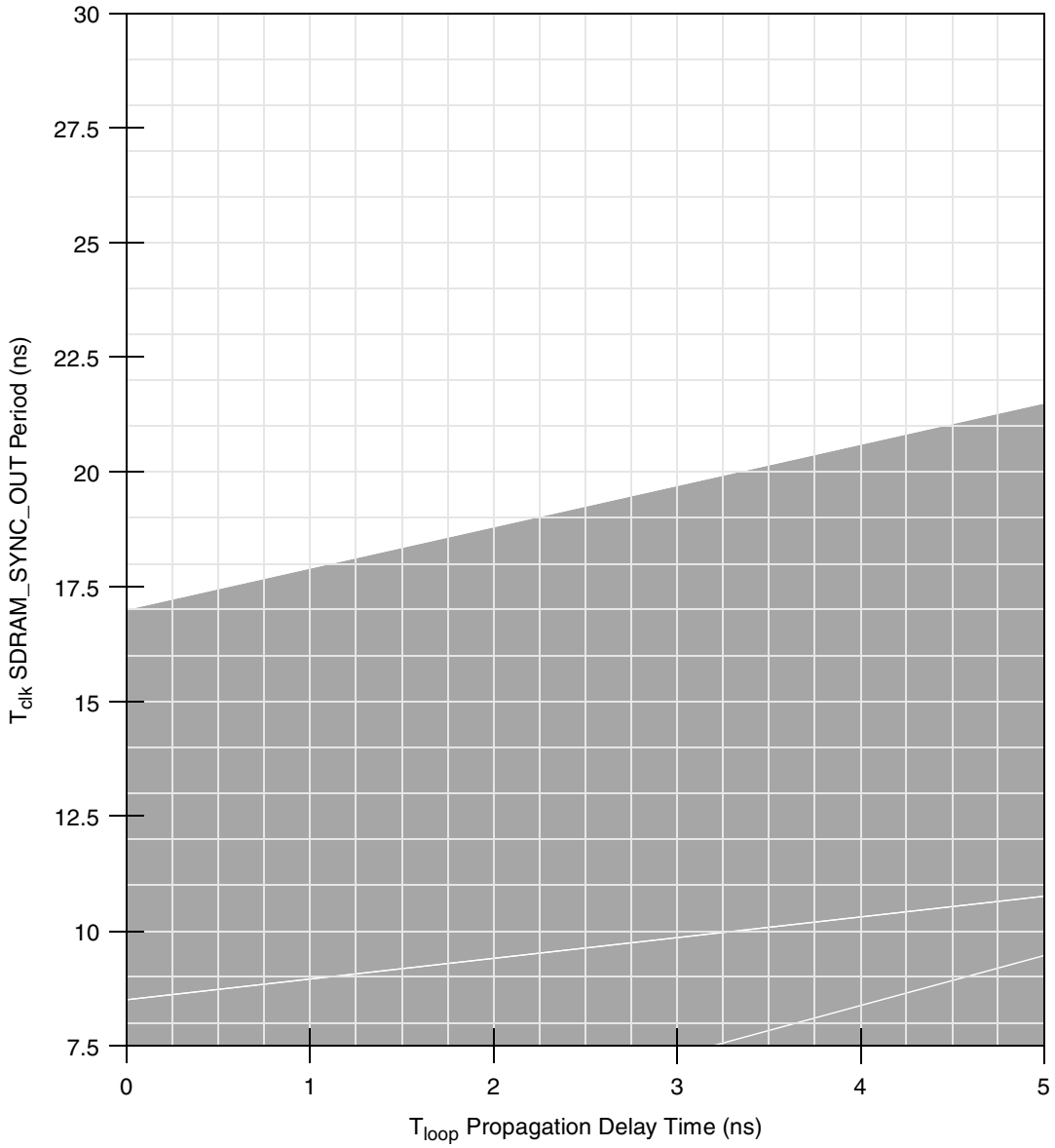


Figure 9. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=0 and Max Tap Delay

Table 11. Output AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
14b	*sys_logic_clk* to output high impedance (for all others)	—	4.0	ns	2

Notes:

1. All PCI signals are measured from $GV_{DD}\_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times GV_{DD}\_OV_{DD}$ or $0.615 \times GV_{DD}\_OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 12.
2. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk* to the TTL level (0.8 or 2.0 V) of the signal in question. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. PCI bused signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[3:0], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[31:0], $\overline{\text{REQ}}$[4:0], $\overline{\text{GNT}}$[4:0], $\overline{\text{IDSEL}}$, and $\overline{\text{INTA}}$.
4. To meet minimum output hold specifications relative to PCI_SYNC_IN for both 33- and 66-MHz PCI systems, the MPC8241 has a programmable output hold delay for PCI signals (the PCI_SYNC_IN to output valid timing is also affected). The initial value of the output hold delay is determined by the values on the $\overline{\text{MCP}}$ and CKE reset configuration signals; the values on these two signals are inverted and subsequently stored as the initial settings of PCI_HOLD_DEL = PMCR2[5, 4] (power management configuration register 2 <0x72>), respectively. Because $\overline{\text{MCP}}$ and CKE have internal pull-up resistors, the default value of PCI_HOLD_DEL after reset is 0b00. Additional output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register. See Figure 15 for PCI_HOLD_DEL effect on output valid and hold time.

Figure 14 provides the AC test load for the MPC8241.

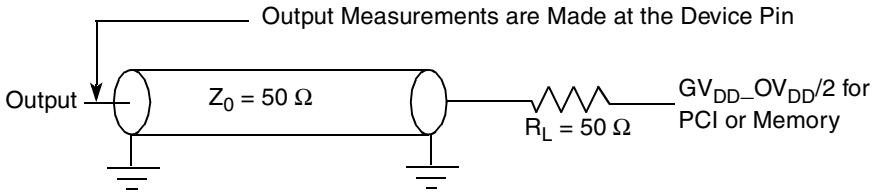
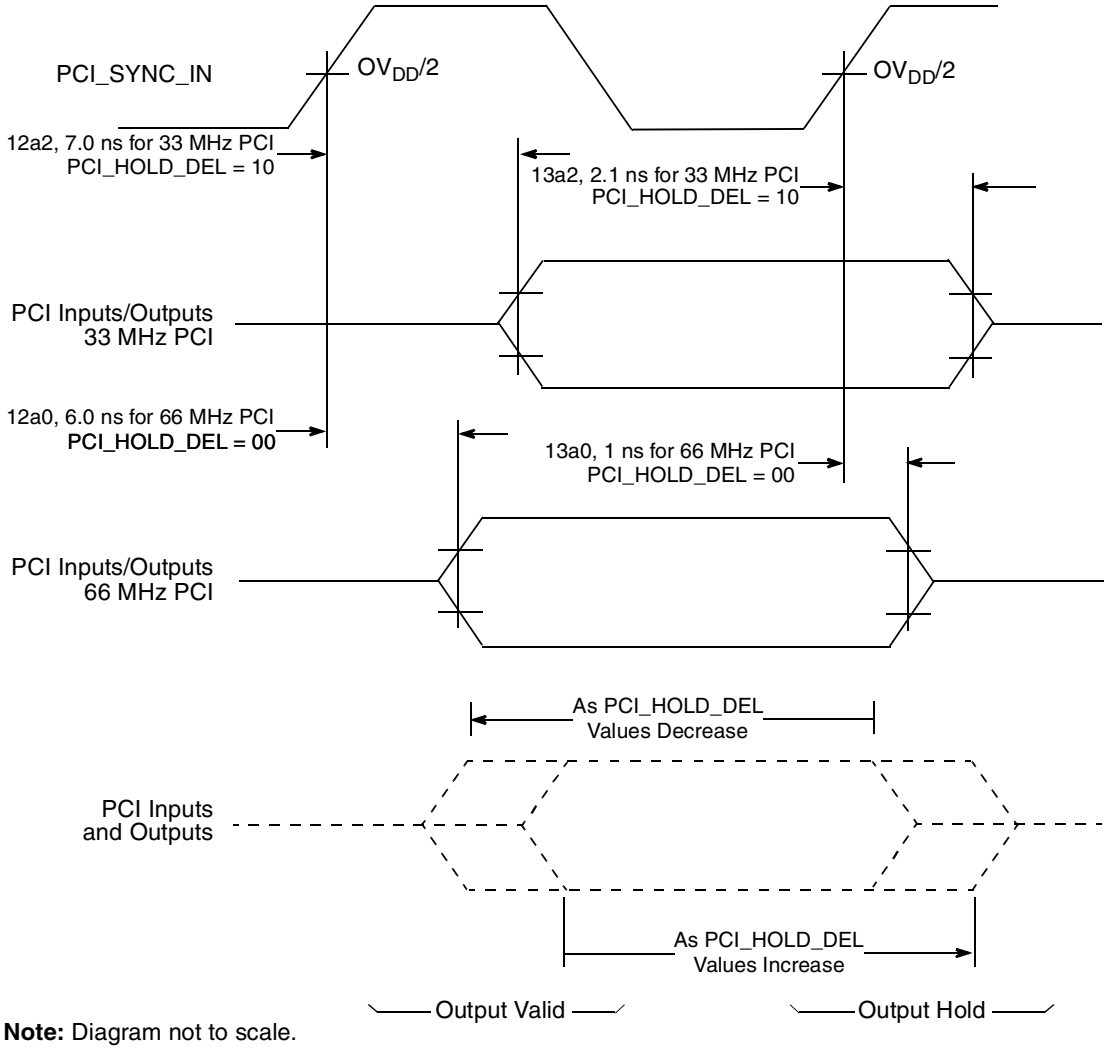


Figure 14. AC Test Load for the MPC8241



Note: Diagram not to scale.

Figure 15. PCI_HOLD_DEL Effect on Output Valid and Hold Time

4.6 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8241.

4.6.1 I²C DC Electrical Characteristics

Table 12 provides the DC electrical characteristics for the I²C interfaces.

Table 12. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

Table 12. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8245 Integrated Processor Reference Manual* for information on the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if the OV_{DD} is switched off.

4.6.2 I^2C AC Electrical Specifications

Table 13 provides the AC timing parameters for the I^2C interfaces.

Table 13. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	µs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	µs
Data output delay time:	t_{I2OVKL}	—	0.9[3]	
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

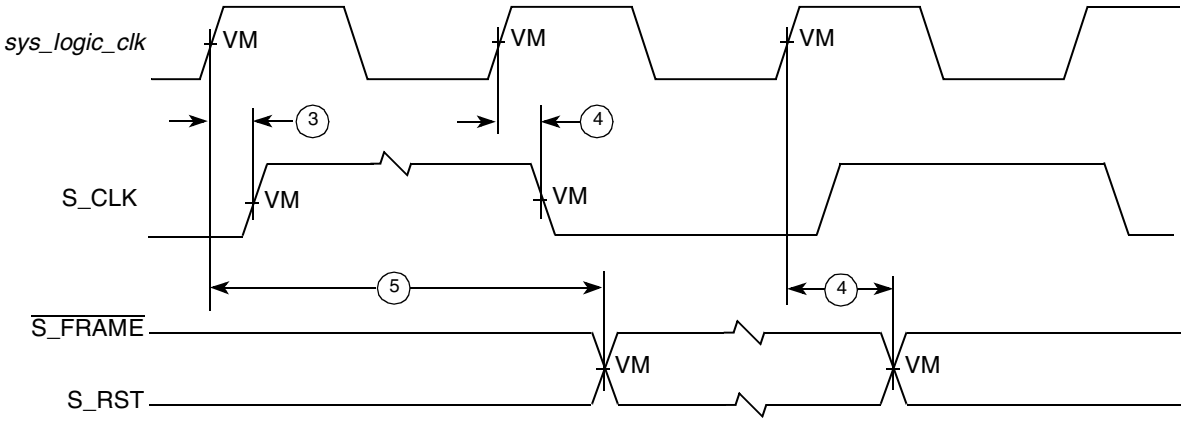


Figure 18. PIC Serial Interrupt Mode Output Timing Diagram

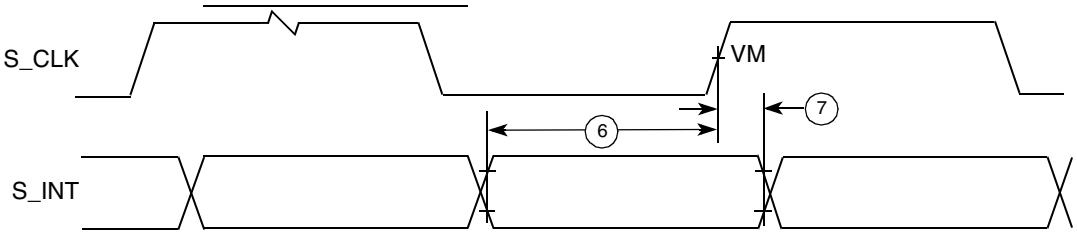


Figure 19. PIC Serial Interrupt Mode Input Timing Diagram

4.7.1 IEEE 1149.1 (JTAG) AC Timing Specifications

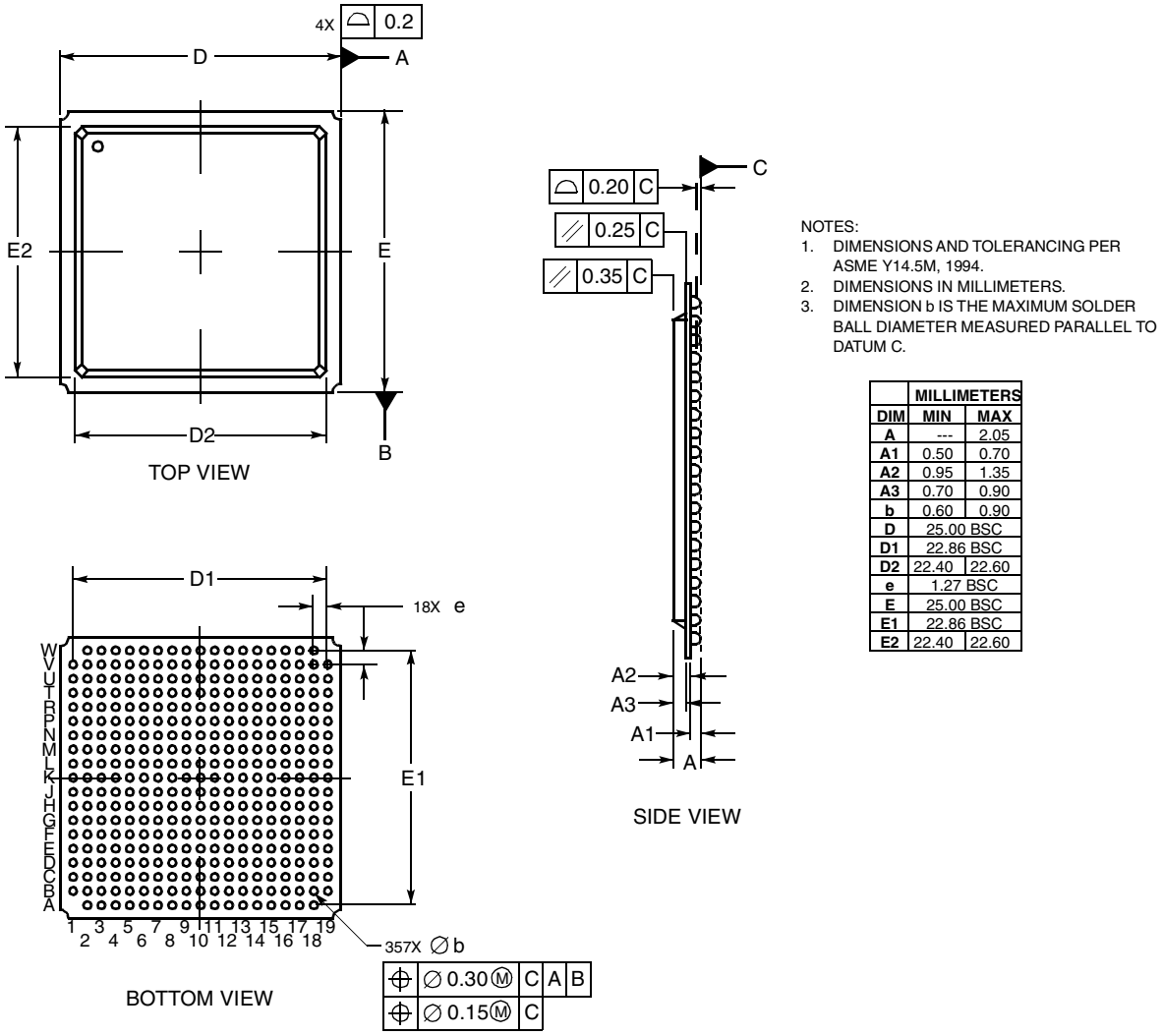
Table 15 provides the JTAG AC timing specifications for the MPC8241 while in the JTAG operating mode at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	—
1	TCK cycle time	40	—	ns	—
2	TCK clock pulse width measured at 1.5 V	20	—	ns	—
3	TCK rise and fall times	0	3	ns	—
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$ assert time	10	—	ns	—
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	—

5.2 Pin Assignments and Package Dimensions

Figure 24 shows the top surface, side profile, and pinout of the MPC8241, 357 PBGA ZP package. Note that this is available for Rev. B parts only.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.05
A1	0.50	0.70
A2	0.95	1.35
A3	0.70	0.90
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	22.40	22.60
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	22.40	22.60

Figure 24. MPC8241 Package Dimensions and Pinout Assignments (ZP Package)

6 PLL Configuration

The PLL_CFG[0:4] are configured by the internal PLLs. For a specific PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations are shown in Table 17 and Table 18.

Table 17. PLL Configurations (166- and 200-MHz)

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	Not available			25-26[5]	75-78	188-195	3 (2)	2.5 (2)
2	00010	34[4]–37[5]	34–37	153–166	34[4]–44[5]	34–44	153–200	1 (4)	4.5 (2)
3	00011[6]	50[7]–66[3]	50–66	100–132	50[7]–66[3]	50–66	100–132	1 (Bypass)	2 (4)
4	00100	25–41[5]	50–82	100–164	25–44[8,10]	50–88	100–176	2 (4)	2 (4)
6	00110[9]	Bypass			Bypass			Bypass	Bypass
7 Rev. B	00111[6]	50[4]–55 [5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (Bypass)	3 (2)
7 Rev. D	00111	Not available							
8	01000	50[4]–55[5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (4)	3 (2)
9	01001	38[4]–41[5,11]	76–82	152–164	38[4]–50[5,12]	76–100	152–200	2 (2)	2 (2)
B	01011	Not available			44[5]	66	198	2(2)	2.5(2)
C	01100	30[4]–33[5]	60–66	150–165	30[4]–40[5]	60–80	150–200	2 (4)	2.5 (2)
E	01110	25–27[5]	50–54	150–162	25–33[5]	60–66	150–198	2 (4)	3 (2)
10	10000	25–27[5,11]	75–83	150–166	25–33[5,12]	75–100	150–200	3 (2)	2 (2)
12	10010	50[4]–55[5,11]	75–83	150–166	50[4]–66[3]	75–99	150–198	1.5 (2)	2 (2)
14	10100	Not available			25–28[5]	50–56	175–196	2 (4)	3.5 (2)
16	10110				25[5]	50	200	2(4)	4(2)
17	10111				25[5]	100	200	4(2)	2(2)
19	11001	33[5,13]	66	165	33[13]–40[5]	66–80	165–200	2(2)	2.5(2)
1A	11010	37[4]–41[5]	37–41	150–166	37[4]–50[5]	37–50	150–200	1 (4)	4 (2)
1B	11011	Not available			33[5,13]	66	198	2(2)	3(2)
1C	11100				44[5,13]	66	198	1.5(2)	3(2)
1D	11101	44[5,13]	66	166	44[13]–53[5]	66–80	165–200	1.5 (2)	2.5 (2)

7.4 Pull-Up/Pull-Down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: MDH[0:31], MDL[0:31], and PAR[0:7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (MDL[0:31] and PAR[4:7]) are disabled, and their outputs drive logic zeros when they would otherwise be driven. For this mode, these pins do not require pull-up resistors and should be left unconnected to minimize possible output switching.

The $\overline{\text{TEST0}}$ pin requires a pull-up resistor of 120 Ω or less connected to GV_{DD}_OV_{DD}.

RTC should have weak pull-up resistors (2–10 kΩ) connected to GV_{DD}_OV_{DD} and that the following signals should be pulled up to GV_{DD}_OV_{DD} with weak pull-up resistors (2–10 kΩ): SDA, SCL, $\overline{\text{SMI}}$, $\overline{\text{SRESET}}$/SDMA12, TBEN/SDMA13, $\overline{\text{CHKSTOP\_IN}}$/SDMA14, TRIG_IN/$\overline{\text{RCS2}}$, $\overline{\text{QACK}}$/DA0, and $\overline{\text{DRDY}}$.

The following PCI control signals should be pulled up to LV_{DD} (the clamping voltage) with weak pull-up resistors (2–10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, and $\overline{\text{TRDY}}$. The resistor values may need to have stronger adjustment to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[3:0], $\overline{\text{REQ4}}$/DA4, TCK, TDI, TMS, and $\overline{\text{TRST}}$. See Table 16.

The following pins have internal pull-up resistors that are enabled only while the device is in the reset state: $\overline{\text{GNT4}}$/DA5, MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, MAA[0:2], and PMAA[0:2]. See Table 16.

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST\_CPU}}$ and $\overline{\text{HRST\_CTRL}}$.

Reset configuration pins should be tied to GND by means of 1-kΩ pull-down resistors to ensure that a logic zero level is read into the configuration bits during reset if the default logic-one level is not desired.

Any other unused active low input pins should be tied to a logic-one level by means of weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND by means of weak pull-down resistors (2–10 kΩ).

7.5 PCI Reference Voltage—LV_{DD}

The MPC8241 PCI reference voltage (LV_{DD}) pins should be connected to 3.3 ± 0.3 V power supply if interfacing the MPC8241 into a 3.3-V PCI bus system. Similarly, the LV_{DD} pins should be connected to 5.0 V ± 5% power supply if interfacing the MPC8241 into a 5-V PCI bus system. For either reference voltage, the MPC8241 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8241 tolerates 5-V signals when interfaced into a 5-V PCI bus system. (See Errata No. 18 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*).

7.6 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port, with additional status monitoring signals. The COP port must independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 27 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 27, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

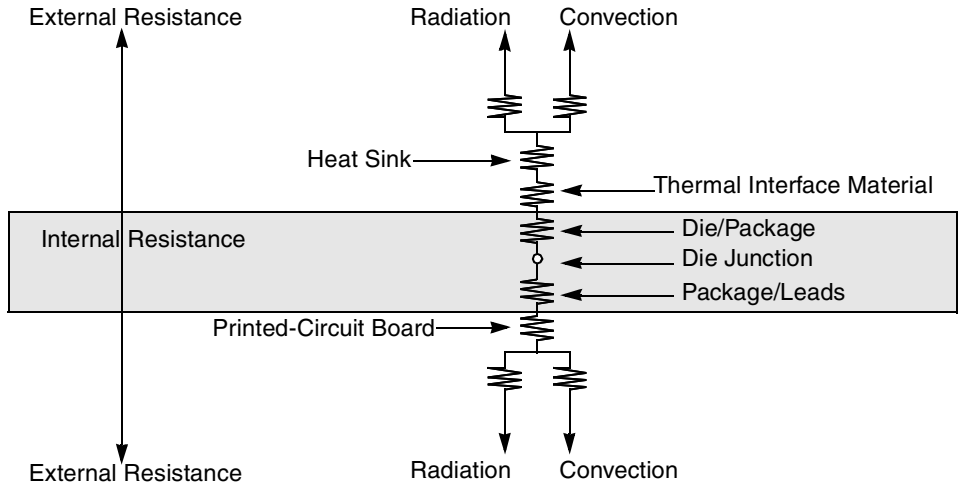
There is no standardized way to number the COP header shown in Figure 27. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 27 is common to all known emulators.

7.7.1 Internal Package Conduction Resistance

For the PBGA, die-up, packaging technology, shown in Figure 28, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-ball thermal resistance

Figure 30 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 30. PBGA Package with Heat Sink Mounted to a Printed-Circuit Board

For this die-up, wire-bond PBGA package, heat generated on the active side of the chip is conducted mainly through the mold cap, the heat sink attach material (or thermal interface material), and finally through the heat sink where forced-air convection removes it.

7.7.2 Adhesives and Thermal Interface Materials

A thermal interface material should be used between the top of the mold cap and the bottom of the heat sink minimizes thermal contact resistance. For applications that attach the heat sink by a spring clip mechanism, Figure 31 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. Thermal grease significantly reduces the interface thermal resistance. That is, the bare joint offers a thermal resistance approximately seven times greater than the thermal grease joint.

A spring clip attaches heat sinks to holes in the printed-circuit board (see Figure 28). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. The selection of any thermal interface material depends on factors such as thermal performance requirements, manufacturability, service temperature, dielectric properties, and cost.

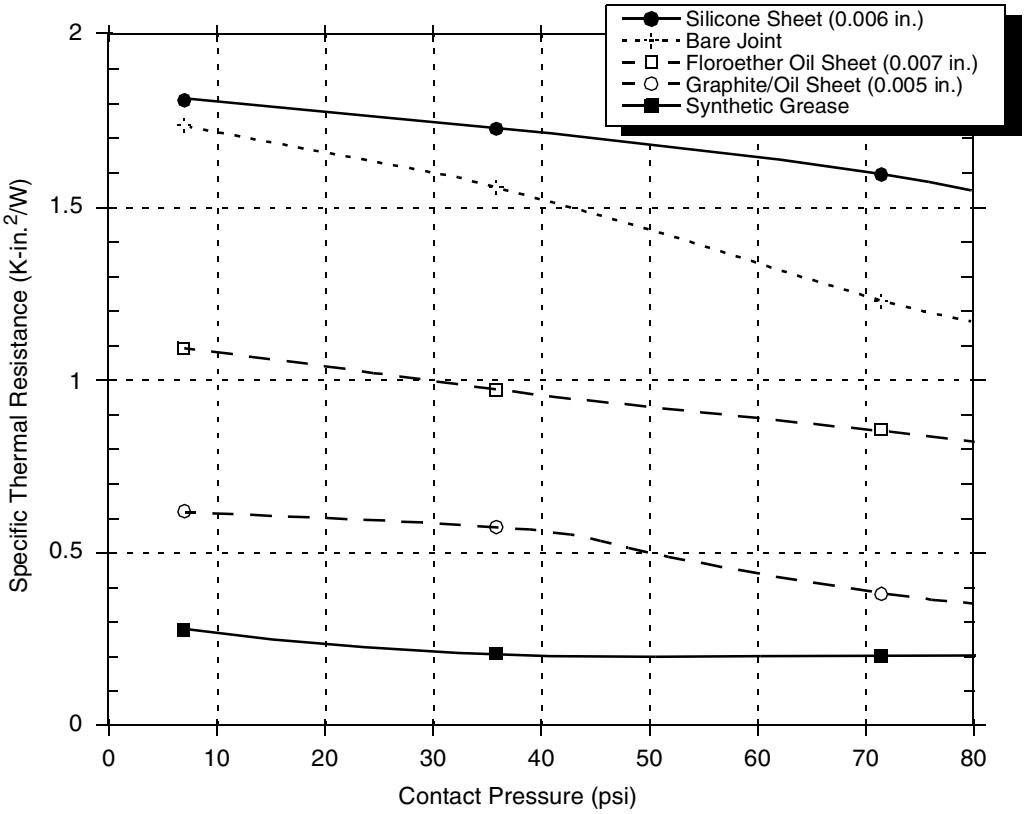


Figure 31. Thermal Performance of Select Thermal Interface Material

The board designer can choose among several types of thermal interface. Heat sink adhesive materials are selected on the basis of high conductivity and adequate mechanical strength to meet equipment shock/vibration requirements. Several commercially-available thermal interfaces and adhesive materials are provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

7.7.3 Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (ψ_{JT}) measures the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature atop the package (°C)
ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance minimizes the change in thermal performance that is caused by removing part of the thermal interface to the heat sink. Considering the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

In many cases, it is appropriate to simulate the system environment using a computational fluid dynamics thermal simulation tool. In such a tool, the simplest thermal model of a package that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board.

7.8 References

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

8 Ordering Information

Ordering information for the parts that this document fully covers is provided in Section 8.1, “Part Numbers Fully Addressed by This Document.” Section 8.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

8.1 Part Numbers Fully Addressed by This Document

Table 19 provides the Freescale part numbering nomenclature for the MPC8241. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number. Read the Revision ID register at address offset 0x08 to determine the revision level.

Table 19. Part Numbering Nomenclature

MPC	*nnnn*	L	*xx*	*nnn*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency [2] (MHz)**	**Revision Level**
MPC	8241	L = Standard spec. 0° to 105°C	ZQ = thick substrate and thick mold cap PBGA (two layers)	166, 200 1.8 V ± 100 mV	D:1.4 = Rev. ID:0x14
			ZQ = thick substrate and thick mold cap PBGA (four layers, thermally enhanced)	266 1.8 V ± 100 mV	
			VR = Lead-free version of package	166, 200, 266 1.8 V ± 100 mV	

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by hardware specifications addendums may support other maximum core frequencies.

8.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specifications addendums that supplement and supersede this document (see Table 20).

Table 20. Part Numbers Addressed by MPC8241TXXPNS Series (Document No. MPC8241ECSO1AD))

MPC	*nnnn*	T	*xx*	*nnn*	*x*	
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency [2] (MHz)**	**Revision Level**	**Processor Version Register Value**

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
8	12/19/2005	Document—Imported new template and made minor editoral corrections. Section 4.3.1—Before Figure 7, added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3. Section 4.3.2—After Figure 12, added a sentence to introduce Figure 13. Section 4.3.3—After Table 11, added a sentence to introduce Figure 14. Section 4.3.4—After Table 13, added to the sentence to introduce Figures 16 thru 19. Section 4.3.6—After Table 16, added a sentence to introduce Figures 22 thru 25. Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2. Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated Section 9.2 to reflect what we offer for new orders. Updated Figure 34 to match with current part marking format. Section 8.3—Added new section for part marking information.
7	05/11/2004	Section 4.1.4 —Table 4: Changed the default for drive strength of DRV_STD_MEM. Section 4.3.1 —Table 8: Changed the wording for item 15 description. Section 4.3.4 —Table 10: Changed T_{os} range and wording in note 7; Figure 11: changed wording for SDRAM_SYNC_IN description relative to T_{OS}.
6.1	—	Section 4.3.1 — Table 9: Corrected last row to state the correct description for the bit setting: Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay”
6	—	Section 4.1.2 — Figure 2: Added note 6 and related label for latching of the PLL_CFG signals. Section 4.1.3 — Updated specifications for the input high and input low voltages of PCI_SYNC_IN. Section 4.3.1 — Table 8: Corrected typo for first number 1a to 1; Updated characteristics for the DLL lock range for the default and remaining three DLL locking modes; Reworded note description for note 6. Replaced contents of Table 9 with bit descriptions for the four DLL locking modes. In Figures 7 through 10, updated the DLL locking mode graphs. Section 4.3.2 — Table 10: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 4.3.3— Table 11: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 5.3 — Table 17: Removed extra listing of DRDY in test/configuration signal list and updated relevant notes for signal in memory Interface signal listing. Updated note #20. Added note 24 for the signals of the UART interface. Section 7.6 — Added relevant notes to this section and updated Figure 29.
5	—	Section 5.1— Updated package information to include all package offerings. Section 5.2 — Included package case outline for ZP (Rev. B) packaging parts. Section 9 — Updated Part markings for the offerings of the MPC8241. All sections — Nontechnical reformatting

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
4	—	Section 1.4.1.2—Table 2: Changed note 1. Figure 2: Updated note 2 and removed 'voltage regulator delay' label since Section 1.7.2 is being deleted this revision. Also, updated Table 5, note 1 to reflect deletion of Section 1.7.2. Section 1.4.1.3—Table 3: Updated the maximum input capacitance from 15 to 16 pF based on characterization data. Section 1.4.3.1—Updated PCI_SYNC_IN jitter specifications to 200 ps. Section 1.4.3.3—Table 11, item 12b: added the word 'address' to help clarify which signals the spec applies to. Figure 15: edited timing for items 12a0 and 12a2 to correspond with Table 11. Section 1.5.2—Changed some dimension values for the side view of package. Section 1.5.3—Updated notes for the $\overline{\text{QACK}}$/DA0 signal because this signal has been found to have no internal pull resistor. Section 1.6—Updated note numbering list for Table 19. Removed mode 5 from PLL tables since that mode is no longer supported. Section 1.7.2 —This section was removed as it was not necessary since the power information is covered in Section 1.4.1.5. Section 1.7.4—Added the words 'the clamping voltage' to describe LV_{DD} in the sixth paragraph. Changed the $\overline{\text{QACK}}$/DA0 signal from the list of signals having an internal pull-up resistor to the list of signals needing a weak pull-up resistor to OV_{DD}. Section 1.9.1—Table 21: Added processor version register value column.
3	—	Section 1.4.1.2—Changed recommended value in Table 2 for I/O buffer supply to 3.3 ± 0.3 V. Changed wording referencing Figure 4 to refer to the MPC8241. Section 1.4.2—Table 6: Updated values for thermal characterization data as per the new packaging and 266-MHz part. Added note 7 for the difference between the 166-/200-MHz and the 266-MHz packaging. Section 1.4.3—Corrected the voltage listing for the 266-MHz part to 1.8 ± 0.1 V in Table 7. Section 1.5—Changed package parameters and illustration based on new packaging. Section 1.6—Table 18: Modified PLL configuration for 166- and 200-MHz parts for mode 7 to specify that this mode is not available for Rev. D of the part. Added sentence to note 1 referencing update for mode 7. Table 19: Made several range updates for various modes to accommodate VCO limits. Added mode 7 and 1E updates for Rev. D. Updated VCO limits listed in notes 4, 6, and 7.
2	—	Section 1.4.1.2—Updated note 1 to include 266-MHz part. Added a line to cautions 2 and 3 in the notes section of Table 2. Added Figures 4 and 5 to show the overshoot and undershoot requirements for the PCI interface. Section 1.4.1.3—Table 3: Updated minimum value for input high voltage, and maximum value for capacitance. Section 1.4.3.2—Appended Figures 9 and 10. Section 1.4.3.4—Added a column to Table 13 to include 133-MHz memory bus speed for 266-MHz part. Section 1.5.2—Changed Figure 24 to accommodate new package offerings. Section 1.6—Added Table 19 for PLL of the 266-MHz part. Section 1.7.7—Corrected note numbering in COP connector diagram. Section 1.9.1—Updated package description in part marking nomenclature.