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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8241tvr200d

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8241.

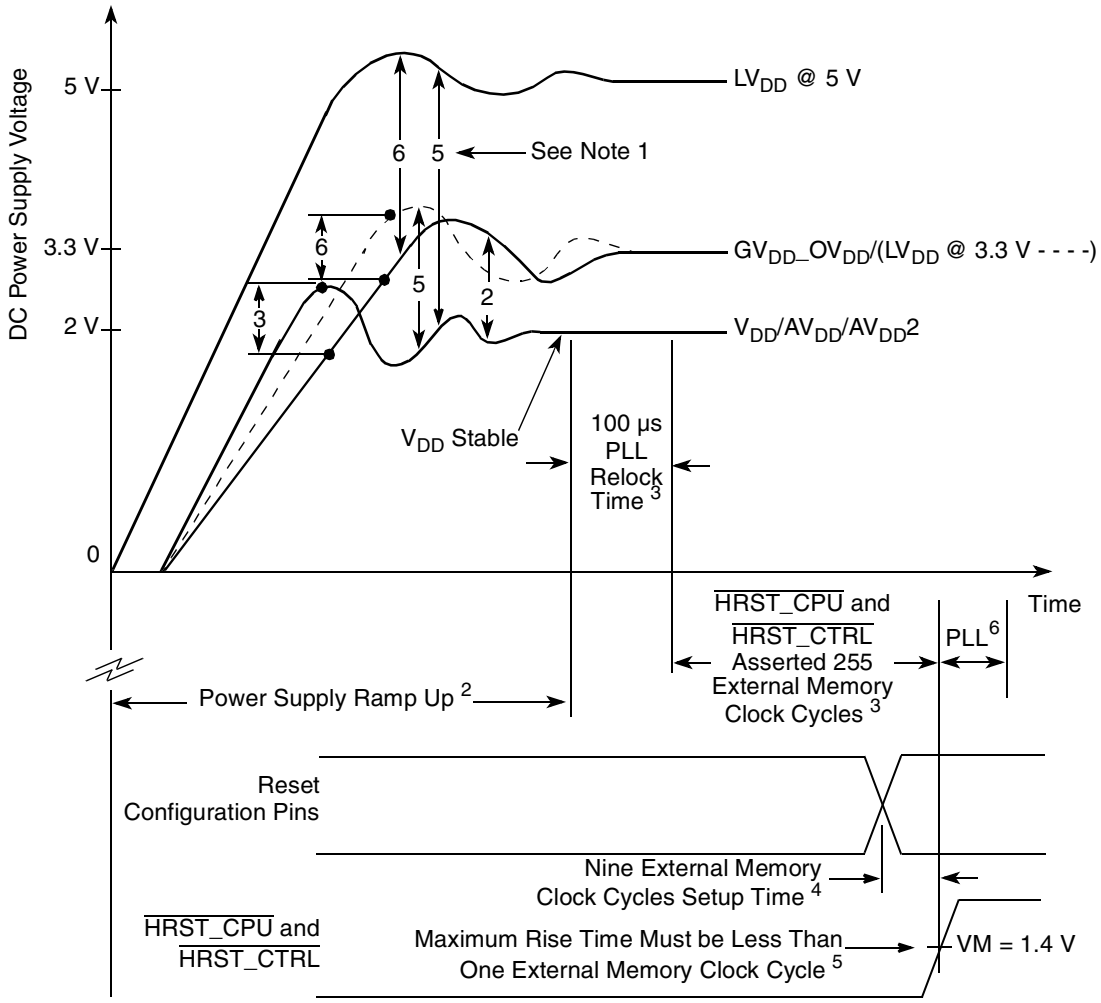
Table 2. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply voltage		V_{DD}	1.8 ± 100 mV	V	2
I/O buffer supply for PCI and standard; supply voltages for memory bus drivers		$GV_{DD}\_OV_{DD}$	3.3 ± 0.3	V	2
CPU PLL supply voltage		AV_{DD}	1.8 ± 100 mV		2
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8 ± 100 mV	V	2
PCI reference		LV_{DD}	5.0 ± 5%	V	4, 5, 6
			3.3 ± 0.3	V	5, 6, 7
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	4, 7
	All other inputs		0 to 3.6	V	8
Die-junction temperature		T_j	0 to 105	•C	

Notes:

1. Freescale has tested these operating conditions and recommends them. Proper device operation outside of these conditions is not guaranteed.
2. **Caution:** $GV_{DD}\_OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 1.8 V at any time including during power-on reset. Note that $GV_{DD}\_OV_{DD}$ pins are all shorted together: This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. Connections should not be made to individual PWRRING pins.
3. **Caution:** $V_{DD}/AV_{DD}/AV_{DD}2$ must not exceed $GV_{DD}\_OV_{DD}$ by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 5.0 V DC power supply.
5. **Caution:** LV_{DD} must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** LV_{DD} must not exceed $GV_{DD}\_OV_{DD}$ by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3 V DC power supply.
8. **Caution:** Input voltage (V_{in}) must not be greater than the supply voltage ($V_{DD}/AV_{DD}/AV_{DD}2$) by more than 2.5 V at all times including during power-on reset. Input voltage (V_{in}) must not be greater than $GV_{DD}\_OV_{DD}$ by more than 0.6 V at all times including during power-on reset.

Figure 2 shows supply voltage sequencing and separation cautions.



Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. See the Cautions section of Table 2 for details on this topic.
3. Refer to Table 8 for details on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for details on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.
6. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ negate in order to be latched.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Register settings that define each DLL mode are shown in Table 9.

Table 9. DLL Mode Definition

DLL Mode	Bit 2 of Configuration Register at 0x76	Bit 7 of Configuration Register at 0x72
Normal tap delay, No DLL extend	0	0
Normal tap delay, DLL extend	0	1
Max tap delay, No DLL extend	1	0
Max tap delay, DLL extend	1	1

The DLL_MAX_DELAY bit can lengthen the amount of time through the delay line by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock is within the DLL lock range, there may be slightly more jitter in the output clock of the DLL if the phase comparator shifts the clock between adjacent tap points. Refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1*, for details on DLL modes and memory design.

The value of the current tap point after the DLL locks can be determined by reading bits 6–0 (DLL_TAP_COUNT) of the DLL tap count register (DTCR, located at offset 0xE3). These bits store the value (binary 0 through 127) of the current tap point and can indicate whether the DLL advances or decrements as it maintains the DLL lock. Therefore, for evaluation purposes, DTCR can be read for all DLL modes that support the T_{loop} value used for the trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN. The DLL mode with the smallest tap point value in the DTCR should be used because the bigger the tap point value, the more jitter that can be expected for clock signals. Keeping a DLL mode locked below tap point decimal 12 is not recommended.

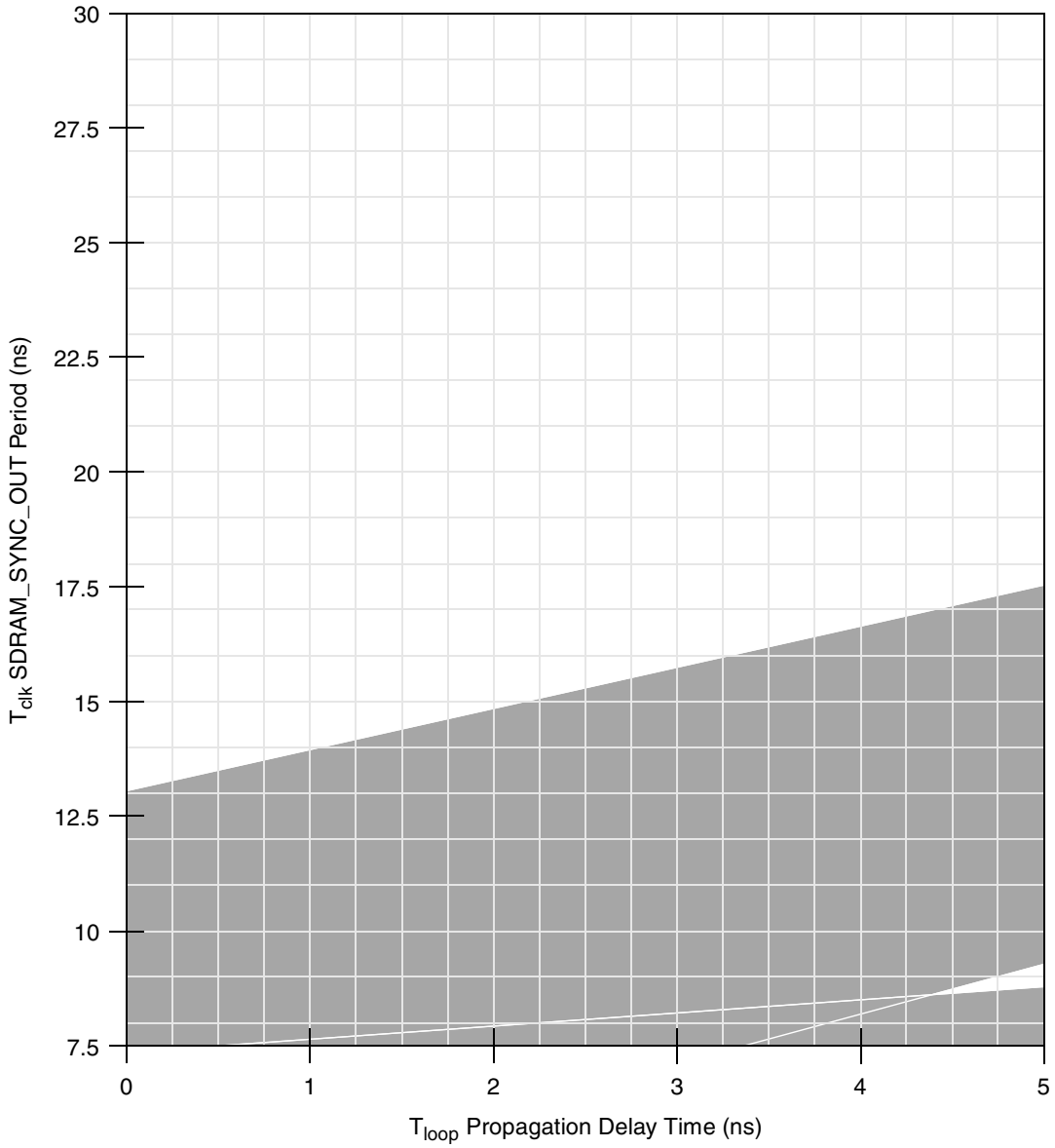


Figure 7. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=0 and Normal Tap Delay

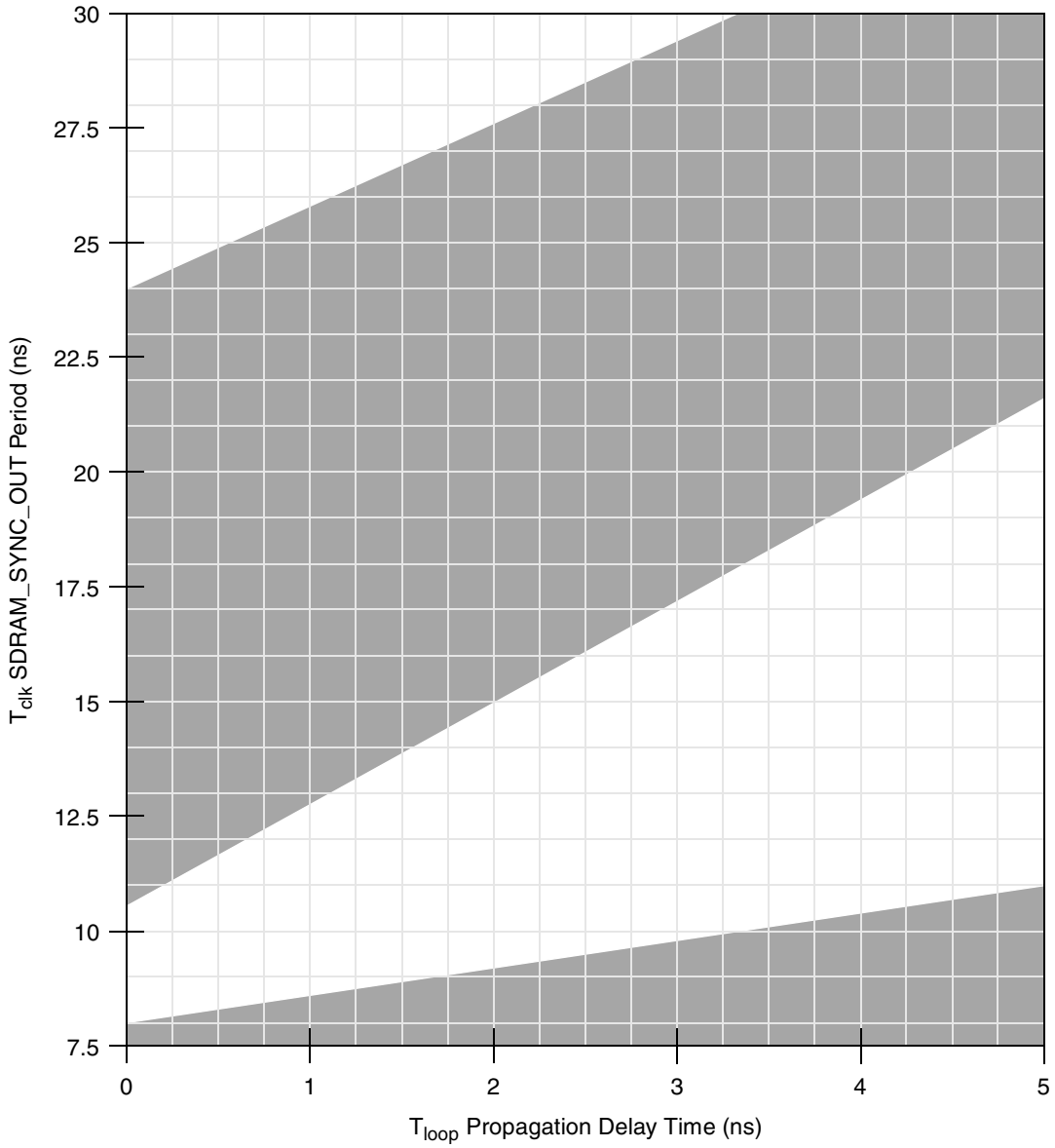


Figure 8. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=1 and Normal Tap Delay

Table 10. Input AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
10b0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	2.6	—	ns	2, 3, 6
10b1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	1.9	—		
10b2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.2	—		
10b3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	0.5	—		
10c	PIC miscellaneous debug input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10d	I^2C input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10e	Mode select inputs valid to $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ (input setup)	$9 \times t_{CLK}$	—	ns	2, 3–5
11	T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* offset time	0.4	1.0	ns	7
11a	*sys_logic_clk* to memory signal inputs invalid (input hold)				
11a0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	0	—	ns	2, 3, 6
11a1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	0.7	—		
11a2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.4	—		
11a3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	2.1	—		
11b	$\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ to mode select inputs invalid (input hold)	0	—	ns	2, 3, 5
11c	PCI_SYNC_IN to inputs invalid (input hold)	1.0	—	ns	1, 2, 3

Notes:

1. All PCI signals are measured from $GV_{DD}\_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times GV_{DD}\_OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 12.
2. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock. *sys_logic_clk*. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ signal. See Figure 13.
6. The memory interface input setup and hold times are programmable to four possible combinations by programming bits 5:4 of register offset <0x77> to select the desired input setup and hold times.
7. T_{os} represents a timing adjustment for SDRAM_SYNC_IN with respect to *sys_logic_clk*. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the *sys_logic_clk* inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. The feedback trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN must be shortened to accommodate this range relative to the SDRAM clock output trace lengths to maintain phase-alignment of the memory clocks with respect to *sys_logic_clk*. It is recommended that the length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN be shortened by 0.7 ns because that is the midpoint of the range of T_{os} and allows the impact from the range of T_{os} to be reduced. Additional analyses of trace lengths and SDRAM loading must be performed to optimize timing. For details on trace measurements and the T_{os} problem, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*.

Table 11. Output AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
14b	*sys_logic_clk* to output high impedance (for all others)	—	4.0	ns	2

Notes:

1. All PCI signals are measured from $GV_{DD}\_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times GV_{DD}\_OV_{DD}$ or $0.615 \times GV_{DD}\_OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 12.
2. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk* to the TTL level (0.8 or 2.0 V) of the signal in question. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. PCI bused signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[3:0], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[31:0], $\overline{\text{REQ}}$[4:0], $\overline{\text{GNT}}$[4:0], $\overline{\text{IDSEL}}$, and $\overline{\text{INTA}}$.
4. To meet minimum output hold specifications relative to PCI_SYNC_IN for both 33- and 66-MHz PCI systems, the MPC8241 has a programmable output hold delay for PCI signals (the PCI_SYNC_IN to output valid timing is also affected). The initial value of the output hold delay is determined by the values on the $\overline{\text{MCP}}$ and CKE reset configuration signals; the values on these two signals are inverted and subsequently stored as the initial settings of PCI_HOLD_DEL = PMCR2[5, 4] (power management configuration register 2 <0x72>), respectively. Because $\overline{\text{MCP}}$ and CKE have internal pull-up resistors, the default value of PCI_HOLD_DEL after reset is 0b00. Additional output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register. See Figure 15 for PCI_HOLD_DEL effect on output valid and hold time.

Figure 14 provides the AC test load for the MPC8241.

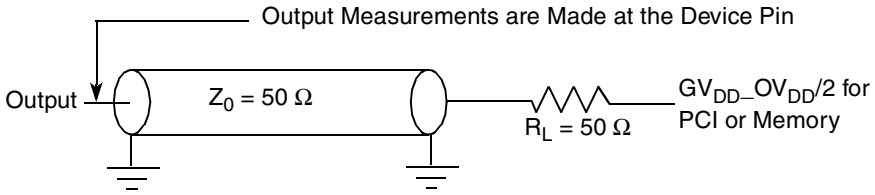
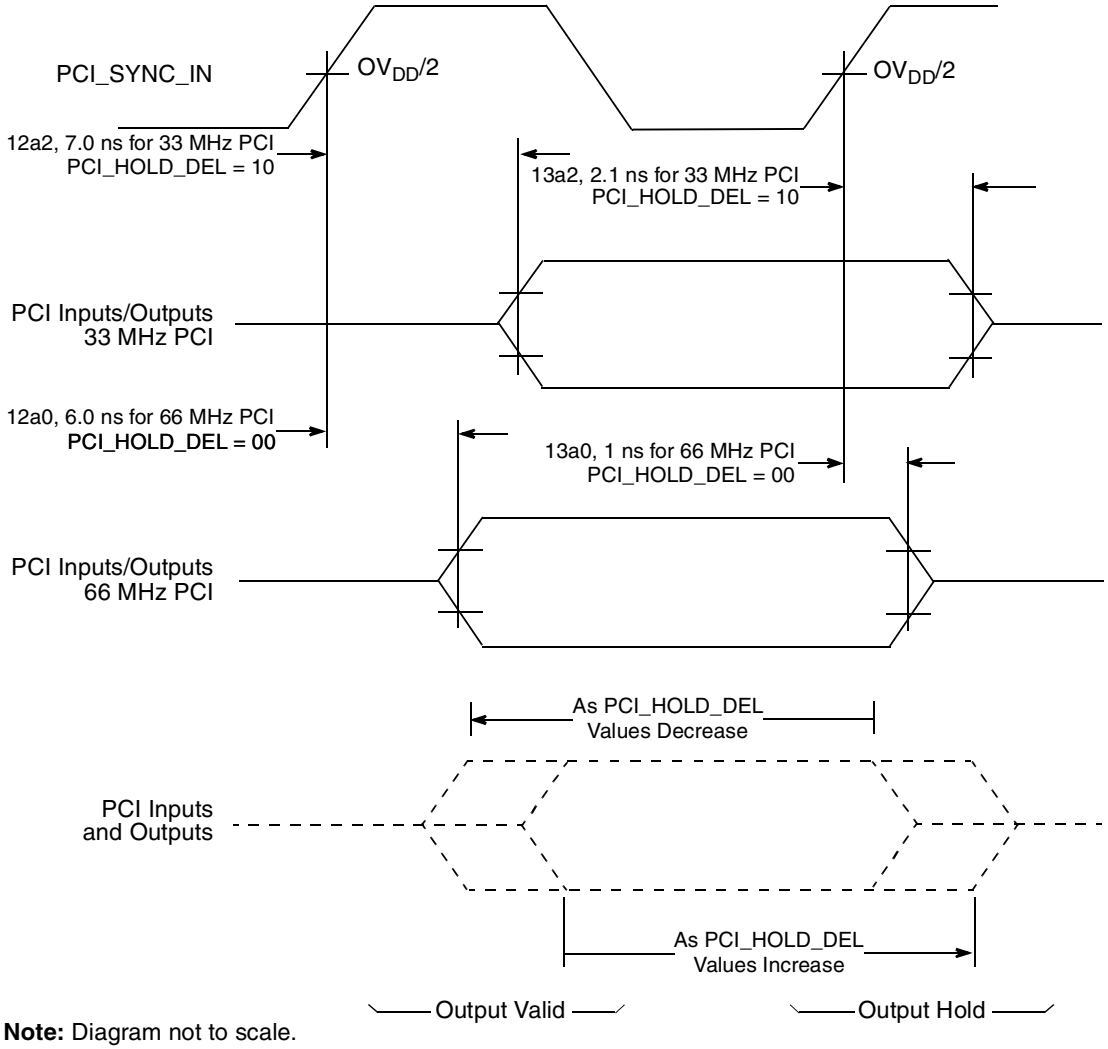


Figure 14. AC Test Load for the MPC8241



Note: Diagram not to scale.

Figure 15. PCI_HOLD_DEL Effect on Output Valid and Hold Time

4.6 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8241.

4.6.1 I²C DC Electrical Characteristics

Table 12 provides the DC electrical characteristics for the I²C interfaces.

Table 12. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

Table 12. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8245 Integrated Processor Reference Manual* for information on the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if the OV_{DD} is switched off.

4.6.2 I^2C AC Electrical Specifications

Table 13 provides the AC timing parameters for the I^2C interfaces.

Table 13. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	µs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	µs
Data output delay time:	t_{I2OVKL}	—	0.9[3]	
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

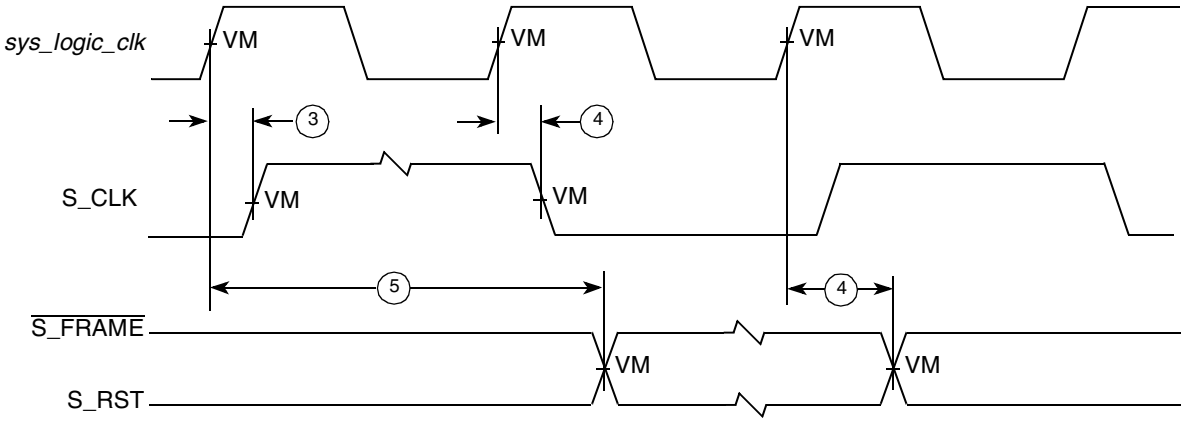


Figure 18. PIC Serial Interrupt Mode Output Timing Diagram

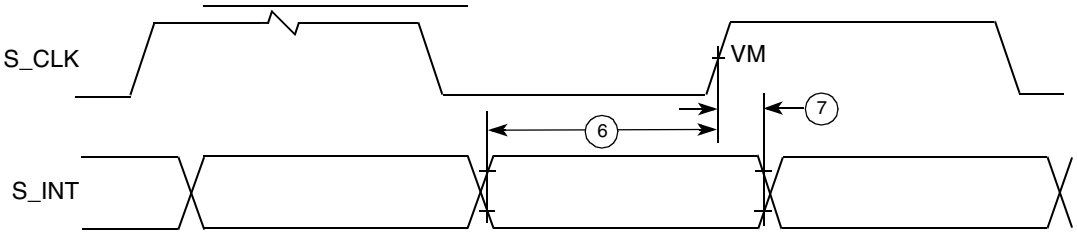


Figure 19. PIC Serial Interrupt Mode Input Timing Diagram

4.7.1 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 15 provides the JTAG AC timing specifications for the MPC8241 while in the JTAG operating mode at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	—
1	TCK cycle time	40	—	ns	—
2	TCK clock pulse width measured at 1.5 V	20	—	ns	—
3	TCK rise and fall times	0	3	ns	—
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$ assert time	10	—	ns	—
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	—

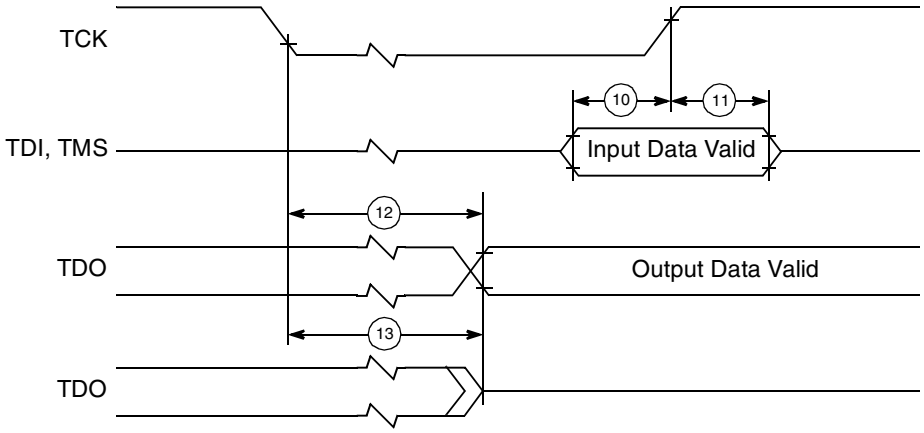


Figure 23. Test Access Port Timing Diagram

5 Package Description

This section details package parameters, pin assignments, and dimensions.

5.1 Package Parameters for the MPC8241

The MPC8241 uses a 25 mm × 25 mm, cavity up, 357-pin plastic ball grid array (PBGA) package. The package parameters are as follows.

Package outline	25 mm × 25 mm
Interconnects	357
Pitch	1.27 mm
Solder balls	ZP (PBGA)—62 Sn/36 Pb/2 Ag—available only in Rev B parts ZQ (Thick substrate thick mold cap PBGA)—62 Sn/36 Pb/2 Ag VR (Lead free version of package)—95.5 Sn/4.0 Ag/0.5 Cu
Solder ball diameter	0.75 mm
Maximum module height	2.52 mm
Co-planarity specification	0.15 mm
Maximum force	6.0 lbs. total, uniformly distributed over package (8 grams/ball)

Table 17. PLL Configurations (166- and 200-MHz) (continued)

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1E	11110[14]	Not usable			Not usable			Off	Off
1F	11111[14]	Not usable			Not usable			Off	Off

Notes:

1. PLL_CFG[0:4] settings not listed are reserved. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value. Note the impact of the relevant revisions for mode 7.
2. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
3. Limited by maximum PCI input frequency (66 MHz).
4. Limited by minimum CPU VCO frequency (300 MHz).
5. Limited by maximum CPU operating frequency.
6. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
7. Limited by minimum CPU operating frequency (100 MHz).
8. Limited due to maximum memory VCO frequency (352 MHz).
9. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
10. Limited by maximum CPU VCO frequency (704 MHz).
11. Limited by maximum system memory interface operating frequency (83 MHz @ 166 MHz CPU bus speed).
12. Limited by maximum system memory interface operating frequency (100 MHz @ 200 MHz CPU bus speed).
13. Limited by minimum memory VCO frequency (132 MHz).
14. In clock off mode, no clocking occurs inside the MPC8241, regardless of the PCI_SYNC_IN input.

Table 18. PLL Configurations (266-MHz Parts)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	25–35[5]	75–105	188–263	3 (2)	2.5 (2)
1	00001	25–29[5]	75–88	225–264	3 (2)	3 (2)
2	00010	50[15]–59[5]	50–59	225–266	1 (4)	4.5 (2)
3	00011[12]	50[14]–66[1]	50–66	100–133	1 (Bypass)	2 (4)
4	00100	25–44[4]	50–88	100–176	2 (4)	2 (4)

7.4 Pull-Up/Pull-Down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: MDH[0:31], MDL[0:31], and PAR[0:7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (MDL[0:31] and PAR[4:7]) are disabled, and their outputs drive logic zeros when they would otherwise be driven. For this mode, these pins do not require pull-up resistors and should be left unconnected to minimize possible output switching.

The $\overline{\text{TEST0}}$ pin requires a pull-up resistor of 120 Ω or less connected to GV_{DD}_OV_{DD}.

RTC should have weak pull-up resistors (2–10 kΩ) connected to GV_{DD}_OV_{DD} and that the following signals should be pulled up to GV_{DD}_OV_{DD} with weak pull-up resistors (2–10 kΩ): SDA, SCL, $\overline{\text{SMI}}$, $\overline{\text{SRESET}}$/SDMA12, TBEN/SDMA13, $\overline{\text{CHKSTOP\_IN}}$/SDMA14, TRIG_IN/$\overline{\text{RCS2}}$, $\overline{\text{QACK}}$/DA0, and $\overline{\text{DRDY}}$.

The following PCI control signals should be pulled up to LV_{DD} (the clamping voltage) with weak pull-up resistors (2–10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, and $\overline{\text{TRDY}}$. The resistor values may need to have stronger adjustment to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[3:0], $\overline{\text{REQ4}}$/DA4, TCK, TDI, TMS, and $\overline{\text{TRST}}$. See Table 16.

The following pins have internal pull-up resistors that are enabled only while the device is in the reset state: $\overline{\text{GNT4}}$/DA5, MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, MAA[0:2], and PMAA[0:2]. See Table 16.

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST\_CPU}}$ and $\overline{\text{HRST\_CTRL}}$.

Reset configuration pins should be tied to GND by means of 1-kΩ pull-down resistors to ensure that a logic zero level is read into the configuration bits during reset if the default logic-one level is not desired.

Any other unused active low input pins should be tied to a logic-one level by means of weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND by means of weak pull-down resistors (2–10 kΩ).

7.5 PCI Reference Voltage—LV_{DD}

The MPC8241 PCI reference voltage (LV_{DD}) pins should be connected to 3.3 ± 0.3 V power supply if interfacing the MPC8241 into a 3.3-V PCI bus system. Similarly, the LV_{DD} pins should be connected to 5.0 V ± 5% power supply if interfacing the MPC8241 into a 5-V PCI bus system. For either reference voltage, the MPC8241 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8241 tolerates 5-V signals when interfaced into a 5-V PCI bus system. (See Errata No. 18 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*).

7.7 Thermal Management

This section provides thermal management information for the plastic ball grid array (PBGA) package for air-cooled applications. Depending on the application environment and the operating frequency, a heat sink may be required to maintain junction temperature within specifications. Proper thermal control design primarily depends on the system-level design: heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks can be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, or mounting clip and screw assembly (see Figure 28).

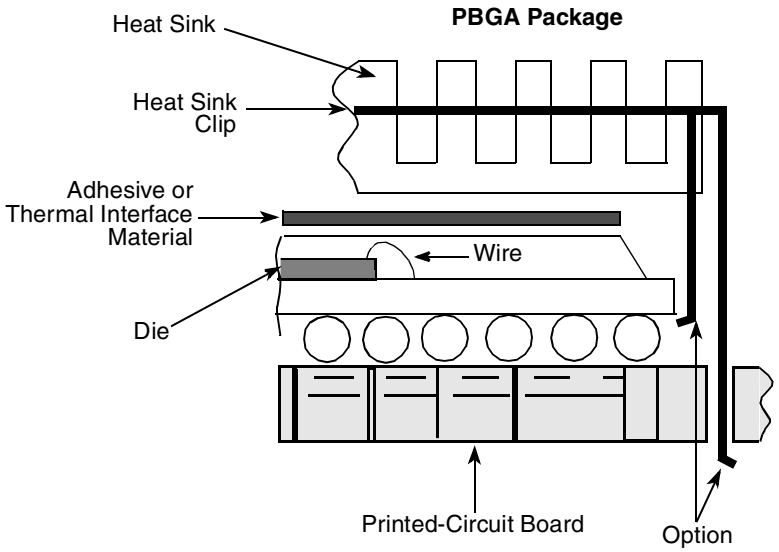


Figure 28. Package Exploded Cross-Sectional View with Several Heat Sink Options

Figure 29 depicts the die junction-to-ambient thermal resistance for four typical cases:

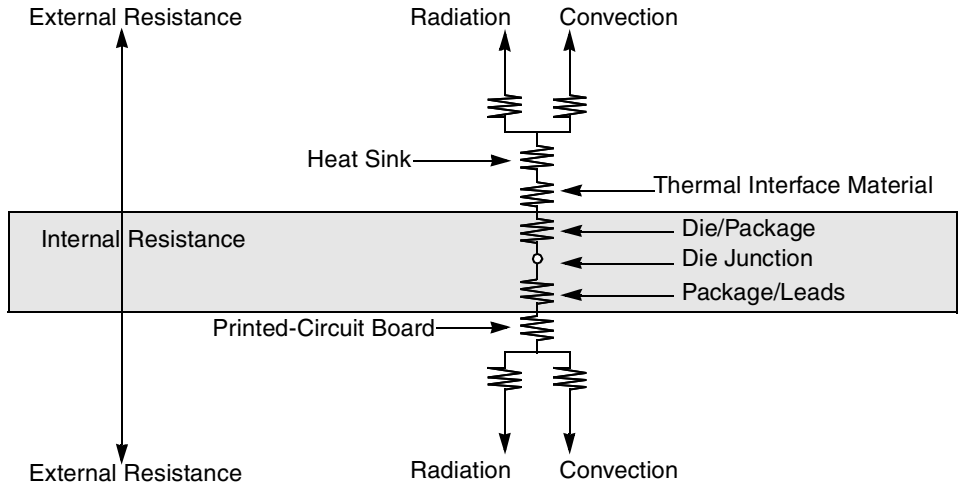
- A heat sink is not attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s).
- A heat sink is not attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s/sink).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p/sink).

7.7.1 Internal Package Conduction Resistance

For the PBGA, die-up, packaging technology, shown in Figure 28, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-ball thermal resistance

Figure 30 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 30. PBGA Package with Heat Sink Mounted to a Printed-Circuit Board

For this die-up, wire-bond PBGA package, heat generated on the active side of the chip is conducted mainly through the mold cap, the heat sink attach material (or thermal interface material), and finally through the heat sink where forced-air convection removes it.

7.7.2 Adhesives and Thermal Interface Materials

A thermal interface material should be used between the top of the mold cap and the bottom of the heat sink minimizes thermal contact resistance. For applications that attach the heat sink by a spring clip mechanism, Figure 31 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. Thermal grease significantly reduces the interface thermal resistance. That is, the bare joint offers a thermal resistance approximately seven times greater than the thermal grease joint.

A spring clip attaches heat sinks to holes in the printed-circuit board (see Figure 28). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. The selection of any thermal interface material depends on factors such as thermal performance requirements, manufacturability, service temperature, dielectric properties, and cost.

where:

T_T = thermocouple temperature atop the package (°C)
ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance minimizes the change in thermal performance that is caused by removing part of the thermal interface to the heat sink. Considering the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

In many cases, it is appropriate to simulate the system environment using a computational fluid dynamics thermal simulation tool. In such a tool, the simplest thermal model of a package that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board.

7.8 References

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

8 Ordering Information

Ordering information for the parts that this document fully covers is provided in Section 8.1, “Part Numbers Fully Addressed by This Document.” Section 8.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

8.1 Part Numbers Fully Addressed by This Document

Table 19 provides the Freescale part numbering nomenclature for the MPC8241. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number. Read the Revision ID register at address offset 0x08 to determine the revision level.

Table 19. Part Numbering Nomenclature

MPC	*nnnn*	L	*xx*	*nnn*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency [2] (MHz)**	**Revision Level**
MPC	8241	L = Standard spec. 0° to 105°C	ZQ = thick substrate and thick mold cap PBGA (two layers)	166, 200 1.8 V ± 100 mV	D:1.4 = Rev. ID:0x14
			ZQ = thick substrate and thick mold cap PBGA (four layers, thermally enhanced)	266 1.8 V ± 100 mV	
			VR = Lead-free version of package	166, 200, 266 1.8 V ± 100 mV	

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by hardware specifications addendums may support other maximum core frequencies.

8.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specifications addendums that supplement and supersede this document (see Table 20).

Table 20. Part Numbers Addressed by MPC8241TXXPNS Series (Document No. MPC8241ECSO1AD))

MPC	*nnnn*	T	*xx*	*nnn*	*x*	
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency [2] (MHz)**	**Revision Level**	**Processor Version Register Value**

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
8	12/19/2005	Document—Imported new template and made minor editoral corrections. Section 4.3.1—Before Figure 7, added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3. Section 4.3.2—After Figure 12, added a sentence to introduce Figure 13. Section 4.3.3—After Table 11, added a sentence to introduce Figure 14. Section 4.3.4—After Table 13, added to the sentence to introduce Figures 16 thru 19. Section 4.3.6—After Table 16, added a sentence to introduce Figures 22 thru 25. Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2. Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated Section 9.2 to reflect what we offer for new orders. Updated Figure 34 to match with current part marking format. Section 8.3—Added new section for part marking information.
7	05/11/2004	Section 4.1.4 —Table 4: Changed the default for drive strength of DRV_STD_MEM. Section 4.3.1 —Table 8: Changed the wording for item 15 description. Section 4.3.4 —Table 10: Changed T_{os} range and wording in note 7; Figure 11: changed wording for SDRAM_SYNC_IN description relative to T_{OS}.
6.1	—	Section 4.3.1 — Table 9: Corrected last row to state the correct description for the bit setting: Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay”
6	—	Section 4.1.2 — Figure 2: Added note 6 and related label for latching of the PLL_CFG signals. Section 4.1.3 — Updated specifications for the input high and input low voltages of PCI_SYNC_IN. Section 4.3.1 — Table 8: Corrected typo for first number 1a to 1; Updated characteristics for the DLL lock range for the default and remaining three DLL locking modes; Reworded note description for note 6. Replaced contents of Table 9 with bit descriptions for the four DLL locking modes. In Figures 7 through 10, updated the DLL locking mode graphs. Section 4.3.2 — Table 10: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 4.3.3— Table 11: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 5.3 — Table 17: Removed extra listing of DRDY in test/configuration signal list and updated relevant notes for signal in memory Interface signal listing. Updated note #20. Added note 24 for the signals of the UART interface. Section 7.6 — Added relevant notes to this section and updated Figure 29.
5	—	Section 5.1— Updated package information to include all package offerings. Section 5.2 — Included package case outline for ZP (Rev. B) packaging parts. Section 9 — Updated Part markings for the offerings of the MPC8241. All sections — Nontechnical reformatting

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
4	—	Section 1.4.1.2—Table 2: Changed note 1. Figure 2: Updated note 2 and removed 'voltage regulator delay' label since Section 1.7.2 is being deleted this revision. Also, updated Table 5, note 1 to reflect deletion of Section 1.7.2. Section 1.4.1.3—Table 3: Updated the maximum input capacitance from 15 to 16 pF based on characterization data. Section 1.4.3.1—Updated PCI_SYNC_IN jitter specifications to 200 ps. Section 1.4.3.3—Table 11, item 12b: added the word 'address' to help clarify which signals the spec applies to. Figure 15: edited timing for items 12a0 and 12a2 to correspond with Table 11. Section 1.5.2—Changed some dimension values for the side view of package. Section 1.5.3—Updated notes for the $\overline{\text{QACK}}$/DA0 signal because this signal has been found to have no internal pull resistor. Section 1.6—Updated note numbering list for Table 19. Removed mode 5 from PLL tables since that mode is no longer supported. Section 1.7.2 —This section was removed as it was not necessary since the power information is covered in Section 1.4.1.5. Section 1.7.4—Added the words 'the clamping voltage' to describe LV_{DD} in the sixth paragraph. Changed the $\overline{\text{QACK}}$/DA0 signal from the list of signals having an internal pull-up resistor to the list of signals needing a weak pull-up resistor to OV_{DD}. Section 1.9.1—Table 21: Added processor version register value column.
3	—	Section 1.4.1.2—Changed recommended value in Table 2 for I/O buffer supply to 3.3 ± 0.3 V. Changed wording referencing Figure 4 to refer to the MPC8241. Section 1.4.2—Table 6: Updated values for thermal characterization data as per the new packaging and 266-MHz part. Added note 7 for the difference between the 166-/200-MHz and the 266-MHz packaging. Section 1.4.3—Corrected the voltage listing for the 266-MHz part to 1.8 ± 0.1 V in Table 7. Section 1.5—Changed package parameters and illustration based on new packaging. Section 1.6—Table 18: Modified PLL configuration for 166- and 200-MHz parts for mode 7 to specify that this mode is not available for Rev. D of the part. Added sentence to note 1 referencing update for mode 7. Table 19: Made several range updates for various modes to accommodate VCO limits. Added mode 7 and 1E updates for Rev. D. Updated VCO limits listed in notes 4, 6, and 7.
2	—	Section 1.4.1.2—Updated note 1 to include 266-MHz part. Added a line to cautions 2 and 3 in the notes section of Table 2. Added Figures 4 and 5 to show the overshoot and undershoot requirements for the PCI interface. Section 1.4.1.3—Table 3: Updated minimum value for input high voltage, and maximum value for capacitance. Section 1.4.3.2—Appended Figures 9 and 10. Section 1.4.3.4—Added a column to Table 13 to include 133-MHz memory bus speed for 266-MHz part. Section 1.5.2—Changed Figure 24 to accommodate new package offerings. Section 1.6—Added Table 19 for PLL of the 266-MHz part. Section 1.7.7—Corrected note numbering in COP connector diagram. Section 1.9.1—Updated package description in part marking nomenclature.

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Document Number: MPC8241EC
Rev. 10
02/2009

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