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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8241tzq166d

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I_2O interface), and an I^2C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, 16-Kbyte instruction cache, 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

An internal peripheral logic bus interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade performance for power consumption. The processor core is clocked from a separate PLL that is referenced to the peripheral logic PLL, allowing the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8241 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The general-purpose processor core and peripheral logic serve a variety of embedded applications. The MPC8241 can be used as either a PCI host or PCI agent controller.

2 Features

Major features of the MPC8241 are as follows:

- Processor core
  - — High-performance, superscalar processor core
  - — Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and a branch processing unit (BPU)
  - — 16-Kbyte instruction cache
  - — 16-Kbyte data cache
  - — Lockable L1 caches—entire cache or on a per-way basis up to three of four ways
  - — Dynamic power management—supports 60x nap, doze, and sleep modes
- Peripheral logic
  - — Peripheral logic bus
    - – Various operating frequencies and bus divider ratios
    - – 32-bit address bus, 64-bit data bus
    - – Full memory coherency
    - – Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - – Store gathering on peripheral logic bus-to-PCI writes
  - — Memory interface
    - – Up to 2 Gbytes of SDRAM memory
    - – High-bandwidth data bus (32- or 64-bit) to SDRAM
    - – Programmable timing for SDRAM
    - – One to 8 banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices

- Write buffering for PCI and processor accesses
- Normal parity, read-modify-write (RMW), or ECC
- Data-path buffering between memory interface and processor
- Low-voltage TTL logic (LVTTL) interfaces
- 272 Mbytes of base and extended ROM/Flash/PortX space
- Base ROM space for 8-bit data path or same size as the SDRAM data path (32- or 64-bit)
- Extended ROM space for 8-, 16-, 32-bit gathering data path, 32- or 64-bit (wide) data path
- PortX: 8-, 16-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing, data ready input signal ($\overline{\text{DRDY}}$), and 4 chip selects

— 32-bit PCI interface
- Operates up to 66 MHz
- PCI 2.2-compatible
- PCI 5.0-V tolerance
- Dual address cycle (DAC) for 64-bit PCI addressing (master only)
- PCI locked accesses to memory
- Accesses to PCI memory, I/O, and configuration spaces
- Selectable big- or little endian operation
- Store gathering of processor-to-PCI write and PCI-to-memory write accesses
- Memory prefetching of PCI read accesses
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)
- PCI agent mode capability
- Address translation with two inbound and outbound units (ATU)
- Internal configuration registers accessible from PCI

— Two-channel integrated DMA controller (writes to ROM/PortX not supported)
- Direct mode or chaining mode (automatic linking of DMA transfers)
- Scatter gathering—read or write discontinuous memory
- 64-byte transfer queue per channel
- Interrupt on completed segment, chain, and error
- Local-to-local memory
- PCI-to-PCI memory
- Local-to-PCI memory
- PCI memory-to-local memory

— Message unit
- Two doorbell registers
- Two inbound and two outbound messaging registers
- I_2O message interface

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8241.

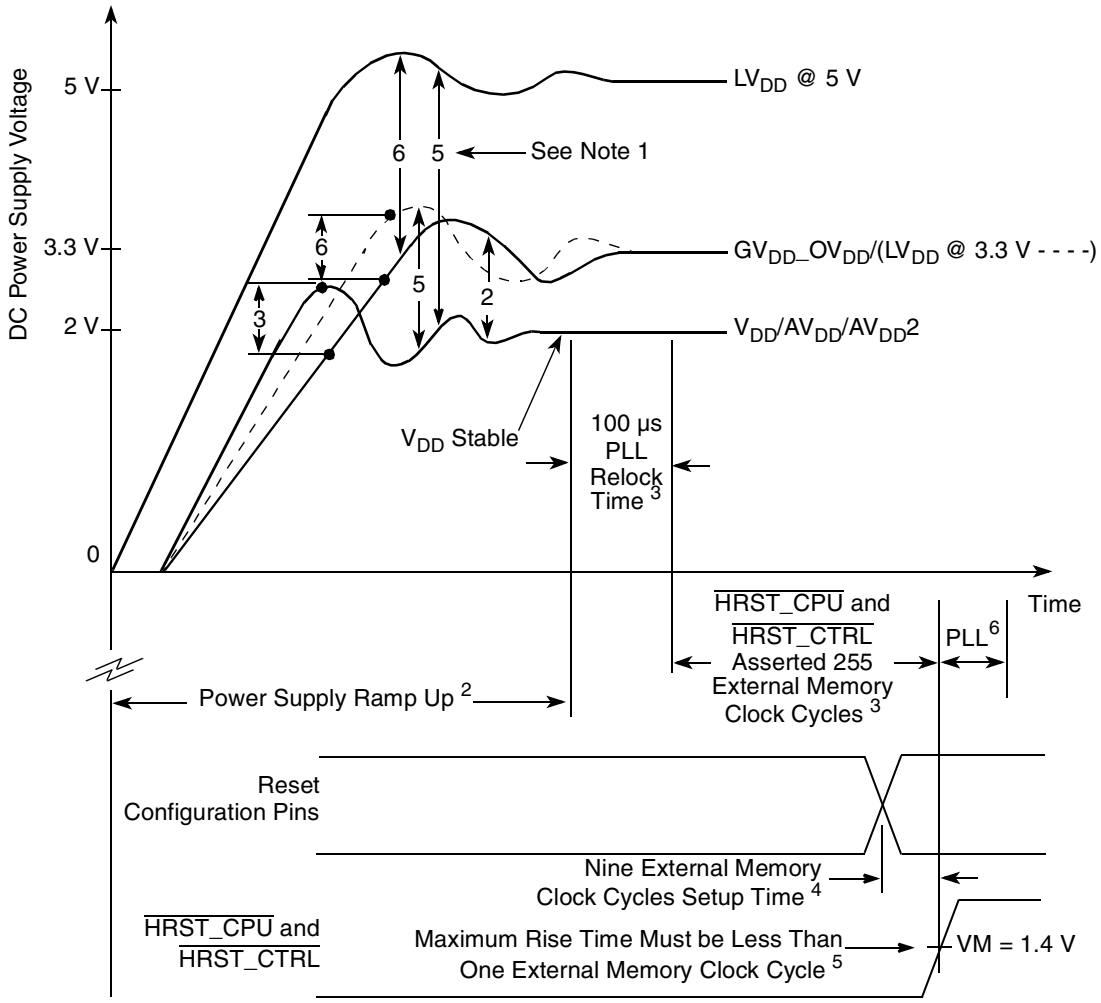
Table 2. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply voltage		V_{DD}	1.8 ± 100 mV	V	2
I/O buffer supply for PCI and standard; supply voltages for memory bus drivers		$GV_{DD}\_OV_{DD}$	3.3 ± 0.3	V	2
CPU PLL supply voltage		AV_{DD}	1.8 ± 100 mV		2
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8 ± 100 mV	V	2
PCI reference		LV_{DD}	5.0 ± 5%	V	4, 5, 6
			3.3 ± 0.3	V	5, 6, 7
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	4, 7
	All other inputs		0 to 3.6	V	8
Die-junction temperature		T_j	0 to 105	•C	

Notes:

1. Freescale has tested these operating conditions and recommends them. Proper device operation outside of these conditions is not guaranteed.
2. **Caution:** $GV_{DD}\_OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 1.8 V at any time including during power-on reset. Note that $GV_{DD}\_OV_{DD}$ pins are all shorted together: This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. Connections should not be made to individual PWRRING pins.
3. **Caution:** $V_{DD}/AV_{DD}/AV_{DD}2$ must not exceed $GV_{DD}\_OV_{DD}$ by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 5.0 V DC power supply.
5. **Caution:** LV_{DD} must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** LV_{DD} must not exceed $GV_{DD}\_OV_{DD}$ by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3 V DC power supply.
8. **Caution:** Input voltage (V_{in}) must not be greater than the supply voltage ($V_{DD}/AV_{DD}/AV_{DD}2$) by more than 2.5 V at all times including during power-on reset. Input voltage (V_{in}) must not be greater than $GV_{DD}\_OV_{DD}$ by more than 0.6 V at all times including during power-on reset.

Figure 2 shows supply voltage sequencing and separation cautions.



Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. See the Cautions section of Table 2 for details on this topic.
3. Refer to Table 8 for details on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for details on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.
6. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ negate in order to be latched.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Figure 3 shows the undershoot and overshoot voltage of the memory interface.

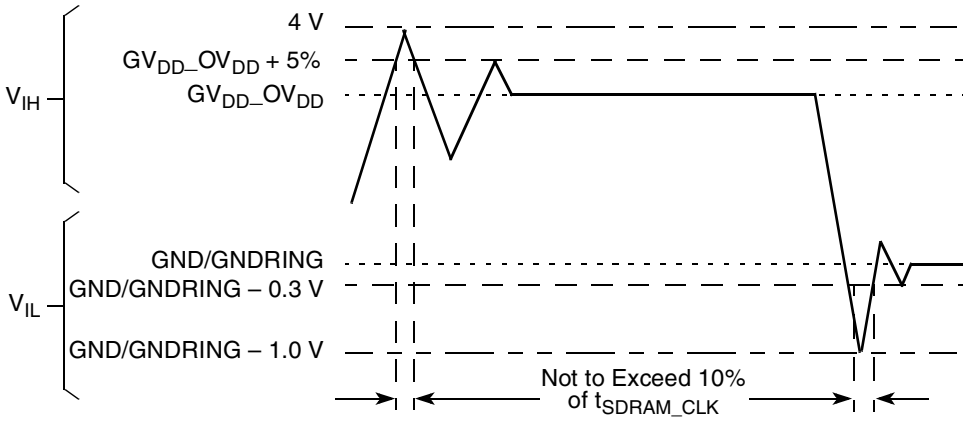


Figure 3. Overshoot/Undershoot Voltage

Figure 4 and Figure 5 show the undershoot and overshoot voltage of the PCI interface for the 3.3- and 5-V signals, respectively.

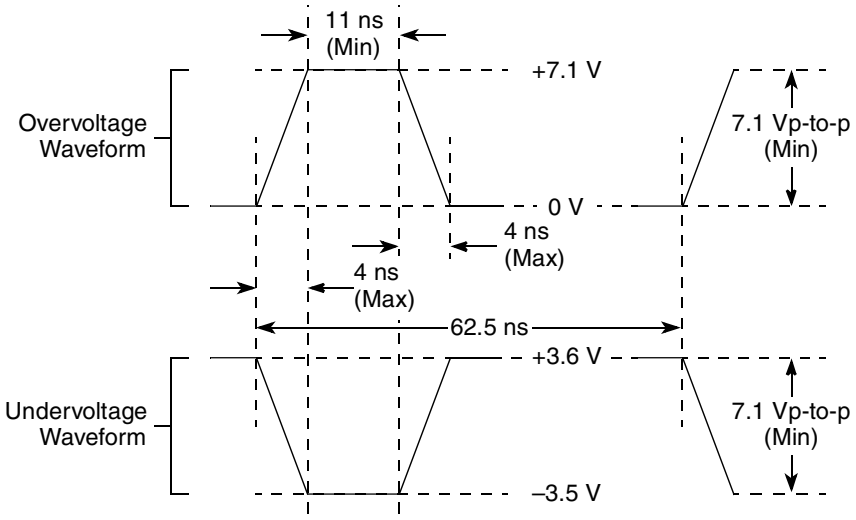


Figure 4. Maximum AC Waveforms for 3.3-V Signaling

Table 3. DC Electrical Specifications (continued)

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Capacitance	V_{in} = 0 V, f = 1 MHz	C_{in}	—	16.0	pF	

Notes:
1. See Table 16 for pins with internal pull-up resistors.
2. All grounded pins are connected together.
3. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} or both GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} must vary in the same direction.
4. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 16.

4.2.1 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 16. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8241 Output Pins [5, 6]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20 (default)	GV_{DD}_OV_{DD} = 3.3 V	36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)		89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) where table entry voltage = GV_{DD}_OV_{DD} – PCI V_{OH}.
2. For all others with GV_{DD}_ OV_{DD} = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = GV_{DD}_OV_{DD} – V_{OH}.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.
4. For all others with GV_{DD}_OV_{DD} = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4-V table entry.
5. See driver bit details for output driver control register (0x73) in the *MPC8245 Integrated Processor Reference Manual*.
6. See Chip Errata No. 19 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*.

4.3 Power Characteristics

Table 5 provides preliminary estimated power consumption data for the MPC8241.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)							Unit	Notes
	33/66/133	33/66/166	33/66/200	33/100/200	66/100/200	66/66/ 266	66/133/ 266		
Typical	0.7	0.8	1.0	1.0	1.0	1.5	1.8	W	1, 5
Max—CFP	0.8	1.0	1.2	1.3	1.3	1.9	2.1	W	1, 2
Max—INT	0.8	0.9	1.0	1.2	1.2	1.6	1.8	W	1, 3
Doze	0.5	0.6	0.7	0.8	0.8	1.0	1.3	W	1, 4, 6
Nap	0.2	0.2	0.3	0.4	0.4	0.4	0.7	W	1, 4, 6
Sleep	0.2	0.2	0.2	0.2	0.3	0.2	0.4	W	1, 4, 6
I/O Power Supplies [7]									
Mode	**Minimum**				**Maximum**			**Unit**	**Notes**
GV_{DD}_OV_{DD}	500				1130			mW	8

Notes:

1. The values include V_{DD}, AV_{DD}, and $AV_{DD}2$ but do not include I/O supply power.
2. Maximum—FP power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.
3. Maximum—INT power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at V_{DD} = 1.9 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at V_{DD} = AV_{DD} = 1.8 V, GV_{DD}_OV_{DD} = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. Power consumption of PLL supply pins (AV_{DD} and $AV_{DD}2$) < 15 mW, guaranteed by design, but not tested.
8. The typical maximum GV_{DD}_OV_{DD} value resulted from the MPC8241 operating at the fastest frequency combination of 66:133:266 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory and on 64-bit boundaries to local memory.

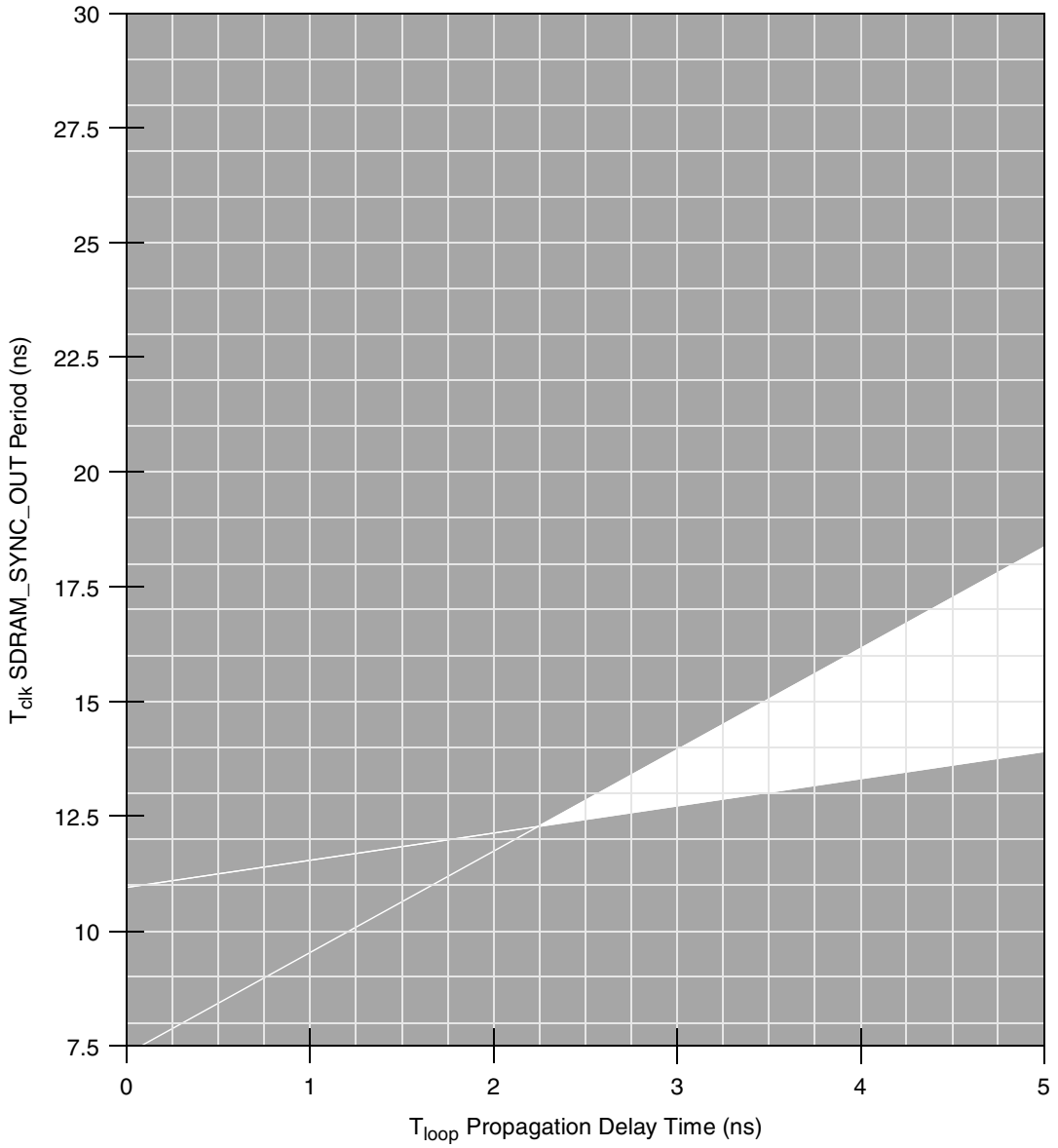


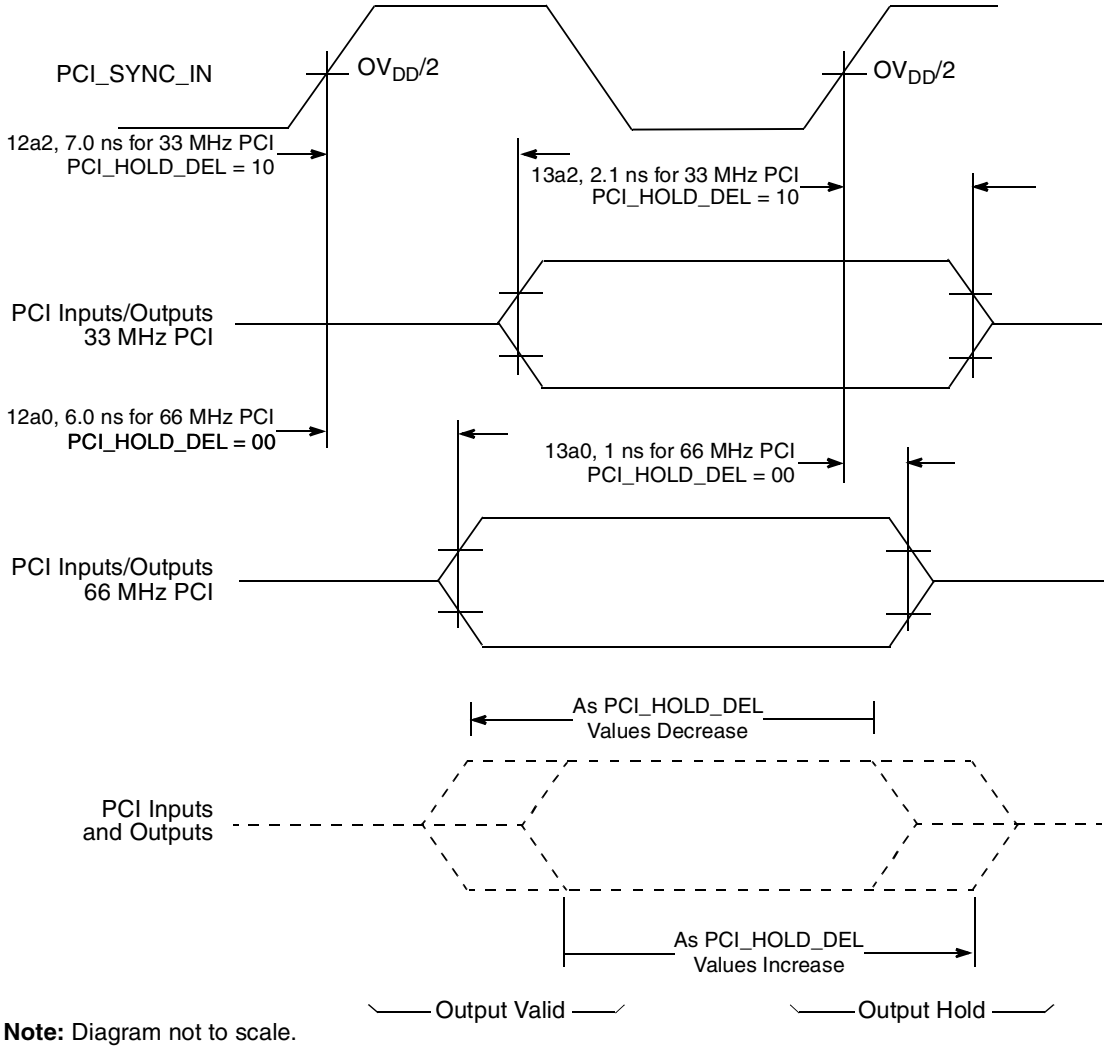
Figure 10. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=1 and Max Tap Delay

4.5.2 Input AC Timing Specifications

Table 10 provides the input AC timing specifications at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. See Figure 11 and Figure 12.

Table 10. Input AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
10a	PCI input signals valid to PCI_SYNC_IN (input setup)	3.0	—	ns	1, 3
10b	Memory input signals valid to *sys_logic_clk* (input setup)				



Note: Diagram not to scale.

Figure 15. PCI_HOLD_DEL Effect on Output Valid and Hold Time

4.6 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8241.

4.6.1 I²C DC Electrical Characteristics

Table 12 provides the DC electrical characteristics for the I²C interfaces.

Table 12. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
$\overline{\text{RCS1}}$	B9	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
$\overline{\text{RCS2}}$/TRIG_IN	P18	I/O	$GV_{DD}\_OV_{DD}$	—	5, 12
$\overline{\text{RCS3}}$/TRIG_OUT	N18	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	5
SDMA[1:0]	A15 B15	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1, 10, 11
SDMA[11:2]	A11 B12 A12 C12 B13 C13 D12 A14 C14 B14	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1
$\overline{\text{DRDY}}$	P1	Input	$GV_{DD}\_OV_{DD}$	—	12, 13
SDMA12/$\overline{\text{SRESET}}$	L3	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA13/TBEN	K3	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA14/$\overline{\text{CHKSTOP\_IN}}$	K2	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDBA1	C11	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
SDBA0	B11	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
PAR[0:7]	E19 C19 D5 D6 E16 F17 B2 C1	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1
$\overline{\text{SDRAS}}$	B19	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10
$\overline{\text{SDCAS}}$	D16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10
CKE	C6	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{\text{WE}}$	B16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
$\overline{\text{AS}}$	A16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
PIC Control Signals					
IRQ0/S_INT	P4	Input	$GV_{DD}\_OV_{DD}$	—	—
IRQ1/S_CLK	R2	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
IRQ2/S_RST	U19	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
IRQ3/$\overline{\text{S\_FRAME}}$	P15	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
IRQ4/$\overline{\text{L\_INT}}$	P2	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
I^2C Control Signals					
SDA	P17	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	8, 12
SCL	R19	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	8, 12
DUART Control Signals					
SOUT1/PCI_CLK0	T16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14
SIN1/PCI_CLK1	U16	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14, 24
SOUT2/$\overline{\text{RTS1}}$/PCI_CLK2	W18	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14
SIN2/$\overline{\text{CTS1}}$/PCI_CLK3	V19	I	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14, 24
Clock-Out Signals					
PCI_CLK0/SOUT1	T16	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI_CLK	5, 14

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
TMS	T18	Input	GV_{DD}_OV_{DD}	—	6, 13
$\overline{TRST}$	R16	Input	GV_{DD}_OV_{DD}	—	6, 13
Power and Ground Signals					
GNDRING/GND	F07 F08 F09 F10 F11 F12 F13 G07 G08 G09 G10 G11 G12 G13 H07 H08 H09 H10 H11 H12 H13 J07 J08 J09 J10 J11 J12 J13 K07 K08 K09 K10 K11 K12 K13 L07 L08 L09 L10 L11 L12 L13 M07 M08 M09 M10 M11 M12 M13 N07 N08 N09 N10 N11 N12 N13 P08 P09 P10 P11 P12 P13 R15	Ground	—	—	17
LV_{DD}	R18 U18 T1 U4 T6 W11 T14	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	—
GV_{DD}_OV_{DD}/PWRRING	D09 D10 D11 E06 E07 E08 E09 E10 E11 E12 E13 E14 F06 F14 G06 G14 H06 H14 J06 J14 K06 K14 L06 L14 M06 M14 N06 N14 P06 P07 P14 R08 R09 R10 R11 R12	Power for memory drivers and PCI/Stnd 3.3 V	GV_{DD}_OV_{DD}	—	18
V_{DD}	F03 H3 L5 N4 P5 V5 U8 W12 W16 R13 P19 L19 H19 F19 F15 C15 A13 A8 B5 A2	Power for core 1.8 V	V_{DD}	—	—
No Connect	N5 W2 B1	—	—	—	—
AV_{DD}	M5	Power for PLL (CPU core logic) 1.8 V	AV_{DD}	—	—
$AV_{DD}2$	R14	Power for PLL (peripheral logic) 1.8 V	$AV_{DD}2$	—	—
Debug/Manufacturing Pins					
DA0/$\overline{QACK}$	A3	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5, 11, 12
DA1/CKO	L1	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5
DA2	R5	Output	GV_{DD}_OV_{DD}	DRV_PCI	19
DA3/PCI_CLK4	V17	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5
DA4/$\overline{REQ4}$	W13	I/O	GV_{DD}_OV_{DD}	—	5, 6
DA5/$\overline{GNT4}$	T11	Output	GV_{DD}_OV_{DD}	DRV_PCI	2, 4, 5

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
DA[10:6]/ PLL_CFG[0:4]	N3 N2 N1 M4 M3	I/O	GV_{DD}_OV_{DD}	—	1, 5, 20
DA[11]	T13	Output	GV_{DD}_OV_{DD}	DRV_PCI	1, 19
DA[12:13]	M16 N16	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	19
DA[14:15]	B6 D8	Output	GV_{DD}_OV_{DD}	DRV_MEM_CTRL	1, 19

Notes:

1. Multi-pin signals such as AD[31:0] or MDL[0:31] physical package pin numbers are listed in order corresponding to the signal names. Ex: AD0 is on pin U1, AD1 is on pin U2,..., AD31 is on pin U13.
2. This pin is affected by a programmable PCI_HOLD_DEL parameter.
3. A weak pull-up resistor (2–10 kΩ) should be placed on this PCI control pin to LV_{DD}.
4. $\overline{\text{GNT4}}$ is a reset configuration pin with an internal pull-up resistor that is enabled only when in the reset state.
5. This pin is a multiplexed signal and appears more than once in this table.
6. This pin has an internal pull-up resistor that is enabled at all times. The value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
7. This pin is a sustained three-state pin as defined by the *PCI Local Bus Specification* (Rev. 2.2).
8. This pin is an open-drain signal.
9. DL[0] is a reset configuration pin with an internal pull-up resistor that is enabled only when in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
10. This pin has an internal pull-up resistor that is enabled only when in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
11. This pin is a reset configuration pin.
12. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to GV_{DD}_OV_{DD}.
13. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 3.
14. External PCI clocking source or fanout buffer may be required for system if using the MPC8241 DUART functionality because PCI_CLK[0:3] are not available in DUART mode. Only PCI_CLK4 is available in DUART mode.
15. OSC_IN uses the 3.3-V PCI interface driver, which is 5-V tolerant. See Table 2 for details.
16. This pin can be programmed as driven (default) or as open-drain (in MIOCR 1).
17. All grounded pins are connected together. Connections should not be made to individual pins. The list represents the balls that are connected to ground.
18. GV_{DD}_OV_{DD} must not exceed V_{DD}/AV_{DD}/AV_{DD}2 by more than 1.8 V at any time including during power-on reset. Note that GV_{DD}_OV_{DD} pins are all shorted together, PWRRING. The list represents the balls that are connected to PWRRING. Connections should not be made to individual PWRRING pins.
19. Treat these pins as no connects unless debug address functionality is used.
20. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ in order to be latched.
21. Place a pull-up resistor of 120 Ω or less on the $\overline{\text{TEST0}}$ pin.
22. SDRAM_CLK[0:3] and SDRAM_SYNC_OUT signals use DRV_MEM_CTRL for chip Rev. 1.1 (A). These signals use DRV_MEM_CLK for chip Rev. 1.2B.
23. The driver capability of this pin is hardwired to 40 Ω and cannot be changed.
24. Freescale typically expects that customers using the serial port will have sufficient drivers available in the RS232 transceiver to drive the $\overline{\text{CTS}}$ pin actively as an input if they are using that mode. No pullups would be needed in these circumstances.
25. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state

Table 17. PLL Configurations (166- and 200-MHz) (continued)

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1E	11110[14]	Not usable			Not usable			Off	Off
1F	11111[14]	Not usable			Not usable			Off	Off

Notes:

1. PLL_CFG[0:4] settings not listed are reserved. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value. Note the impact of the relevant revisions for mode 7.
2. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
3. Limited by maximum PCI input frequency (66 MHz).
4. Limited by minimum CPU VCO frequency (300 MHz).
5. Limited by maximum CPU operating frequency.
6. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
7. Limited by minimum CPU operating frequency (100 MHz).
8. Limited due to maximum memory VCO frequency (352 MHz).
9. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
10. Limited by maximum CPU VCO frequency (704 MHz).
11. Limited by maximum system memory interface operating frequency (83 MHz @ 166 MHz CPU bus speed).
12. Limited by maximum system memory interface operating frequency (100 MHz @ 200 MHz CPU bus speed).
13. Limited by minimum memory VCO frequency (132 MHz).
14. In clock off mode, no clocking occurs inside the MPC8241, regardless of the PCI_SYNC_IN input.

Table 18. PLL Configurations (266-MHz Parts)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	25–35[5]	75–105	188–263	3 (2)	2.5 (2)
1	00001	25–29[5]	75–88	225–264	3 (2)	3 (2)
2	00010	50[15]–59[5]	50–59	225–266	1 (4)	4.5 (2)
3	00011[12]	50[14]–66[1]	50–66	100–133	1 (Bypass)	2 (4)
4	00100	25–44[4]	50–88	100–176	2 (4)	2 (4)

Place the circuits as closely as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing from the capacitors to the input signal pins should be as direct as possible with minimal inductance of vias.

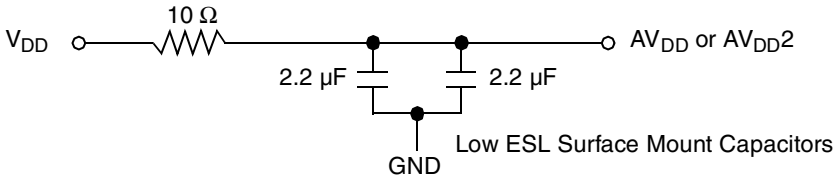


Figure 26. PLL Power Supply Filter Circuit

7.2 Decoupling Recommendations

Dynamic power management, large address and data buses, and high operating frequencies enable the MPC8241 to generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8241 system, and the MPC8241 itself requires a clean, tightly regulated source of power. Therefore, place at least one decoupling capacitor at each V_{DD}, GV_{DD}_OV_{DD}, and LV_{DD} pin. These decoupling capacitors receive their power from dedicated power planes in the PCB, using short traces to minimize inductance. These capacitors should have a value of 0.1 µF. To minimize lead inductance, use only ceramic SMT (surface mount technology) capacitors, preferably 0508 or 0603, on which connections are made along the length of the part.

In addition, distribute several bulk storage capacitors around the PCB to feed the V_{DD}, GV_{DD}_OV_{DD}, and LV_{DD} planes and enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the necessary quick response time, and should be connected to the power and ground planes through two vias to minimize inductance. Freescale recommends using bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

7.3 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Tie unused active-low inputs to OV_{DD}. Connect unused active-high inputs to GND. All no connect (NC) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}_OV_{DD}, LV_{DD}, and GND pins.

The PCI_SYNC_OUT signal is to be routed halfway out to the PCI devices and then returned to the PCI_SYNC_IN input.

The SDRAM_SYNC_OUT signal is to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the MPC8241. The trace length can be used to skew or adjust the timing window as needed. See the Tundra *Tsi107™ Design Guide* (AN1849) and Freescale application notes AN2164/D, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1* and AN2746, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part* 2 for more details. Note the SDRAM_SYNC_IN to PCI_SYNC_IN time requirement (see Table 10).

7.4 Pull-Up/Pull-Down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: MDH[0:31], MDL[0:31], and PAR[0:7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (MDL[0:31] and PAR[4:7]) are disabled, and their outputs drive logic zeros when they would otherwise be driven. For this mode, these pins do not require pull-up resistors and should be left unconnected to minimize possible output switching.

The $\overline{\text{TEST0}}$ pin requires a pull-up resistor of 120 Ω or less connected to GV_{DD}_OV_{DD}.

RTC should have weak pull-up resistors (2–10 kΩ) connected to GV_{DD}_OV_{DD} and that the following signals should be pulled up to GV_{DD}_OV_{DD} with weak pull-up resistors (2–10 kΩ): SDA, SCL, $\overline{\text{SMI}}$, $\overline{\text{SRESET}}$/SDMA12, TBEN/SDMA13, $\overline{\text{CHKSTOP\_IN}}$/SDMA14, TRIG_IN/$\overline{\text{RCS2}}$, $\overline{\text{QACK}}$/DA0, and $\overline{\text{DRDY}}$.

The following PCI control signals should be pulled up to LV_{DD} (the clamping voltage) with weak pull-up resistors (2–10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, and $\overline{\text{TRDY}}$. The resistor values may need to have stronger adjustment to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[3:0], $\overline{\text{REQ4}}$/DA4, TCK, TDI, TMS, and $\overline{\text{TRST}}$. See Table 16.

The following pins have internal pull-up resistors that are enabled only while the device is in the reset state: $\overline{\text{GNT4}}$/DA5, MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, MAA[0:2], and PMAA[0:2]. See Table 16.

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST\_CPU}}$ and $\overline{\text{HRST\_CTRL}}$.

Reset configuration pins should be tied to GND by means of 1-kΩ pull-down resistors to ensure that a logic zero level is read into the configuration bits during reset if the default logic-one level is not desired.

Any other unused active low input pins should be tied to a logic-one level by means of weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND by means of weak pull-down resistors (2–10 kΩ).

7.5 PCI Reference Voltage—LV_{DD}

The MPC8241 PCI reference voltage (LV_{DD}) pins should be connected to 3.3 ± 0.3 V power supply if interfacing the MPC8241 into a 3.3-V PCI bus system. Similarly, the LV_{DD} pins should be connected to 5.0 V ± 5% power supply if interfacing the MPC8241 into a 5-V PCI bus system. For either reference voltage, the MPC8241 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8241 tolerates 5-V signals when interfaced into a 5-V PCI bus system. (See Errata No. 18 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*).

7.6 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port, with additional status monitoring signals. The COP port must independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 27 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 27, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 27. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 27 is common to all known emulators.

7.7 Thermal Management

This section provides thermal management information for the plastic ball grid array (PBGA) package for air-cooled applications. Depending on the application environment and the operating frequency, a heat sink may be required to maintain junction temperature within specifications. Proper thermal control design primarily depends on the system-level design: heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks can be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, or mounting clip and screw assembly (see Figure 28).

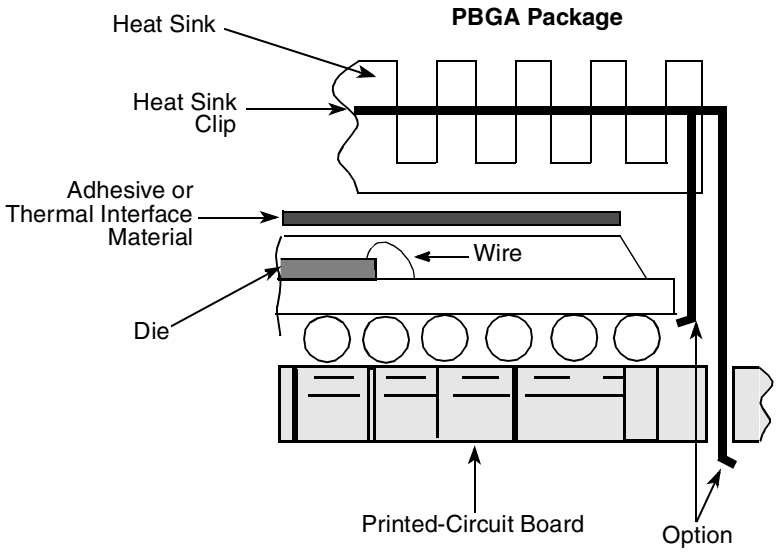


Figure 28. Package Exploded Cross-Sectional View with Several Heat Sink Options

Figure 29 depicts the die junction-to-ambient thermal resistance for four typical cases:

- A heat sink is not attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s).
- A heat sink is not attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s/sink).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p/sink).

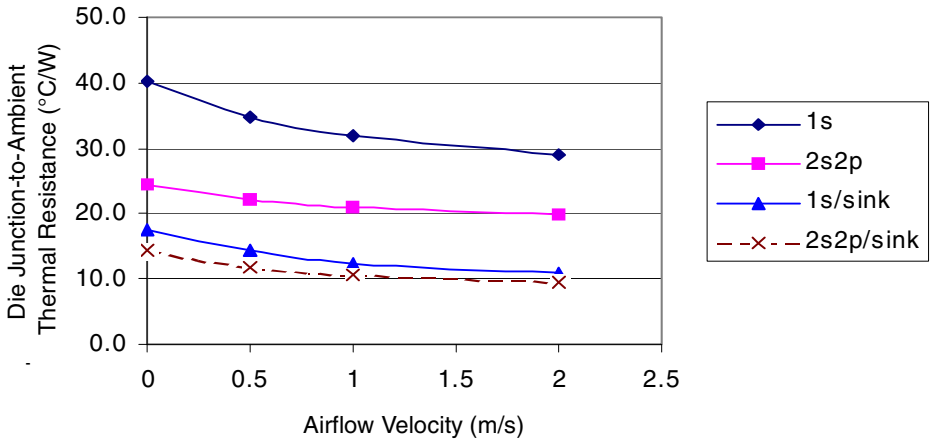


Figure 29. Die Junction-to-Ambient Resistance

The board designer can choose among several types of heat sinks to place on the MPC8241. Several commercially available heat sinks for the MPC8241 are provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

7.7.3 Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (ψ_{JT}) measures the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\psi_{JT} \times P_D)$$

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
8	12/19/2005	Document—Imported new template and made minor editoral corrections. Section 4.3.1—Before Figure 7, added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3. Section 4.3.2—After Figure 12, added a sentence to introduce Figure 13. Section 4.3.3—After Table 11, added a sentence to introduce Figure 14. Section 4.3.4—After Table 13, added to the sentence to introduce Figures 16 thru 19. Section 4.3.6—After Table 16, added a sentence to introduce Figures 22 thru 25. Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2. Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated Section 9.2 to reflect what we offer for new orders. Updated Figure 34 to match with current part marking format. Section 8.3—Added new section for part marking information.
7	05/11/2004	Section 4.1.4 —Table 4: Changed the default for drive strength of DRV_STD_MEM. Section 4.3.1 —Table 8: Changed the wording for item 15 description. Section 4.3.4 —Table 10: Changed T_{os} range and wording in note 7; Figure 11: changed wording for SDRAM_SYNC_IN description relative to T_{OS}.
6.1	—	Section 4.3.1 — Table 9: Corrected last row to state the correct description for the bit setting: Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay”
6	—	Section 4.1.2 — Figure 2: Added note 6 and related label for latching of the PLL_CFG signals. Section 4.1.3 — Updated specifications for the input high and input low voltages of PCI_SYNC_IN. Section 4.3.1 — Table 8: Corrected typo for first number 1a to 1; Updated characteristics for the DLL lock range for the default and remaining three DLL locking modes; Reworded note description for note 6. Replaced contents of Table 9 with bit descriptions for the four DLL locking modes. In Figures 7 through 10, updated the DLL locking mode graphs. Section 4.3.2 — Table 10: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 4.3.3— Table 11: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 5.3 — Table 17: Removed extra listing of DRDY in test/configuration signal list and updated relevant notes for signal in memory Interface signal listing. Updated note #20. Added note 24 for the signals of the UART interface. Section 7.6 — Added relevant notes to this section and updated Figure 29.
5	—	Section 5.1— Updated package information to include all package offerings. Section 5.2 — Included package case outline for ZP (Rev. B) packaging parts. Section 9 — Updated Part markings for the offerings of the MPC8241. All sections — Nontechnical reformatting