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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8241tzq200d

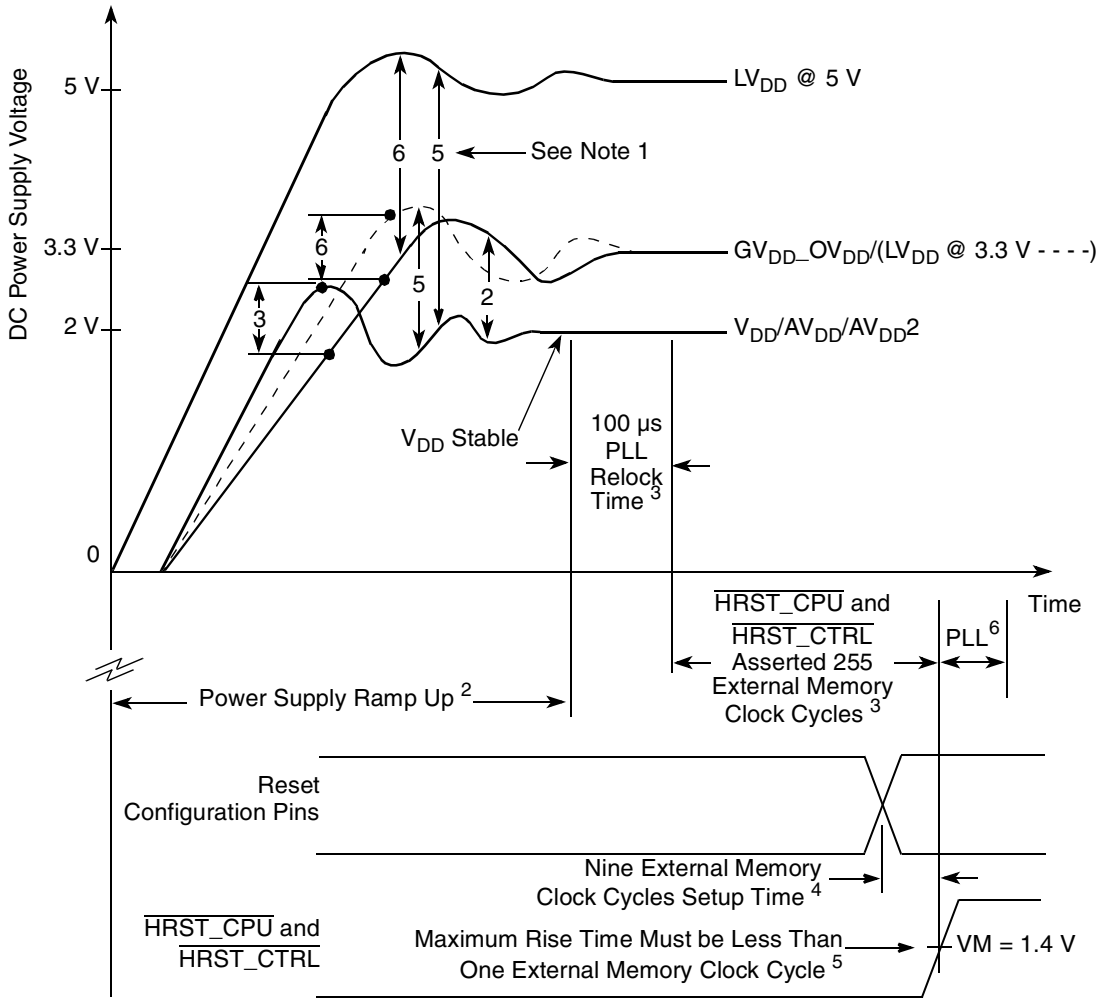
- Write buffering for PCI and processor accesses
- Normal parity, read-modify-write (RMW), or ECC
- Data-path buffering between memory interface and processor
- Low-voltage TTL logic (LVTTL) interfaces
- 272 Mbytes of base and extended ROM/Flash/PortX space
- Base ROM space for 8-bit data path or same size as the SDRAM data path (32- or 64-bit)
- Extended ROM space for 8-, 16-, 32-bit gathering data path, 32- or 64-bit (wide) data path
- PortX: 8-, 16-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing, data ready input signal ($\overline{\text{DRDY}}$), and 4 chip selects

— 32-bit PCI interface
- Operates up to 66 MHz
- PCI 2.2-compatible
- PCI 5.0-V tolerance
- Dual address cycle (DAC) for 64-bit PCI addressing (master only)
- PCI locked accesses to memory
- Accesses to PCI memory, I/O, and configuration spaces
- Selectable big- or little endian operation
- Store gathering of processor-to-PCI write and PCI-to-memory write accesses
- Memory prefetching of PCI read accesses
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)
- PCI agent mode capability
- Address translation with two inbound and outbound units (ATU)
- Internal configuration registers accessible from PCI

— Two-channel integrated DMA controller (writes to ROM/PortX not supported)
- Direct mode or chaining mode (automatic linking of DMA transfers)
- Scatter gathering—read or write discontinuous memory
- 64-byte transfer queue per channel
- Interrupt on completed segment, chain, and error
- Local-to-local memory
- PCI-to-PCI memory
- Local-to-PCI memory
- PCI memory-to-local memory

— Message unit
- Two doorbell registers
- Two inbound and two outbound messaging registers
- I_2O message interface

Figure 2 shows supply voltage sequencing and separation cautions.



Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. See the Cautions section of Table 2 for details on this topic.
3. Refer to Table 8 for details on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for details on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.
6. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ negate in order to be latched.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Table 3. DC Electrical Specifications (continued)

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Capacitance	V_{in} = 0 V, f = 1 MHz	C_{in}	—	16.0	pF	

Notes:
1. See Table 16 for pins with internal pull-up resistors.
2. All grounded pins are connected together.
3. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} or both GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} must vary in the same direction.
4. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 16.

4.2.1 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 16. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8241 Output Pins [5, 6]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20 (default)	GV_{DD}_OV_{DD} = 3.3 V	36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)		89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) where table entry voltage = GV_{DD}_OV_{DD} – PCI V_{OH}.
2. For all others with GV_{DD}_ OV_{DD} = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = GV_{DD}_OV_{DD} – V_{OH}.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.
4. For all others with GV_{DD}_OV_{DD} = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4-V table entry.
5. See driver bit details for output driver control register (0x73) in the *MPC8245 Integrated Processor Reference Manual*.
6. See Chip Errata No. 19 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*.

4.3 Power Characteristics

Table 5 provides preliminary estimated power consumption data for the MPC8241.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)							Unit	Notes
	33/66/133	33/66/166	33/66/200	33/100/200	66/100/200	66/66/ 266	66/133/ 266		
Typical	0.7	0.8	1.0	1.0	1.0	1.5	1.8	W	1, 5
Max—CFP	0.8	1.0	1.2	1.3	1.3	1.9	2.1	W	1, 2
Max—INT	0.8	0.9	1.0	1.2	1.2	1.6	1.8	W	1, 3
Doze	0.5	0.6	0.7	0.8	0.8	1.0	1.3	W	1, 4, 6
Nap	0.2	0.2	0.3	0.4	0.4	0.4	0.7	W	1, 4, 6
Sleep	0.2	0.2	0.2	0.2	0.3	0.2	0.4	W	1, 4, 6
I/O Power Supplies [7]									
Mode	**Minimum**				**Maximum**			**Unit**	**Notes**
GV_{DD}_OV_{DD}	500				1130			mW	8

Notes:

1. The values include V_{DD}, AV_{DD}, and $AV_{DD}2$ but do not include I/O supply power.
2. Maximum—FP power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.
3. Maximum—INT power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at V_{DD} = 1.9 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at V_{DD} = AV_{DD} = 1.8 V, GV_{DD}_OV_{DD} = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. Power consumption of PLL supply pins (AV_{DD} and $AV_{DD}2$) < 15 mW, guaranteed by design, but not tested.
8. The typical maximum GV_{DD}_OV_{DD} value resulted from the MPC8241 operating at the fastest frequency combination of 66:133:266 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory and on 64-bit boundaries to local memory.

4.4 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8241. For details, see Section 7.7, "Thermal Management."

Table 6. Thermal Characterization Data

Rating	Thermal Test Board Description	Symbol	Value [7] (166- and 200-MHz Parts)	Value [7] (266-MHz Part)	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	38	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JMA}$	25	20	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	31	22	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	22	17	°C/W	1, 3
Junction-to-board (bottom)	Four-layer board (2s2p)	$R_{\theta JB}$	17	11	°C/W	4
Junction-to-case (top)	Single-layer board (1s)	$R_{\theta JC}$	8	7	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	2	2	°C/W	6

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the board horizontal.
3. Per EIA/JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per EIA/JESD51-2.
7. Note that the 166- and 200-MHz parts are in a two-layer package and the 266-MHz part is in a four-layer package, which causes the two package types to have different thermal characterization data.

4.5 AC Electrical Characteristics

After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 8, "Ordering Information."

Register settings that define each DLL mode are shown in Table 9.

Table 9. DLL Mode Definition

DLL Mode	Bit 2 of Configuration Register at 0x76	Bit 7 of Configuration Register at 0x72
Normal tap delay, No DLL extend	0	0
Normal tap delay, DLL extend	0	1
Max tap delay, No DLL extend	1	0
Max tap delay, DLL extend	1	1

The DLL_MAX_DELAY bit can lengthen the amount of time through the delay line by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock is within the DLL lock range, there may be slightly more jitter in the output clock of the DLL if the phase comparator shifts the clock between adjacent tap points. Refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1*, for details on DLL modes and memory design.

The value of the current tap point after the DLL locks can be determined by reading bits 6–0 (DLL_TAP_COUNT) of the DLL tap count register (DTCR, located at offset 0xE3). These bits store the value (binary 0 through 127) of the current tap point and can indicate whether the DLL advances or decrements as it maintains the DLL lock. Therefore, for evaluation purposes, DTCR can be read for all DLL modes that support the T_{loop} value used for the trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN. The DLL mode with the smallest tap point value in the DTCR should be used because the bigger the tap point value, the more jitter that can be expected for clock signals. Keeping a DLL mode locked below tap point decimal 12 is not recommended.

Figure 13 shows the input timing diagram for mode select signals.

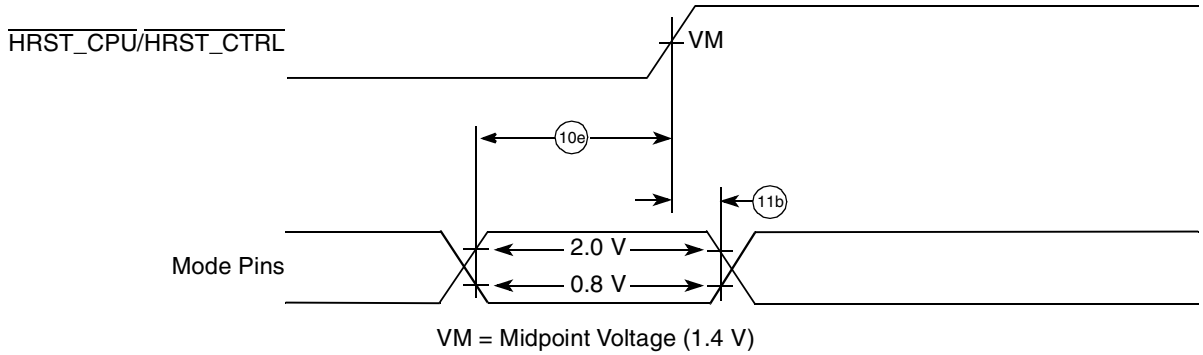


Figure 13. Input Timing Diagram for Mode Select Signals

4.5.3 Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V (see Figure 11). All output timings assume a purely resistive 50-Ω load (see Figure 14). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths that Table 4 indicates.

Table 11. Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, see Figure 15				
12a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{\text{MCP}}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{\text{MCP}}$,CKE] = 00	—	7.5		
12b	*sys_logic_clk* to output valid (memory address, control, and data signals)	—	4.5	ns	2
12c	*sys_logic_clk* to output valid (for all others)	—	7.0	ns	2
12d	*sys_logic_clk* to output valid (for I^2C)	—	5.0	ns	2
12e	*sys_logic_clk* to output valid (ROM/Flash/Port X)	—	6.0	ns	2
13a	Output hold (PCI), see Figure 15				
13a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{\text{MCP}}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{\text{MCP}}$,CKE] = 00	3.5	—		
13b	Output hold (all others)	1.0	—	ns	2
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	1, 3

Table 12. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8245 Integrated Processor Reference Manual* for information on the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if the OV_{DD} is switched off.

4.6.2 I^2C AC Electrical Specifications

Table 13 provides the AC timing parameters for the I^2C interfaces.

Table 13. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	µs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	µs
Data output delay time:	t_{I2OVKL}	—	0.9[3]	
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

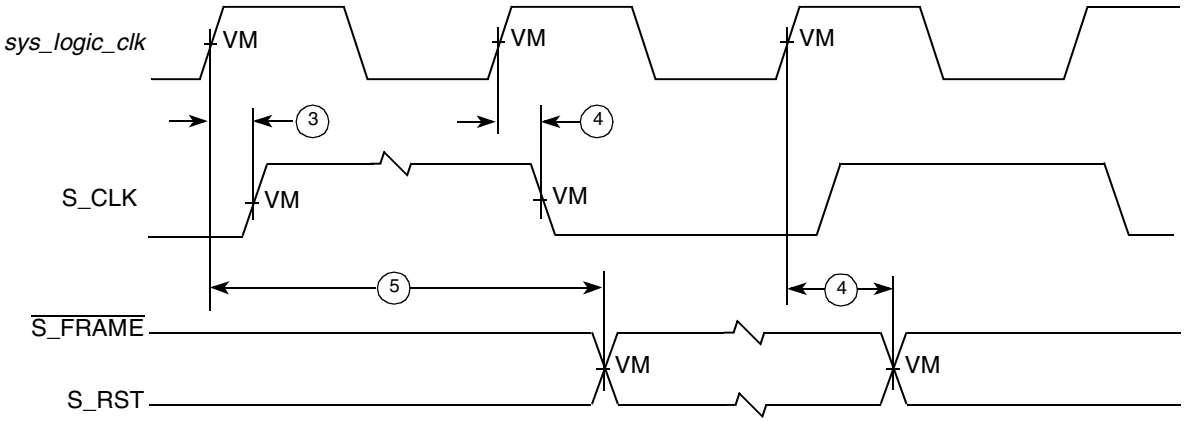


Figure 18. PIC Serial Interrupt Mode Output Timing Diagram

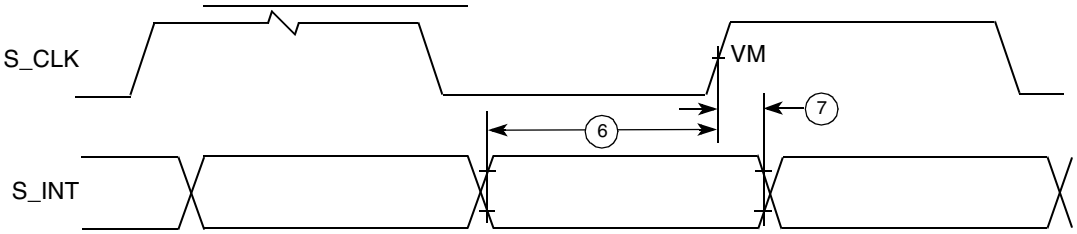


Figure 19. PIC Serial Interrupt Mode Input Timing Diagram

4.7.1 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 15 provides the JTAG AC timing specifications for the MPC8241 while in the JTAG operating mode at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	—
1	TCK cycle time	40	—	ns	—
2	TCK clock pulse width measured at 1.5 V	20	—	ns	—
3	TCK rise and fall times	0	3	ns	—
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$ assert time	10	—	ns	—
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	—

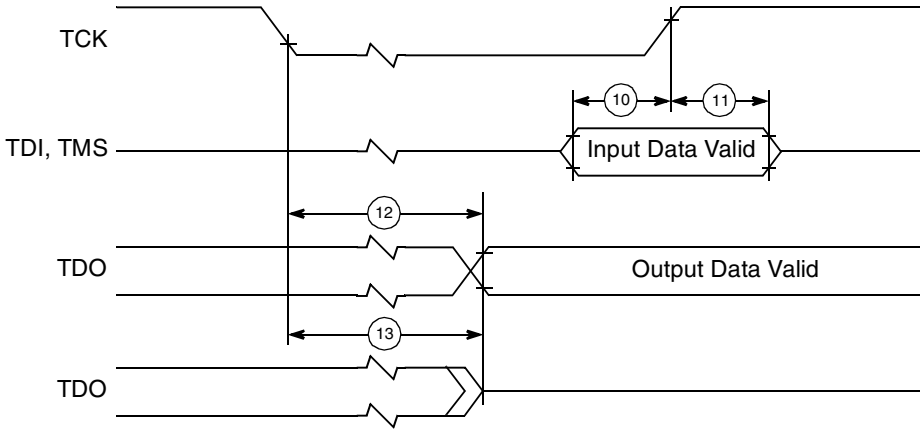


Figure 23. Test Access Port Timing Diagram

5 Package Description

This section details package parameters, pin assignments, and dimensions.

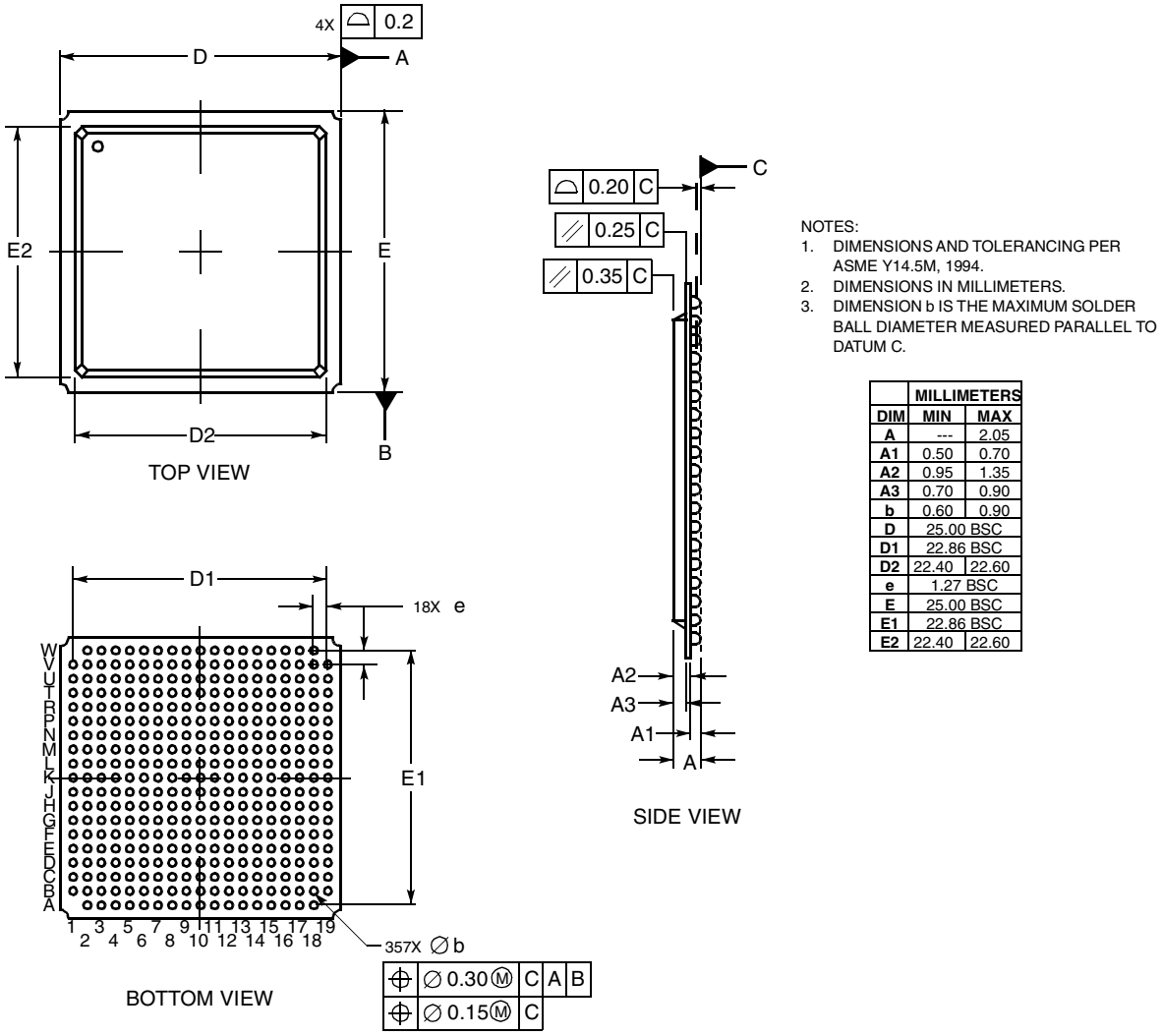
5.1 Package Parameters for the MPC8241

The MPC8241 uses a 25 mm × 25 mm, cavity up, 357-pin plastic ball grid array (PBGA) package. The package parameters are as follows.

Package outline	25 mm × 25 mm
Interconnects	357
Pitch	1.27 mm
Solder balls	ZP (PBGA)—62 Sn/36 Pb/2 Ag—available only in Rev B parts ZQ (Thick substrate thick mold cap PBGA)—62 Sn/36 Pb/2 Ag VR (Lead free version of package)—95.5 Sn/4.0 Ag/0.5 Cu
Solder ball diameter	0.75 mm
Maximum module height	2.52 mm
Co-planarity specification	0.15 mm
Maximum force	6.0 lbs. total, uniformly distributed over package (8 grams/ball)

5.2 Pin Assignments and Package Dimensions

Figure 24 shows the top surface, side profile, and pinout of the MPC8241, 357 PBGA ZP package. Note that this is available for Rev. B parts only.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.05
A1	0.50	0.70
A2	0.95	1.35
A3	0.70	0.90
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	22.40	22.60
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	22.40	22.60

Figure 24. MPC8241 Package Dimensions and Pinout Assignments (ZP Package)

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
TMS	T18	Input	GV_{DD}_OV_{DD}	—	6, 13
$\overline{TRST}$	R16	Input	GV_{DD}_OV_{DD}	—	6, 13
Power and Ground Signals					
GNDRING/GND	F07 F08 F09 F10 F11 F12 F13 G07 G08 G09 G10 G11 G12 G13 H07 H08 H09 H10 H11 H12 H13 J07 J08 J09 J10 J11 J12 J13 K07 K08 K09 K10 K11 K12 K13 L07 L08 L09 L10 L11 L12 L13 M07 M08 M09 M10 M11 M12 M13 N07 N08 N09 N10 N11 N12 N13 P08 P09 P10 P11 P12 P13 R15	Ground	—	—	17
LV_{DD}	R18 U18 T1 U4 T6 W11 T14	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	—
GV_{DD}_OV_{DD}/PWRRING	D09 D10 D11 E06 E07 E08 E09 E10 E11 E12 E13 E14 F06 F14 G06 G14 H06 H14 J06 J14 K06 K14 L06 L14 M06 M14 N06 N14 P06 P07 P14 R08 R09 R10 R11 R12	Power for memory drivers and PCI/Stnd 3.3 V	GV_{DD}_OV_{DD}	—	18
V_{DD}	F03 H3 L5 N4 P5 V5 U8 W12 W16 R13 P19 L19 H19 F19 F15 C15 A13 A8 B5 A2	Power for core 1.8 V	V_{DD}	—	—
No Connect	N5 W2 B1	—	—	—	—
AV_{DD}	M5	Power for PLL (CPU core logic) 1.8 V	AV_{DD}	—	—
$AV_{DD}2$	R14	Power for PLL (peripheral logic) 1.8 V	$AV_{DD}2$	—	—
Debug/Manufacturing Pins					
DA0/$\overline{QACK}$	A3	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5, 11, 12
DA1/CKO	L1	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5
DA2	R5	Output	GV_{DD}_OV_{DD}	DRV_PCI	19
DA3/PCI_CLK4	V17	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5
DA4/$\overline{REQ4}$	W13	I/O	GV_{DD}_OV_{DD}	—	5, 6
DA5/$\overline{GNT4}$	T11	Output	GV_{DD}_OV_{DD}	DRV_PCI	2, 4, 5

6 PLL Configuration

The PLL_CFG[0:4] are configured by the internal PLLs. For a specific PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations are shown in Table 17 and Table 18.

Table 17. PLL Configurations (166- and 200-MHz)

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	Not available			25-26[5]	75-78	188-195	3 (2)	2.5 (2)
2	00010	34[4]–37[5]	34–37	153–166	34[4]–44[5]	34–44	153–200	1 (4)	4.5 (2)
3	00011[6]	50[7]–66[3]	50–66	100–132	50[7]–66[3]	50–66	100–132	1 (Bypass)	2 (4)
4	00100	25–41[5]	50–82	100–164	25–44[8,10]	50–88	100–176	2 (4)	2 (4)
6	00110[9]	Bypass			Bypass			Bypass	Bypass
7 Rev. B	00111[6]	50[4]–55 [5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (Bypass)	3 (2)
7 Rev. D	00111	Not available							
8	01000	50[4]–55[5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (4)	3 (2)
9	01001	38[4]–41[5,11]	76–82	152–164	38[4]–50[5,12]	76–100	152–200	2 (2)	2 (2)
B	01011	Not available			44[5]	66	198	2(2)	2.5(2)
C	01100	30[4]–33[5]	60–66	150–165	30[4]–40[5]	60–80	150–200	2 (4)	2.5 (2)
E	01110	25–27[5]	50–54	150–162	25–33[5]	60–66	150–198	2 (4)	3 (2)
10	10000	25–27[5,11]	75–83	150–166	25–33[5,12]	75–100	150–200	3 (2)	2 (2)
12	10010	50[4]–55[5,11]	75–83	150–166	50[4]–66[3]	75–99	150–198	1.5 (2)	2 (2)
14	10100	Not available			25–28[5]	50–56	175–196	2 (4)	3.5 (2)
16	10110				25[5]	50	200	2(4)	4(2)
17	10111				25[5]	100	200	4(2)	2(2)
19	11001	33[5,13]	66	165	33[13]–40[5]	66–80	165–200	2(2)	2.5(2)
1A	11010	37[4]–41[5]	37–41	150–166	37[4]–50[5]	37–50	150–200	1 (4)	4 (2)
1B	11011	Not available			33[5,13]	66	198	2(2)	3(2)
1C	11100				44[5,13]	66	198	1.5(2)	3(2)
1D	11101	44[5,13]	66	166	44[13]–53[5]	66–80	165–200	1.5 (2)	2.5 (2)

Table 18. PLL Configurations (266-MHz Parts) (continued)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Off	Off

Notes:

1. Limited by maximum PCI input frequency (66 MHz).
2. Note the impact of the relevant revisions for modes 7 and 1E.
3. Limited by minimum memory VCO frequency (132 MHz).
4. Limited due to maximum memory VCO frequency (352 MHz).
5. Limited by maximum CPU operating frequency.
6. Limited by minimum CPU VCO frequency (300 MHz).
7. Limited by maximum CPU VCO frequency (704 MHz).
8. In clock off mode, no clocking occurs inside the MPC8241, regardless of the PCI_SYNC_IN input.
9. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
10. PLL_CFG[0:4] settings that are not listed are reserved.
11. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
12. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
13. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
14. Limited by minimum CPU operating frequency (100 MHz).
15. Limited by minimum memory bus frequency (50 MHz).

7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8241.

7.1 PLL Power Supply Filtering

The AV_{DD} and $AV_{DD}2$ power signals on the MPC8241 provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and $AV_{DD}2$ input signals should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 26 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD} and $AV_{DD}2$ power signal pins. In *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), Dr. Howard Johnson recommends using multiple small capacitors of equal value instead of multiple values.

7.4 Pull-Up/Pull-Down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: MDH[0:31], MDL[0:31], and PAR[0:7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (MDL[0:31] and PAR[4:7]) are disabled, and their outputs drive logic zeros when they would otherwise be driven. For this mode, these pins do not require pull-up resistors and should be left unconnected to minimize possible output switching.

The $\overline{\text{TEST0}}$ pin requires a pull-up resistor of 120 Ω or less connected to GV_{DD}_OV_{DD}.

RTC should have weak pull-up resistors (2–10 kΩ) connected to GV_{DD}_OV_{DD} and that the following signals should be pulled up to GV_{DD}_OV_{DD} with weak pull-up resistors (2–10 kΩ): SDA, SCL, $\overline{\text{SMI}}$, $\overline{\text{SRESET}}$/SDMA12, TBEN/SDMA13, $\overline{\text{CHKSTOP\_IN}}$/SDMA14, TRIG_IN/$\overline{\text{RCS2}}$, $\overline{\text{QACK}}$/DA0, and $\overline{\text{DRDY}}$.

The following PCI control signals should be pulled up to LV_{DD} (the clamping voltage) with weak pull-up resistors (2–10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, and $\overline{\text{TRDY}}$. The resistor values may need to have stronger adjustment to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[3:0], $\overline{\text{REQ4}}$/DA4, TCK, TDI, TMS, and $\overline{\text{TRST}}$. See Table 16.

The following pins have internal pull-up resistors that are enabled only while the device is in the reset state: $\overline{\text{GNT4}}$/DA5, MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, MAA[0:2], and PMAA[0:2]. See Table 16.

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST\_CPU}}$ and $\overline{\text{HRST\_CTRL}}$.

Reset configuration pins should be tied to GND by means of 1-kΩ pull-down resistors to ensure that a logic zero level is read into the configuration bits during reset if the default logic-one level is not desired.

Any other unused active low input pins should be tied to a logic-one level by means of weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND by means of weak pull-down resistors (2–10 kΩ).

7.5 PCI Reference Voltage—LV_{DD}

The MPC8241 PCI reference voltage (LV_{DD}) pins should be connected to 3.3 ± 0.3 V power supply if interfacing the MPC8241 into a 3.3-V PCI bus system. Similarly, the LV_{DD} pins should be connected to 5.0 V ± 5% power supply if interfacing the MPC8241 into a 5-V PCI bus system. For either reference voltage, the MPC8241 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8241 tolerates 5-V signals when interfaced into a 5-V PCI bus system. (See Errata No. 18 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*).

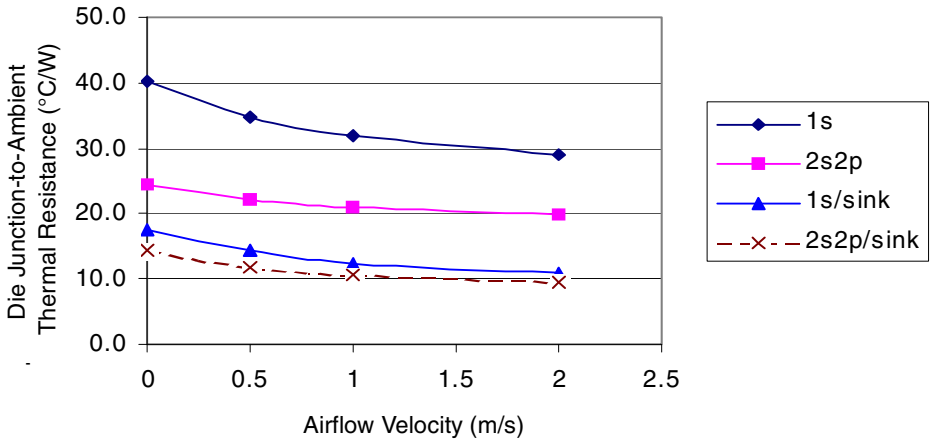


Figure 29. Die Junction-to-Ambient Resistance

The board designer can choose among several types of heat sinks to place on the MPC8241. Several commercially available heat sinks for the MPC8241 are provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

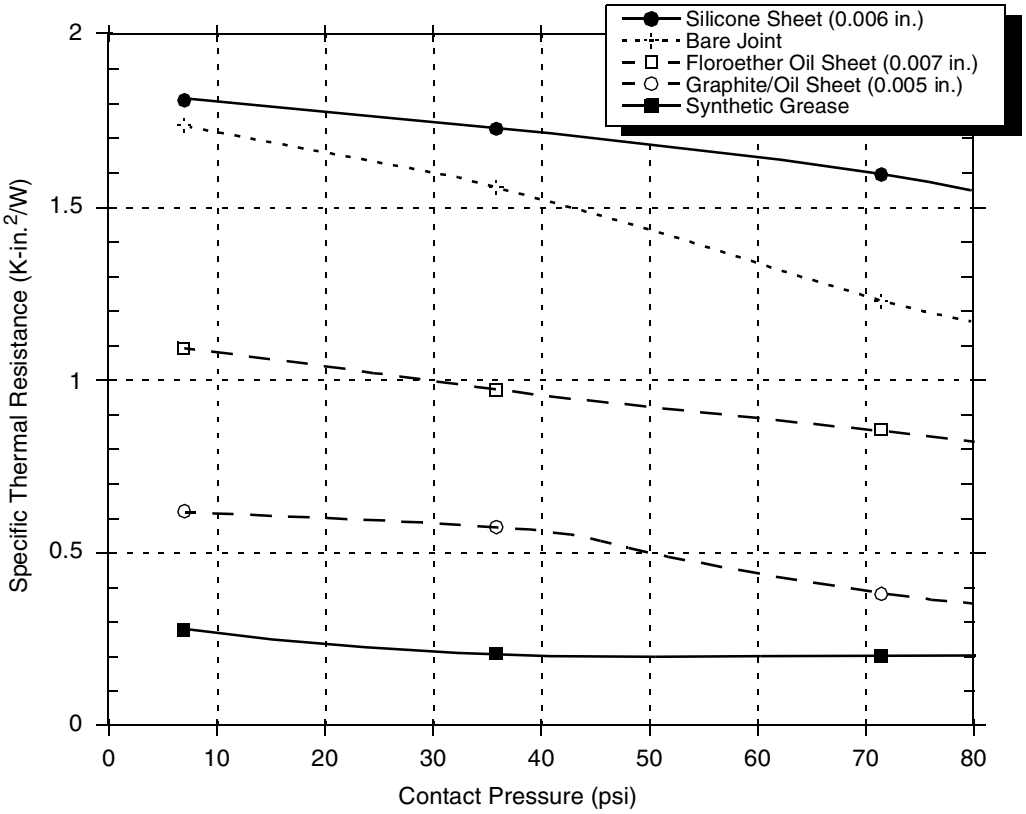


Figure 31. Thermal Performance of Select Thermal Interface Material

The board designer can choose among several types of thermal interface. Heat sink adhesive materials are selected on the basis of high conductivity and adequate mechanical strength to meet equipment shock/vibration requirements. Several commercially-available thermal interfaces and adhesive materials are provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481

where:

T_T = thermocouple temperature atop the package (°C)
ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance minimizes the change in thermal performance that is caused by removing part of the thermal interface to the heat sink. Considering the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

In many cases, it is appropriate to simulate the system environment using a computational fluid dynamics thermal simulation tool. In such a tool, the simplest thermal model of a package that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board.

7.8 References

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

8 Ordering Information

Ordering information for the parts that this document fully covers is provided in Section 8.1, “Part Numbers Fully Addressed by This Document.” Section 8.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

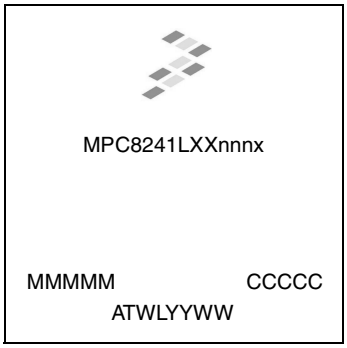
Table 20. Part Numbers Addressed by MPC8241TXXPNS Series (Document No. MPC8241ECSO1AD))

MPC	*nnnn*	T	*xx*	*nnn*	*x*	
MPC	8241	T = Extended temperature spec. –40° to 105°C	ZQ = thick substrate and thick mold cap PBGA (two layers)	166, 200 @ 1.8 V ± 100 mV	D:1.4 = Rev. ID:0x14	0x80811014

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by hardware specifications addendums may support other maximum core frequencies.

8.3 Part Marking

Parts are marked as the example shown in Figure 32.



Notes:
MMMMM is the 5-digit mask number.
ATWLYYWW is traceability code.
CCCCC is the country code.

Figure 32. Part Marking for MPC8241 Device

9 Document Revision History

Table 21 provides a revision history for this hardware specification.

Table 21. Revision History Table

Revision	Date	Substantive Change(s)
10	02/2009	In Table 16, “MPC8241 Pinout Listing,” added footnote 10 to PMAA[2]. In Table 16, “MPC8241 Pinout Listing,” removed footnote 12 for second listing of $\overline{\text{RCS3}}$/TRIG_OUT .
9	09/2007	Completely replaced Section 4.6 with compliant I^2C specifications as with other related integrated processor devices. Section 7.6, “JTAG Configuration Signals” Reworded paragraph beginning “The arrangement shown in Figure 27 .. .”

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