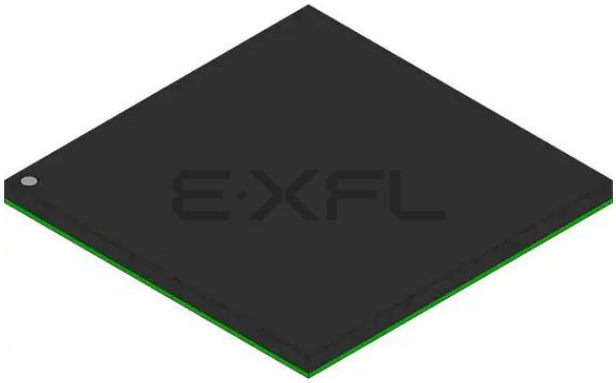

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8241lvr166d

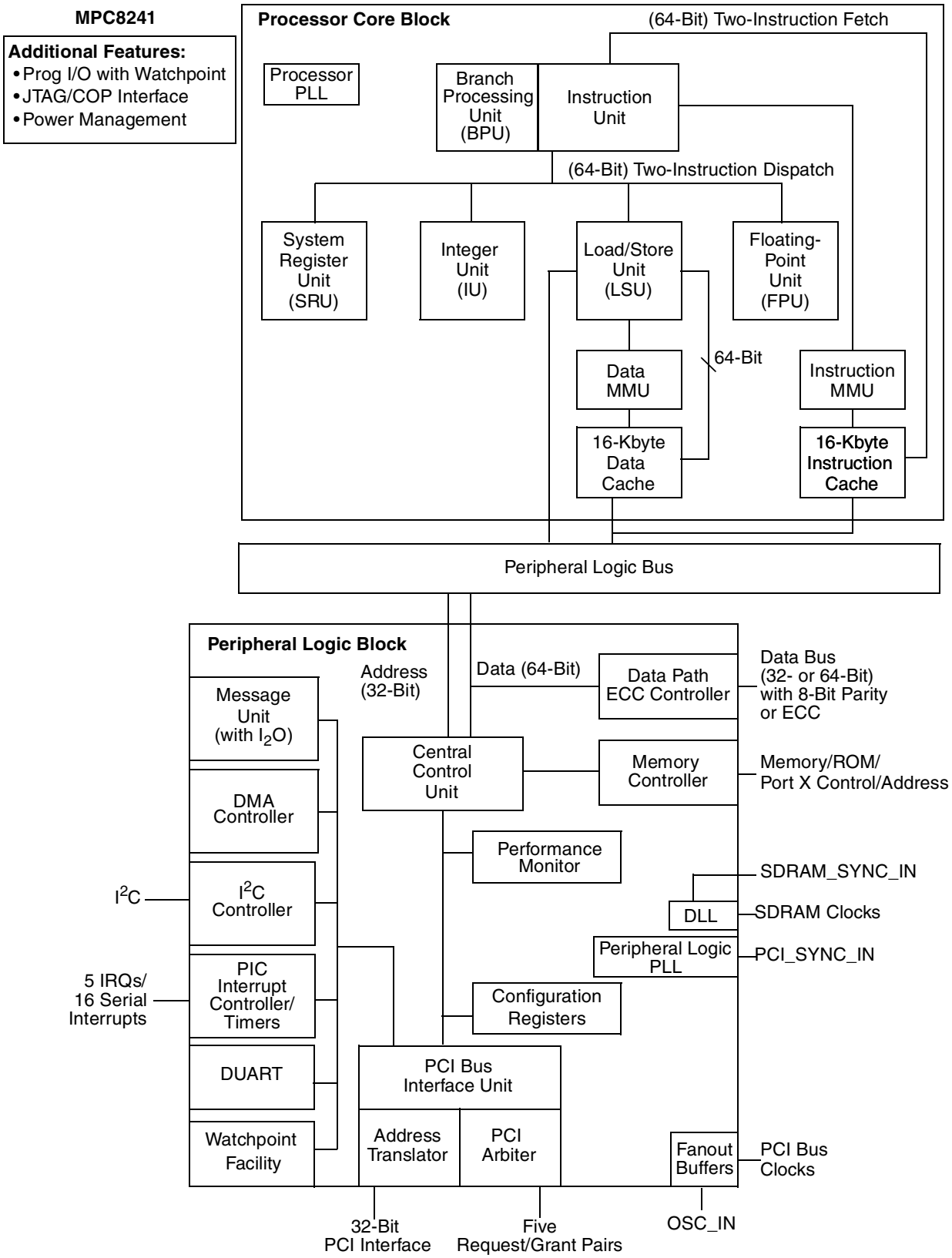


Figure 1. MPC8241 Block Diagram

  - I^2C controller with full master/slave support that accepts broadcast messages
  - Programmable interrupt controller (PIC)
    - Five hardware interrupts (IRQs) or 16 serial interrupts
    - Four programmable timers with cascade
  - Two (dual) universal asynchronous receiver/transmitters (UARTs)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI bus and memory interface output drivers
- System level performance monitor facility
- Debug features
  - Memory attribute and PCI attribute signals
  - Debug address signals
  - $\overline{\text{MIV}}$ signal—marks valid address and data bus cycles on the memory bus
  - Programmable input and output signals with watchpoint capability
  - Error injection/capture on data path
  - IEEE Std. 1149.1 (JTAG)/test interface

3 General Parameters

The following list summarizes the general parameters of the MPC8241:

Technology	0.25 µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully static
Packages	Surface-mount 357 (thick substrate and thick mold cap) plastic ball grid array (PBGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 2 for details and recommended operating conditions)
I/O power supply	3.0 to 3.6 V DC

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8241.

4.1 DC Electrical Characteristics

This section covers ratings, conditions, and other characteristics.

4.1.1 Absolute Maximum Ratings

This section describes the MPC8241 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	–0.3 to 2.1	V
Supply voltage—memory bus drivers, PCI and standard I/O buffers	$GV_{DD\_}OV_{DD}$	–0.3 to 3.6	V
Supply voltage—PLLs	$AV_{DD}/AV_{DD}2$	–0.3 to 2.1	V
Supply voltage—PCI reference	LV_{DD}	–0.3 to 5.4	V
Input voltage [2]	V_{in}	–0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105	•C
Storage temperature range	T_{stg}	–55 to 150	•C

Notes:
1. Table 2 provides functional and tested operating conditions. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8241.

Table 2. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply voltage		V_{DD}	1.8 ± 100 mV	V	2
I/O buffer supply for PCI and standard; supply voltages for memory bus drivers		$GV_{DD}\_OV_{DD}$	3.3 ± 0.3	V	2
CPU PLL supply voltage		AV_{DD}	1.8 ± 100 mV		2
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8 ± 100 mV	V	2
PCI reference		LV_{DD}	5.0 ± 5%	V	4, 5, 6
			3.3 ± 0.3	V	5, 6, 7
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	4, 7
	All other inputs		0 to 3.6	V	8
Die-junction temperature		T_j	0 to 105	•C	

Notes:

1. Freescale has tested these operating conditions and recommends them. Proper device operation outside of these conditions is not guaranteed.
2. **Caution:** $GV_{DD}\_OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 1.8 V at any time including during power-on reset. Note that $GV_{DD}\_OV_{DD}$ pins are all shorted together: This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. Connections should not be made to individual PWRRING pins.
3. **Caution:** $V_{DD}/AV_{DD}/AV_{DD}2$ must not exceed $GV_{DD}\_OV_{DD}$ by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 5.0 V DC power supply.
5. **Caution:** LV_{DD} must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** LV_{DD} must not exceed $GV_{DD}\_OV_{DD}$ by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3 V DC power supply.
8. **Caution:** Input voltage (V_{in}) must not be greater than the supply voltage ($V_{DD}/AV_{DD}/AV_{DD}2$) by more than 2.5 V at all times including during power-on reset. Input voltage (V_{in}) must not be greater than $GV_{DD}\_OV_{DD}$ by more than 0.6 V at all times including during power-on reset.

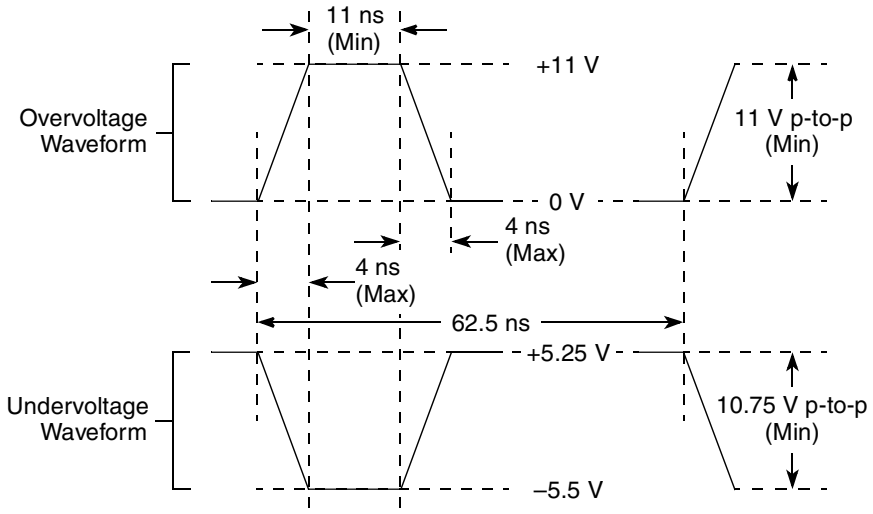


Figure 5. Maximum AC Waveforms for 5-V Signaling

4.2 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC8241 at recommended operating conditions.

Table 3. DC Electrical Specifications

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Input high voltage	PCI only, except PCI_SYNC_IN	V_{IH}	$0.65 \times GV_{DD}\_OV_{DD}$	LV_{DD}	V	1
Input low voltage	PCI only, except PCI_SYNC_IN	V_{IL}	—	$0.3 \times GV_{DD}\_OV_{DD}$	V	
Input high voltage	All other pins, including PCI_SYNC_IN ($GV_{DD}\_OV_{DD}$ = 3.3 V)	V_{IH}	2.0	3.3	V	
Input low voltage	All inputs, including PCI_SYNC_IN	V_{IL}	GND/GNDRING	0.8	V	2
Input leakage current for pins using DRV_PCI driver	$0.5\ V \le V_{in} \le 2.7$ V @ LV_{DD} = 4.75 V	I_L	—	±70	μA	3
Input leakage current all others	LV_{DD} = 3.6 V $GV_{DD}\_OV_{DD} \le 3.465$ V	I_L	—	±10	μA	3
Output high voltage	I_{OH} = driver dependent ($GV_{DD}\_OV_{DD}$ = 3.3 V)	V_{OH}	2.4	—	V	4
Output low voltage	I_{OL} = driver dependent ($GV_{DD}\_OV_{DD}$ = 3.3 V)	V_{OL}	—	0.4	V	4

Table 3. DC Electrical Specifications (continued)

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Capacitance	V_{in} = 0 V, f = 1 MHz	C_{in}	—	16.0	pF	

Notes:
1. See Table 16 for pins with internal pull-up resistors.
2. All grounded pins are connected together.
3. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} or both GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} must vary in the same direction.
4. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 16.

4.2.1 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 16. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8241 Output Pins [5, 6]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20 (default)	GV_{DD}_OV_{DD} = 3.3 V	36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)		89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) where table entry voltage = GV_{DD}_OV_{DD} – PCI V_{OH}.
2. For all others with GV_{DD}_ OV_{DD} = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = GV_{DD}_OV_{DD} – V_{OH}.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.
4. For all others with GV_{DD}_OV_{DD} = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4-V table entry.
5. See driver bit details for output driver control register (0x73) in the *MPC8245 Integrated Processor Reference Manual*.
6. See Chip Errata No. 19 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*.

Table 7 provides the operating frequency information for the MPC8241 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V.

Table 7. Operating Frequency

Characteristic	166 MHz		200 MHz		266 MHz		Unit
	$V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 ± 100 mV						
	Min	Max	Min	Max	Min	Max	
Processor frequency (CPU)	100	166	100	200	100	266	MHz
Memory bus frequency	33	83	33	100	33	133	MHz
PCI input frequency	25–66						MHz

Caution: The PCI_SYNC_IN frequency and PLL_CFG[0:4] settings must be chosen such that the resulting peripheral logic/memory bus frequency and CPU (core) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 6, "PLL Configuration," for valid PLL_CFG[0:4] settings and PCI_SYNC_IN frequencies.

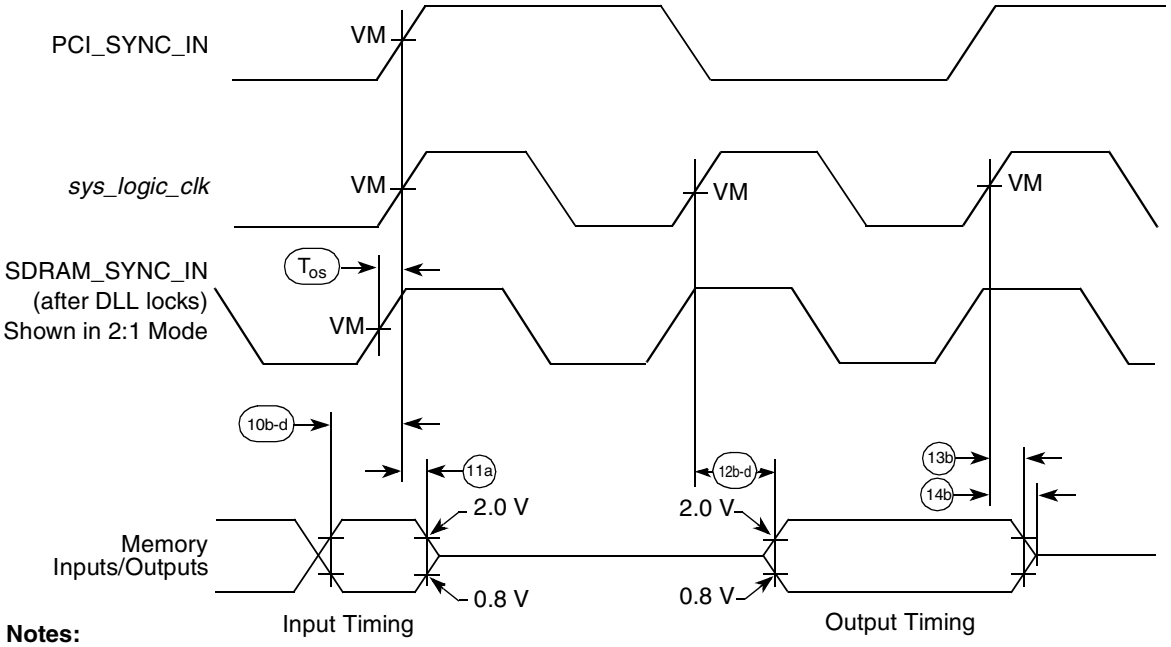
4.5.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications at recommended operating conditions, as defined in Section 4.5.2, "Input AC Timing Specifications." These specifications are for the default driver strengths indicated in Table 4. Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
1	Frequency of operation (PCI_SYNC_IN)	25	66	MHz	
2, 3	PCI_SYNC_IN rise and fall times	—	2.0	ns	1
4	PCI_SYNC_IN duty cycle measured at 1.4 V	40	60	%	
5a	PCI_SYNC_IN pulse width high measured at 1.4 V	6	9	ns	2
5b	PCI_SYNC_IN pulse width low measured at 1.4 V	6	9	ns	2
7	PCI_SYNC_IN jitter	—	200	ps	
8a	PCI_CLK[0:4] skew (pin-to-pin)	—	250	ps	
8b	SDRAM_CLK[0:3] skew (pin-to-pin)	—	190	ps	3
10	Internal PLL relock time	—	100	µs	2, 4, 5
15	DLL lock range with DLL_EXTEND = 0 (disabled) and normal tap delay; (default DLL mode)	See Figure 7		ns	6
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	



Notes:
VM = Midpoint voltage (1.4 V).
10b-d = Input signals valid timing.
11a = Input hold time of SDRAM_SYNC_IN to memory.
12b-d = *sys_logic_clk* to output valid timing.
13b = Output hold time for non-PCI signals.
14b = SDRAM-SYNC_IN to output high-impedance timing for non-PCI signals.
T_{os} = Offset timing required to align *sys_logic_clk* with SDRAM_SYNC_IN. The SDRAM_SYNC_IN signal is adjusted by the DLL to accommodate for internal delay. This causes SDRAM_SYNC_IN to appear before *sys_logic_clk* once the DLL locks.

Figure 11. Input/Output Timing Diagram Referenced to SDRAM_SYNC_IN

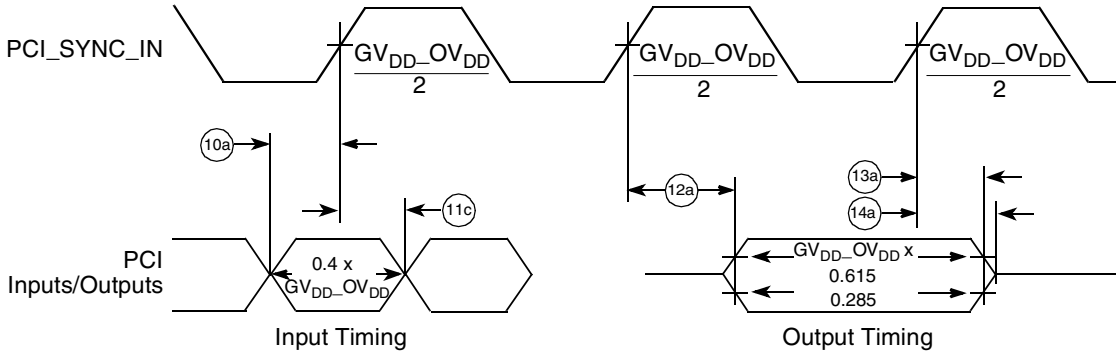


Figure 12. Input/Output Timing Diagram Referenced to PCI_SYNC_IN

Figure 13 shows the input timing diagram for mode select signals.

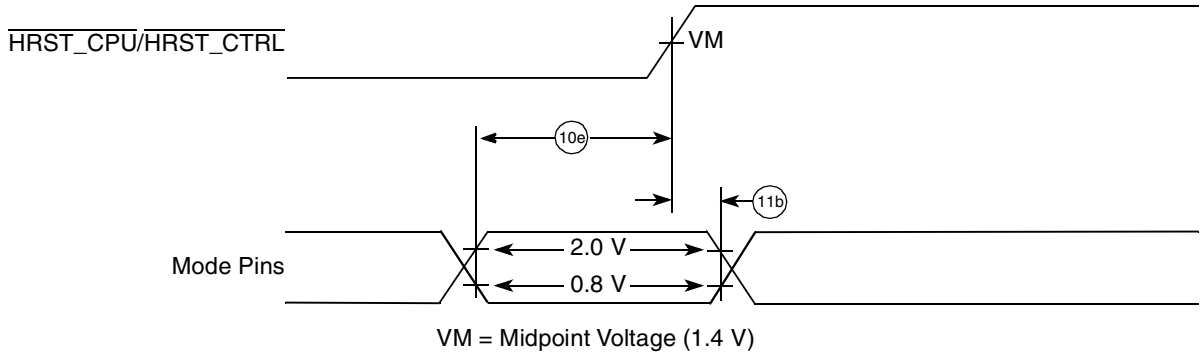


Figure 13. Input Timing Diagram for Mode Select Signals

4.5.3 Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V (see Figure 11). All output timings assume a purely resistive 50-Ω load (see Figure 14). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths that Table 4 indicates.

Table 11. Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, see Figure 15				
12a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{\text{MCP}}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{\text{MCP}}$,CKE] = 00	—	7.5		
12b	*sys_logic_clk* to output valid (memory address, control, and data signals)	—	4.5	ns	2
12c	*sys_logic_clk* to output valid (for all others)	—	7.0	ns	2
12d	*sys_logic_clk* to output valid (for I^2C)	—	5.0	ns	2
12e	*sys_logic_clk* to output valid (ROM/Flash/Port X)	—	6.0	ns	2
13a	Output hold (PCI), see Figure 15				
13a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{\text{MCP}}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{\text{MCP}}$,CKE] = 00	3.5	—		
13b	Output hold (all others)	1.0	—	ns	2
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	1, 3

Table 12. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8245 Integrated Processor Reference Manual* for information on the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if the OV_{DD} is switched off.

4.6.2 I^2C AC Electrical Specifications

Table 13 provides the AC timing parameters for the I^2C interfaces.

Table 13. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	µs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	µs
Data output delay time:	t_{I2OVKL}	—	0.9[3]	
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

Figure 17 shows the AC timing diagram for the I^2C bus.

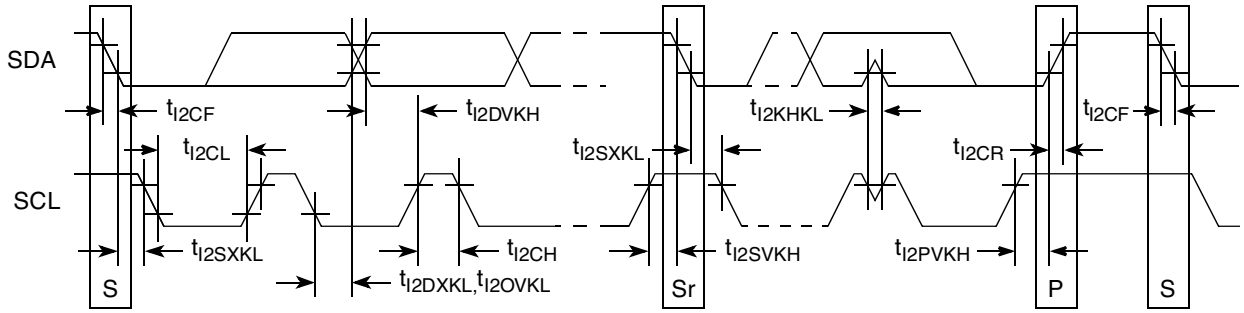


Figure 17. I^2C Bus AC Timing Diagram

4.7 PIC Serial Interrupt Mode AC Timing Specifications

Table 14 provides the PIC serial interrupt mode AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with GV_{DD}–OV_{DD} = 3.3 V ± 5% and LV_{DD} = 3.3 V ± 0.3 V.

Table 14. PIC Serial Interrupt Mode AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	S_CLK frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	1
2	S_CLK duty cycle	40	60	%	—
3	S_CLK output valid time	—	6	ns	—
4	Output hold time	0	—	ns	—
5	$\overline{\text{S\_FRAME}}$, S_RST output valid time	—	1 *sys_logic_clk* period + 6	ns	2
6	S_INT input setup time to S_CLK	1 *sys_logic_clk* period + 2	—	ns	2
7	S_INT inputs invalid (hold time) to S_CLK	—	0	ns	2

Notes:

1. See the *MPC8245 Integrated Processor Reference Manual* for a description of the PIC interrupt control register (ICR) and S_CLK frequency programming.
2. S_RST, $\overline{\text{S\_FRAME}}$, and S_INT shown in Figure 18 and Figure 19, depict timing relationships to *sys_logic_clk* and S_CLK and do not describe functional relationships between S_RST, $\overline{\text{S\_FRAME}}$, and S_INT. The *MPC8245 Integrated Processor Reference Manual* describes the functional relationships between these signals.
3. The *sys_logic_clk* waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; *sys_logic_clk* is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the *MPC8245 Integrated Processor Reference Manual* for a complete clocking description.

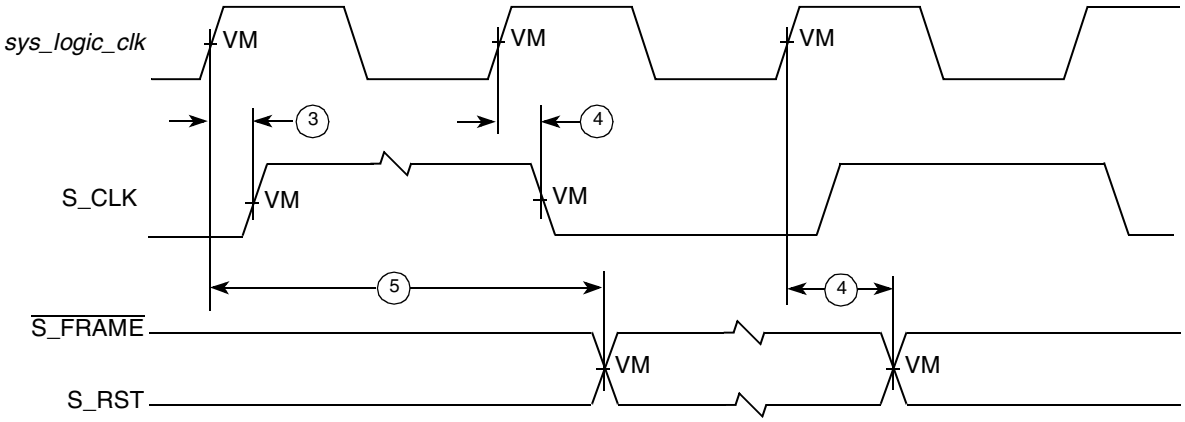


Figure 18. PIC Serial Interrupt Mode Output Timing Diagram

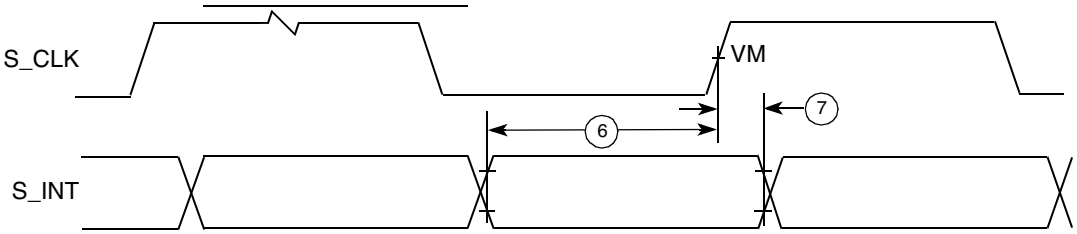


Figure 19. PIC Serial Interrupt Mode Input Timing Diagram

4.7.1 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 15 provides the JTAG AC timing specifications for the MPC8241 while in the JTAG operating mode at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	—
1	TCK cycle time	40	—	ns	—
2	TCK clock pulse width measured at 1.5 V	20	—	ns	—
3	TCK rise and fall times	0	3	ns	—
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$ assert time	10	—	ns	—
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	—

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
11	TMS, TDI data hold time	15	—	ns	—
12	TCK to TDO data valid	0	15	ns	—
13	TCK to TDO high impedance	0	15	ns	—

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
3. Nontest (other than TDO) signal output timing with respect to TCK.

Figure 20 through Figure 23 show the different timing diagrams for JTAG.

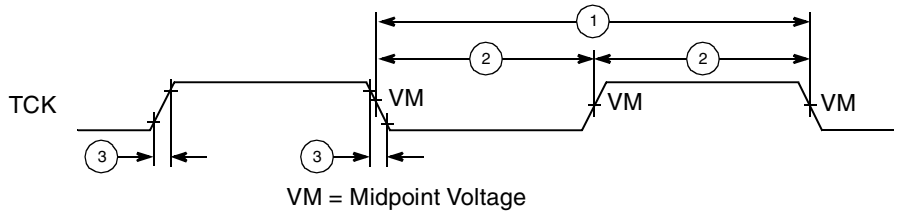


Figure 20. JTAG Clock Input Timing Diagram

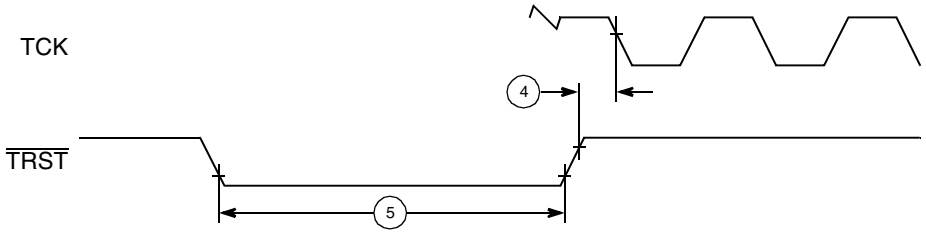


Figure 21. JTAG $\overline{\text{TRST}}$ Timing Diagram

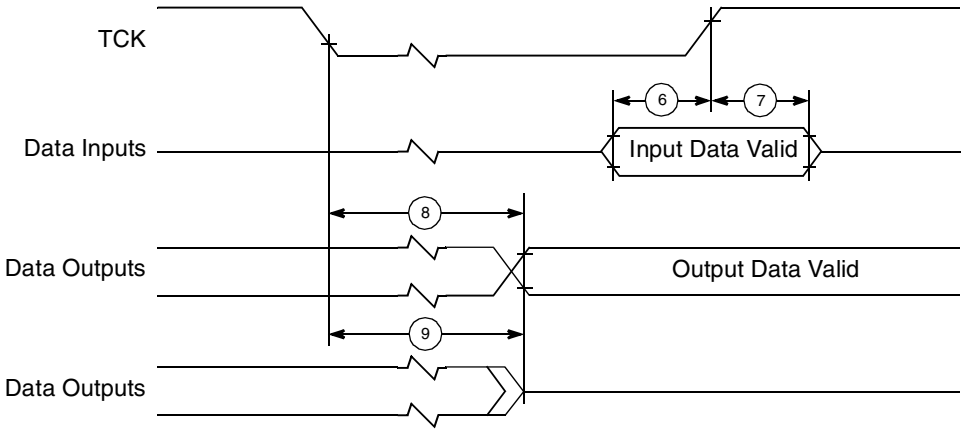


Figure 22. JTAG Boundary Scan Timing Diagram

Figure 25 shows the top surface, side profile, and pinout of the MPC8241, 357 PBGA ZQ and VR packages.

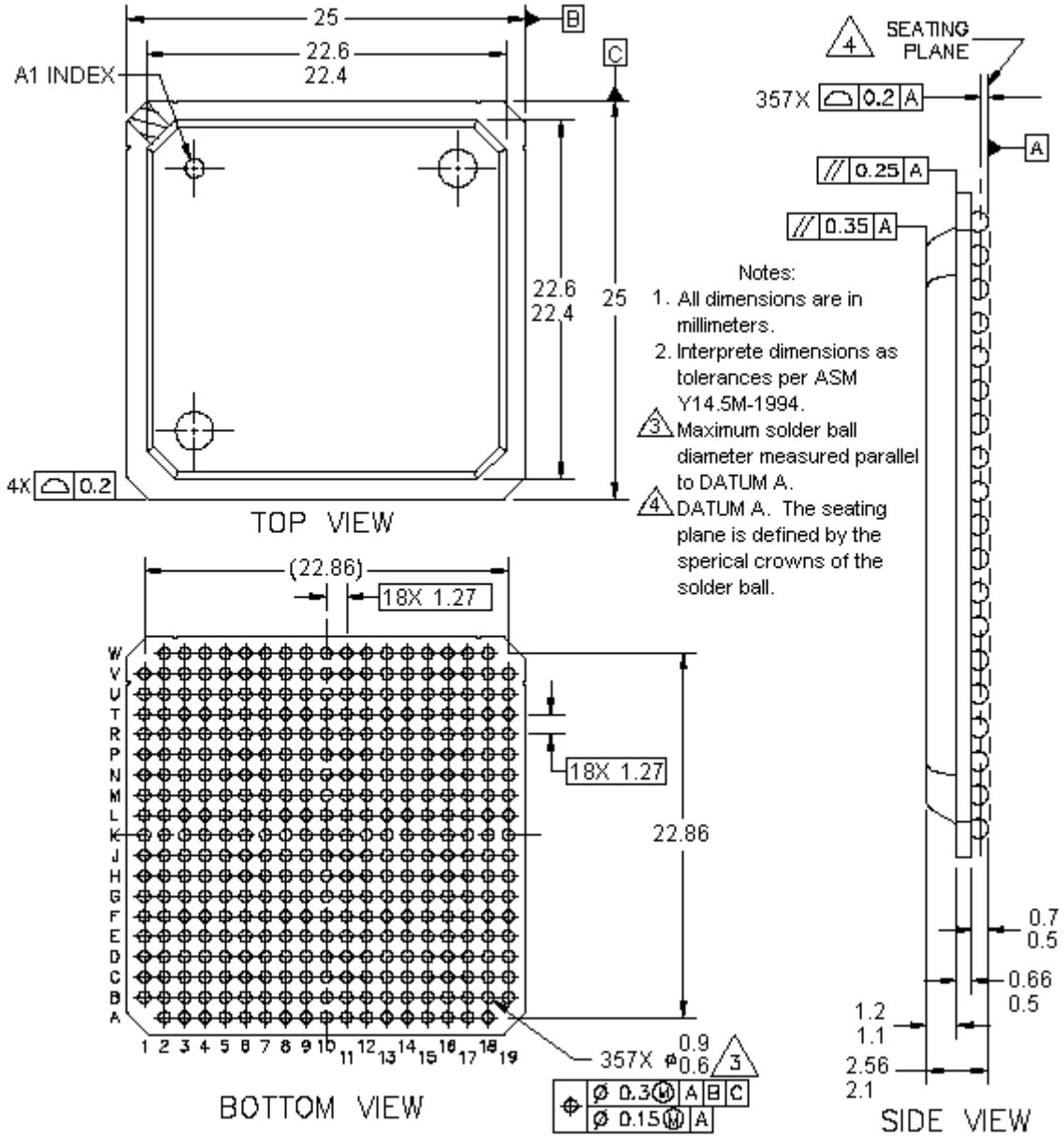


Figure 25. MPC8241 Package Dimensions and Pinout Assignments (ZQ and VR Packages)

5.3 Pinout Listings

Table 16 provides the pinout listing for the MPC8241, 357 PBGA package.

Table 16. MPC8241 Pinout Listing

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
$\overline{\text{C/BE}}$[3:0]	V11 V7 W3 R3	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 2
$\overline{\text{DEVSEL}}$	U6	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{FRAME}}$	T8	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{IRDY}}$	U7	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{LOCK}}$	V6	Input	$GV_{DD}\_OV_{DD}$	—	3
AD[31:0]	U13 V13 U11 W14 V14 U12 W10 T10 V10 U9 V9 W9 W8 T9 W7 V8 V4 W4 V3 V2 T5 R6 V1 T2 U3 P3 T4 R1 T3 R4 U2 U1	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 2
PAR	R7	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2
$\overline{\text{GNT}}$[3:0]	W15 U15 W17 V12	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 2
$\overline{\text{GNT4}}$/DA5	T11	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 4, 5
$\overline{\text{REQ}}$[3:0]	V16 U14 T15 V15	Input	$GV_{DD}\_OV_{DD}$	—	1, 6
$\overline{\text{REQ4}}$/DA4	W13	I/O	$GV_{DD}\_OV_{DD}$	—	5, 6
$\overline{\text{PERR}}$	T7	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3, 7
$\overline{\text{SERR}}$	U5	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3, 8
$\overline{\text{STOP}}$	W5	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{TRDY}}$	W6	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{INTA}}$	T12	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 8
IDSEL	U10	Input	$GV_{DD}\_OV_{DD}$	—	—
Memory Interface Signals					
MDL[0:31]	M19 M17 L16 L17 K18 J18 K17 K16 J15 J17 H18 F16 H16 H15 G17 D19 B3 C4 C2 D3 G5 E1 H5 E2 F1 F2 G2 J5 H1 H4 J4 J1	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1, 9
MDH[0:31]	M18 L18 L15 K19 K15 J19 J16 H17 G19 G18 G16 D18 F18 E18 G15 E15 C3 D4 E5 F5 D1 E4 D2 E3 F4 G3 G4 G1 H2 J3 J2 K5	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1
DQM[0:7]	A18 B18 A6 C7 D15 D14 A9 B8	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1
$\overline{\text{CS}}$[0:7]	A17 B17 C16 C17 C9 C8 A10 B10	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1
FOE	A7	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{\text{RCS0}}$	C10	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
$\overline{\text{RCS1}}$	B9	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
$\overline{\text{RCS2}}$/TRIG_IN	P18	I/O	$GV_{DD}\_OV_{DD}$	—	5, 12
$\overline{\text{RCS3}}$/TRIG_OUT	N18	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	5
SDMA[1:0]	A15 B15	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1, 10, 11
SDMA[11:2]	A11 B12 A12 C12 B13 C13 D12 A14 C14 B14	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1
$\overline{\text{DRDY}}$	P1	Input	$GV_{DD}\_OV_{DD}$	—	12, 13
SDMA12/$\overline{\text{SRESET}}$	L3	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA13/TBEN	K3	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA14/$\overline{\text{CHKSTOP\_IN}}$	K2	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDBA1	C11	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
SDBA0	B11	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
PAR[0:7]	E19 C19 D5 D6 E16 F17 B2 C1	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1
$\overline{\text{SDRAS}}$	B19	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10
$\overline{\text{SDCAS}}$	D16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10
CKE	C6	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{\text{WE}}$	B16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
$\overline{\text{AS}}$	A16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
PIC Control Signals					
IRQ0/S_INT	P4	Input	$GV_{DD}\_OV_{DD}$	—	—
IRQ1/S_CLK	R2	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
IRQ2/S_RST	U19	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
IRQ3/$\overline{\text{S\_FRAME}}$	P15	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
IRQ4/$\overline{\text{L\_INT}}$	P2	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
I^2C Control Signals					
SDA	P17	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	8, 12
SCL	R19	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	8, 12
DUART Control Signals					
SOUT1/PCI_CLK0	T16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14
SIN1/PCI_CLK1	U16	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14, 24
SOUT2/$\overline{\text{RTS1}}$/PCI_CLK2	W18	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14
SIN2/$\overline{\text{CTS1}}$/PCI_CLK3	V19	I	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14, 24
Clock-Out Signals					
PCI_CLK0/SOUT1	T16	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI_CLK	5, 14

Table 18. PLL Configurations (266-MHz Parts) (continued)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Off	Off

Notes:

1. Limited by maximum PCI input frequency (66 MHz).
2. Note the impact of the relevant revisions for modes 7 and 1E.
3. Limited by minimum memory VCO frequency (132 MHz).
4. Limited due to maximum memory VCO frequency (352 MHz).
5. Limited by maximum CPU operating frequency.
6. Limited by minimum CPU VCO frequency (300 MHz).
7. Limited by maximum CPU VCO frequency (704 MHz).
8. In clock off mode, no clocking occurs inside the MPC8241, regardless of the PCI_SYNC_IN input.
9. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
10. PLL_CFG[0:4] settings that are not listed are reserved.
11. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
12. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
13. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
14. Limited by minimum CPU operating frequency (100 MHz).
15. Limited by minimum memory bus frequency (50 MHz).

7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8241.

7.1 PLL Power Supply Filtering

The AV_{DD} and $AV_{DD}2$ power signals on the MPC8241 provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and $AV_{DD}2$ input signals should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 26 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD} and $AV_{DD}2$ power signal pins. In *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), Dr. Howard Johnson recommends using multiple small capacitors of equal value instead of multiple values.

Place the circuits as closely as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing from the capacitors to the input signal pins should be as direct as possible with minimal inductance of vias.

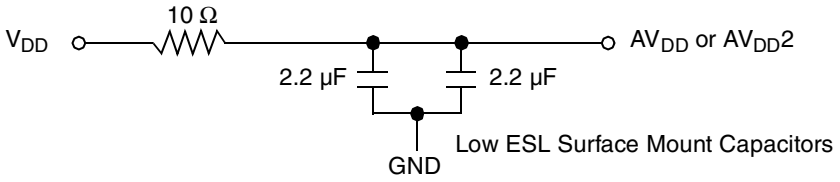


Figure 26. PLL Power Supply Filter Circuit

7.2 Decoupling Recommendations

Dynamic power management, large address and data buses, and high operating frequencies enable the MPC8241 to generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8241 system, and the MPC8241 itself requires a clean, tightly regulated source of power. Therefore, place at least one decoupling capacitor at each V_{DD}, GV_{DD}_OV_{DD}, and LV_{DD} pin. These decoupling capacitors receive their power from dedicated power planes in the PCB, using short traces to minimize inductance. These capacitors should have a value of 0.1 µF. To minimize lead inductance, use only ceramic SMT (surface mount technology) capacitors, preferably 0508 or 0603, on which connections are made along the length of the part.

In addition, distribute several bulk storage capacitors around the PCB to feed the V_{DD}, GV_{DD}_OV_{DD}, and LV_{DD} planes and enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the necessary quick response time, and should be connected to the power and ground planes through two vias to minimize inductance. Freescale recommends using bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

7.3 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Tie unused active-low inputs to OV_{DD}. Connect unused active-high inputs to GND. All no connect (NC) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}_OV_{DD}, LV_{DD}, and GND pins.

The PCI_SYNC_OUT signal is to be routed halfway out to the PCI devices and then returned to the PCI_SYNC_IN input.

The SDRAM_SYNC_OUT signal is to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the MPC8241. The trace length can be used to skew or adjust the timing window as needed. See the Tundra *Tsi107™ Design Guide* (AN1849) and Freescale application notes AN2164/D, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1* and AN2746, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part* 2 for more details. Note the SDRAM_SYNC_IN to PCI_SYNC_IN time requirement (see Table 10).

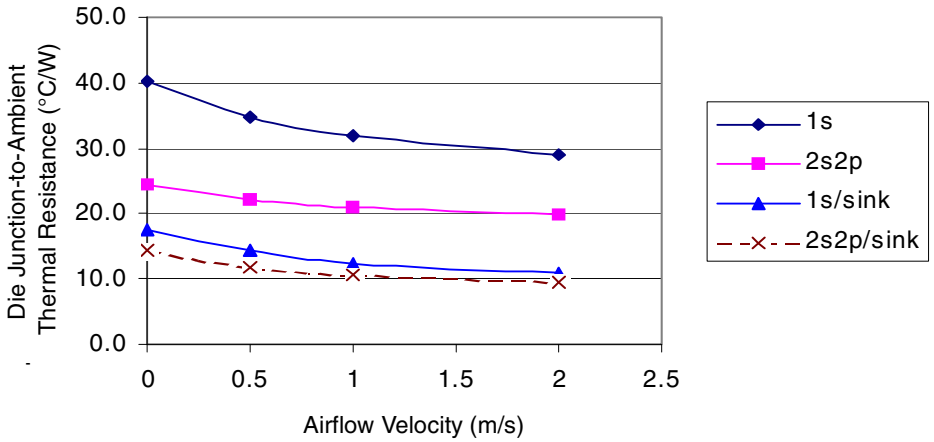


Figure 29. Die Junction-to-Ambient Resistance

The board designer can choose among several types of heat sinks to place on the MPC8241. Several commercially available heat sinks for the MPC8241 are provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

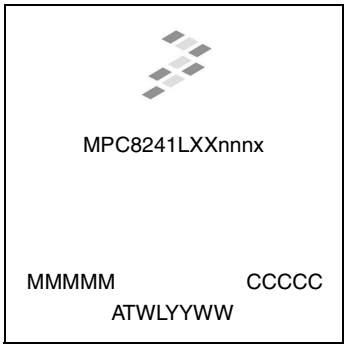
Table 20. Part Numbers Addressed by MPC8241TXXPNS Series (Document No. MPC8241ECSO1AD))

MPC	*nnnn*	T	*xx*	*nnn*	*x*	
MPC	8241	T = Extended temperature spec. –40° to 105°C	ZQ = thick substrate and thick mold cap PBGA (two layers)	166, 200 @ 1.8 V ± 100 mV	D:1.4 = Rev. ID:0x14	0x80811014

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by hardware specifications addendums may support other maximum core frequencies.

8.3 Part Marking

Parts are marked as the example shown in Figure 32.



Notes:
MMMMM is the 5-digit mask number.
ATWLYYWW is traceability code.
CCCCC is the country code.

Figure 32. Part Marking for MPC8241 Device

9 Document Revision History

Table 21 provides a revision history for this hardware specification.

Table 21. Revision History Table

Revision	Date	Substantive Change(s)
10	02/2009	In Table 16, “MPC8241 Pinout Listing,” added footnote 10 to PMAA[2]. In Table 16, “MPC8241 Pinout Listing,” removed footnote 12 for second listing of $\overline{\text{RCS3}}$/TRIG_OUT .
9	09/2007	Completely replaced Section 4.6 with compliant I^2C specifications as with other related integrated processor devices. Section 7.6, “JTAG Configuration Signals” Reworded paragraph beginning “The arrangement shown in Figure 27 .. .”