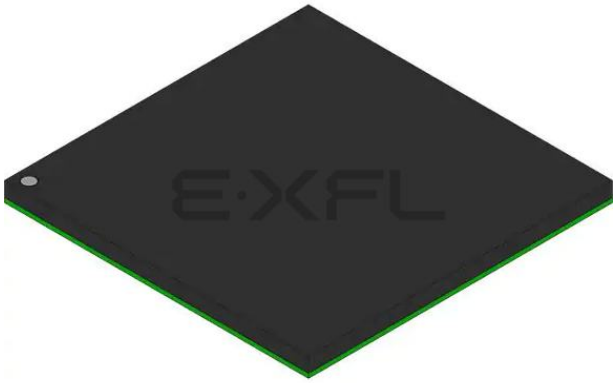

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8241lvr200d

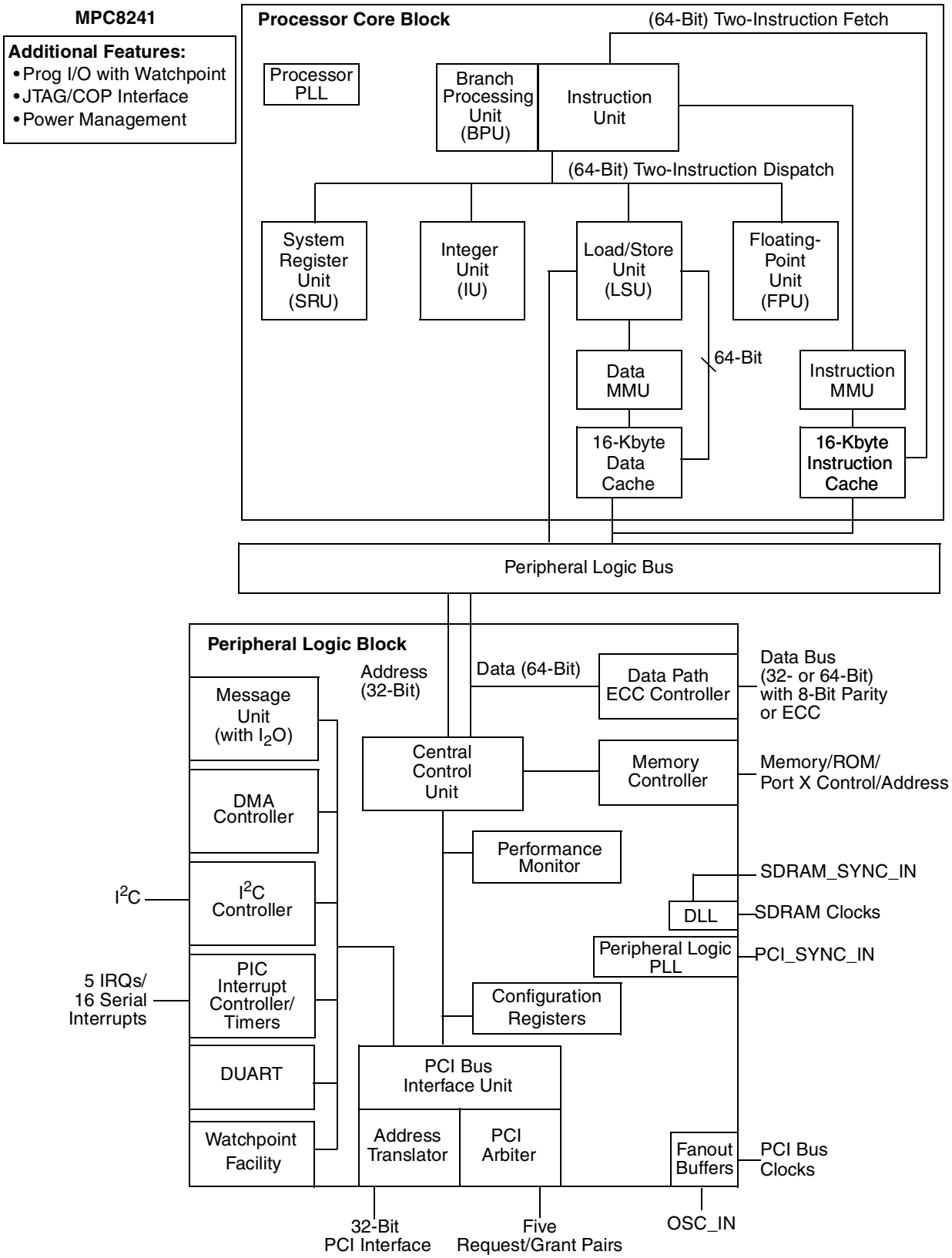


Figure 1. MPC8241 Block Diagram

  - I^2C controller with full master/slave support that accepts broadcast messages
  - Programmable interrupt controller (PIC)
    - Five hardware interrupts (IRQs) or 16 serial interrupts
    - Four programmable timers with cascade
  - Two (dual) universal asynchronous receiver/transmitters (UARTs)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI bus and memory interface output drivers
- System level performance monitor facility
- Debug features
  - Memory attribute and PCI attribute signals
  - Debug address signals
  - $\overline{\text{MIV}}$ signal—marks valid address and data bus cycles on the memory bus
  - Programmable input and output signals with watchpoint capability
  - Error injection/capture on data path
  - IEEE Std. 1149.1 (JTAG)/test interface

3 General Parameters

The following list summarizes the general parameters of the MPC8241:

Technology	0.25 µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully static
Packages	Surface-mount 357 (thick substrate and thick mold cap) plastic ball grid array (PBGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 2 for details and recommended operating conditions)
I/O power supply	3.0 to 3.6 V DC

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8241.

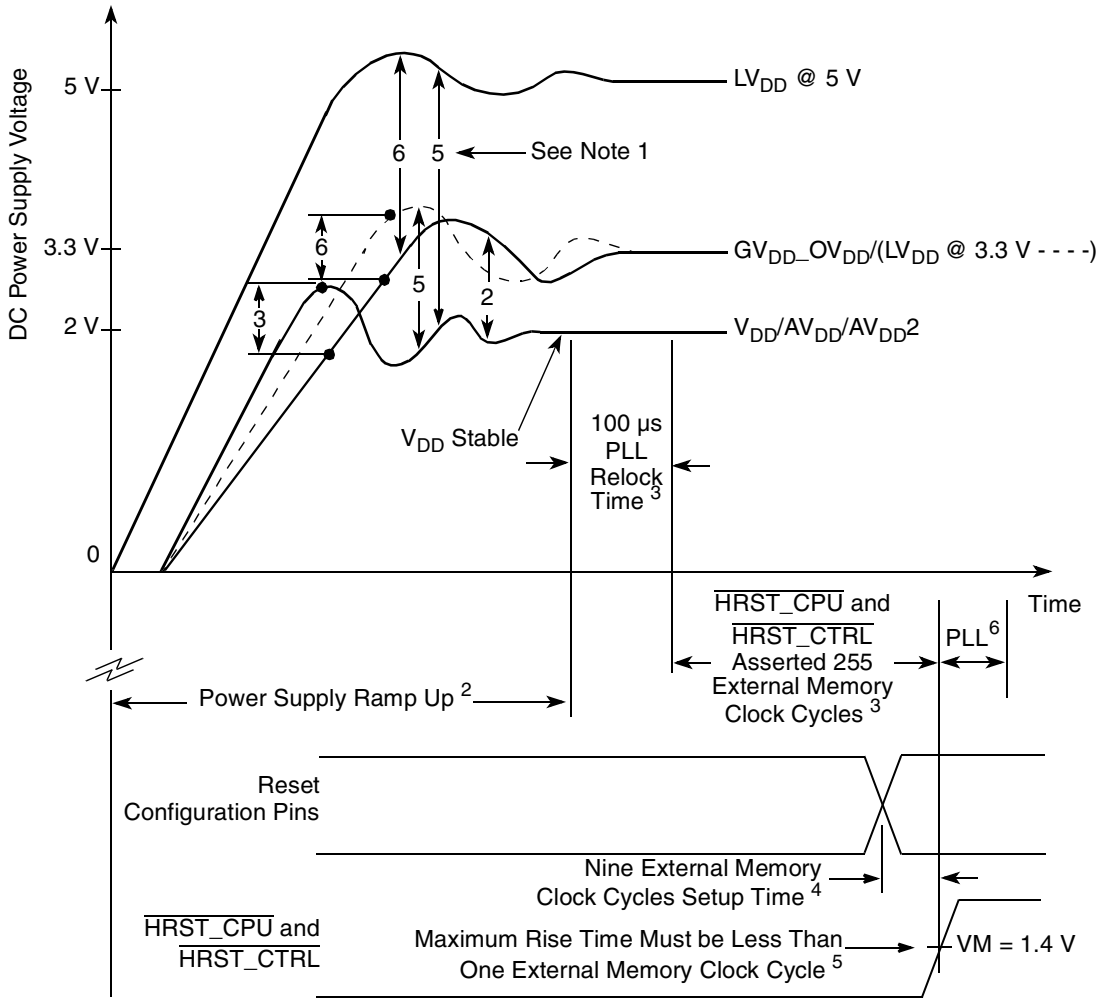
Table 2. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply voltage		V_{DD}	1.8 ± 100 mV	V	2
I/O buffer supply for PCI and standard; supply voltages for memory bus drivers		$GV_{DD}\_OV_{DD}$	3.3 ± 0.3	V	2
CPU PLL supply voltage		AV_{DD}	1.8 ± 100 mV		2
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8 ± 100 mV	V	2
PCI reference		LV_{DD}	5.0 ± 5%	V	4, 5, 6
			3.3 ± 0.3	V	5, 6, 7
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	4, 7
	All other inputs		0 to 3.6	V	8
Die-junction temperature		T_j	0 to 105	•C	

Notes:

1. Freescale has tested these operating conditions and recommends them. Proper device operation outside of these conditions is not guaranteed.
2. **Caution:** $GV_{DD}\_OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 1.8 V at any time including during power-on reset. Note that $GV_{DD}\_OV_{DD}$ pins are all shorted together: This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. Connections should not be made to individual PWRRING pins.
3. **Caution:** $V_{DD}/AV_{DD}/AV_{DD}2$ must not exceed $GV_{DD}\_OV_{DD}$ by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 5.0 V DC power supply.
5. **Caution:** LV_{DD} must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** LV_{DD} must not exceed $GV_{DD}\_OV_{DD}$ by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3 V DC power supply.
8. **Caution:** Input voltage (V_{in}) must not be greater than the supply voltage ($V_{DD}/AV_{DD}/AV_{DD}2$) by more than 2.5 V at all times including during power-on reset. Input voltage (V_{in}) must not be greater than $GV_{DD}\_OV_{DD}$ by more than 0.6 V at all times including during power-on reset.

Figure 2 shows supply voltage sequencing and separation cautions.



Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. See the Cautions section of Table 2 for details on this topic.
3. Refer to Table 8 for details on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for details on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.
6. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ negate in order to be latched.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Table 3. DC Electrical Specifications (continued)

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Capacitance	V_{in} = 0 V, f = 1 MHz	C_{in}	—	16.0	pF	

Notes:
1. See Table 16 for pins with internal pull-up resistors.
2. All grounded pins are connected together.
3. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} or both GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} must vary in the same direction.
4. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 16.

4.2.1 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 16. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8241 Output Pins [5, 6]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20 (default)	GV_{DD}_OV_{DD} = 3.3 V	36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)		89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) where table entry voltage = GV_{DD}_OV_{DD} – PCI V_{OH}.
2. For all others with GV_{DD}_ OV_{DD} = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = GV_{DD}_OV_{DD} – V_{OH}.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.
4. For all others with GV_{DD}_OV_{DD} = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4-V table entry.
5. See driver bit details for output driver control register (0x73) in the *MPC8245 Integrated Processor Reference Manual*.
6. See Chip Errata No. 19 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*.

4.3 Power Characteristics

Table 5 provides preliminary estimated power consumption data for the MPC8241.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)							Unit	Notes
	33/66/133	33/66/166	33/66/200	33/100/200	66/100/200	66/66/ 266	66/133/ 266		
Typical	0.7	0.8	1.0	1.0	1.0	1.5	1.8	W	1, 5
Max—CFP	0.8	1.0	1.2	1.3	1.3	1.9	2.1	W	1, 2
Max—INT	0.8	0.9	1.0	1.2	1.2	1.6	1.8	W	1, 3
Doze	0.5	0.6	0.7	0.8	0.8	1.0	1.3	W	1, 4, 6
Nap	0.2	0.2	0.3	0.4	0.4	0.4	0.7	W	1, 4, 6
Sleep	0.2	0.2	0.2	0.2	0.3	0.2	0.4	W	1, 4, 6
I/O Power Supplies [7]									
Mode	**Minimum**				**Maximum**			**Unit**	**Notes**
GV_{DD}_OV_{DD}	500				1130			mW	8

Notes:

1. The values include V_{DD}, AV_{DD}, and $AV_{DD}2$ but do not include I/O supply power.
2. Maximum—FP power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.
3. Maximum—INT power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at V_{DD} = 1.9 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at V_{DD} = AV_{DD} = 1.8 V, GV_{DD}_OV_{DD} = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. Power consumption of PLL supply pins (AV_{DD} and $AV_{DD}2$) < 15 mW, guaranteed by design, but not tested.
8. The typical maximum GV_{DD}_OV_{DD} value resulted from the MPC8241 operating at the fastest frequency combination of 66:133:266 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory and on 64-bit boundaries to local memory.

4.4 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8241. For details, see Section 7.7, "Thermal Management."

Table 6. Thermal Characterization Data

Rating	Thermal Test Board Description	Symbol	Value [7] (166- and 200-MHz Parts)	Value [7] (266-MHz Part)	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	38	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JMA}$	25	20	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	31	22	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	22	17	°C/W	1, 3
Junction-to-board (bottom)	Four-layer board (2s2p)	$R_{\theta JB}$	17	11	°C/W	4
Junction-to-case (top)	Single-layer board (1s)	$R_{\theta JC}$	8	7	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	2	2	°C/W	6

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the board horizontal.
3. Per EIA/JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per EIA/JESD51-2.
7. Note that the 166- and 200-MHz parts are in a two-layer package and the 266-MHz part is in a four-layer package, which causes the two package types to have different thermal characterization data.

4.5 AC Electrical Characteristics

After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 8, "Ordering Information."

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 through 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines,* for details on MPC8241 memory clock design.
7. Rise and fall times for the OSC_IN input are guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram, and Figure 7 through Figure 10 show the DLL locking range loop delay versus frequency of operation.

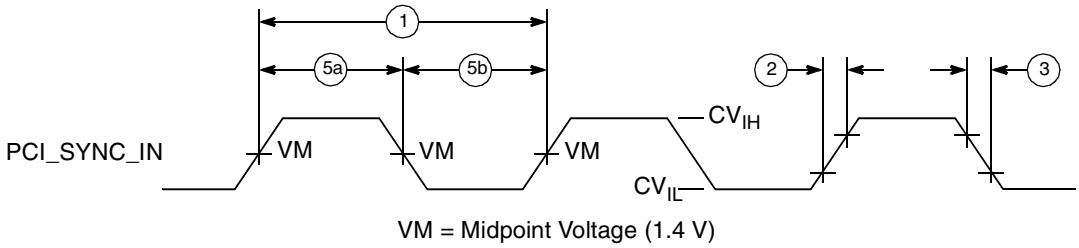


Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Register settings that define each DLL mode are shown in Table 9.

Table 9. DLL Mode Definition

DLL Mode	Bit 2 of Configuration Register at 0x76	Bit 7 of Configuration Register at 0x72
Normal tap delay, No DLL extend	0	0
Normal tap delay, DLL extend	0	1
Max tap delay, No DLL extend	1	0
Max tap delay, DLL extend	1	1

The DLL_MAX_DELAY bit can lengthen the amount of time through the delay line by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock is within the DLL lock range, there may be slightly more jitter in the output clock of the DLL if the phase comparator shifts the clock between adjacent tap points. Refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1*, for details on DLL modes and memory design.

The value of the current tap point after the DLL locks can be determined by reading bits 6–0 (DLL_TAP_COUNT) of the DLL tap count register (DTCR, located at offset 0xE3). These bits store the value (binary 0 through 127) of the current tap point and can indicate whether the DLL advances or decrements as it maintains the DLL lock. Therefore, for evaluation purposes, DTCR can be read for all DLL modes that support the T_{loop} value used for the trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN. The DLL mode with the smallest tap point value in the DTCR should be used because the bigger the tap point value, the more jitter that can be expected for clock signals. Keeping a DLL mode locked below tap point decimal 12 is not recommended.

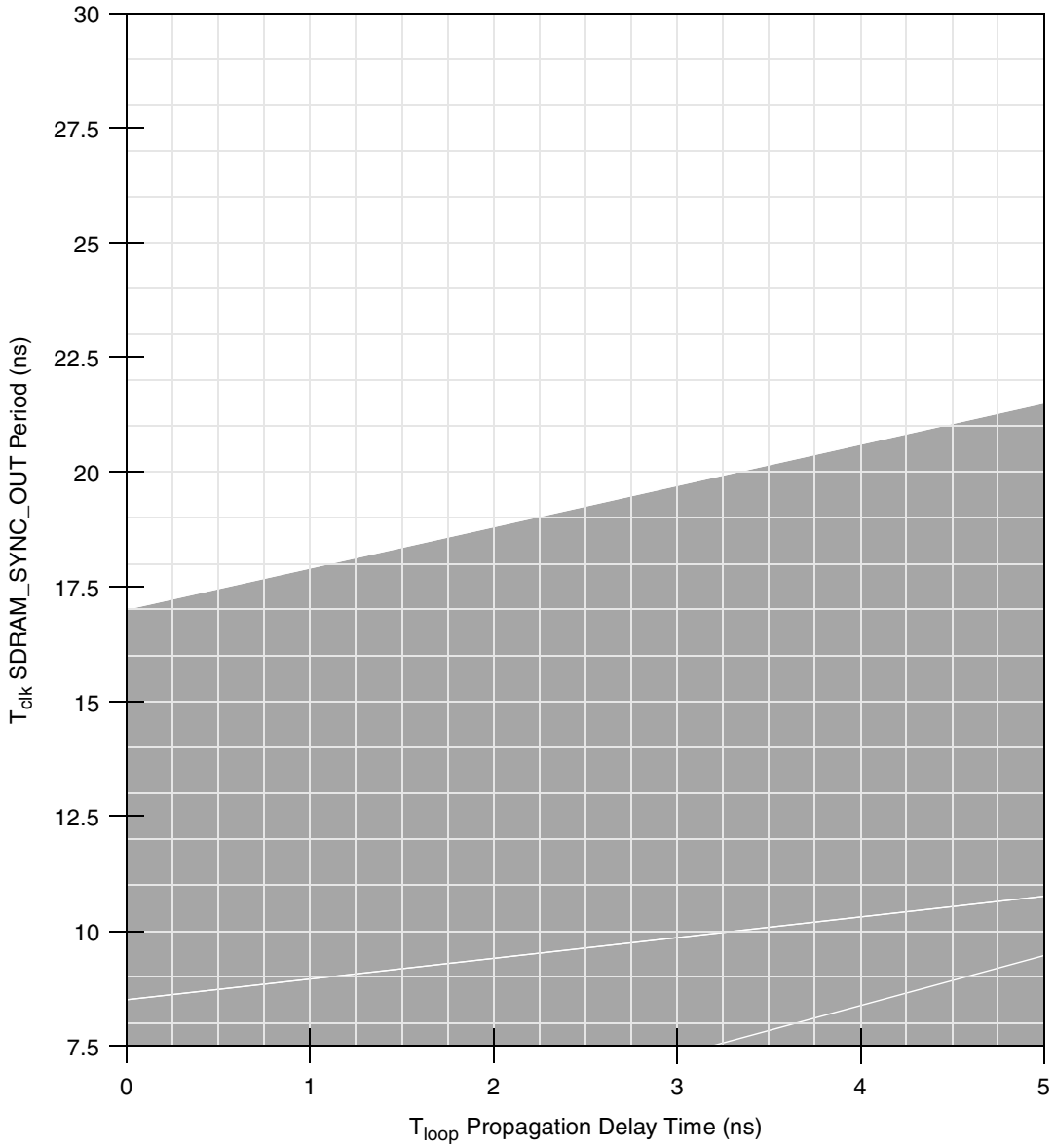
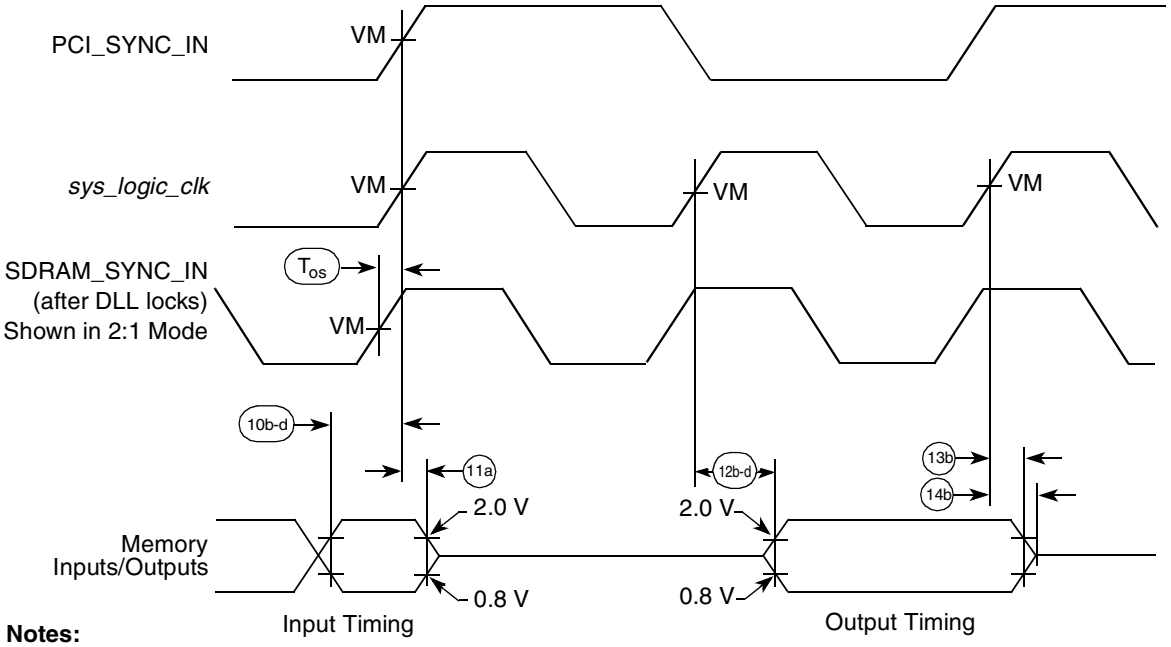


Figure 9. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=0 and Max Tap Delay



Notes:
VM = Midpoint voltage (1.4 V).
10b-d = Input signals valid timing.
11a = Input hold time of SDRAM_SYNC_IN to memory.
12b-d = *sys_logic_clk* to output valid timing.
13b = Output hold time for non-PCI signals.
14b = SDRAM-SYNC_IN to output high-impedance timing for non-PCI signals.
T_{os} = Offset timing required to align *sys_logic_clk* with SDRAM_SYNC_IN. The SDRAM_SYNC_IN signal is adjusted by the DLL to accommodate for internal delay. This causes SDRAM_SYNC_IN to appear before *sys_logic_clk* once the DLL locks.

Figure 11. Input/Output Timing Diagram Referenced to SDRAM_SYNC_IN

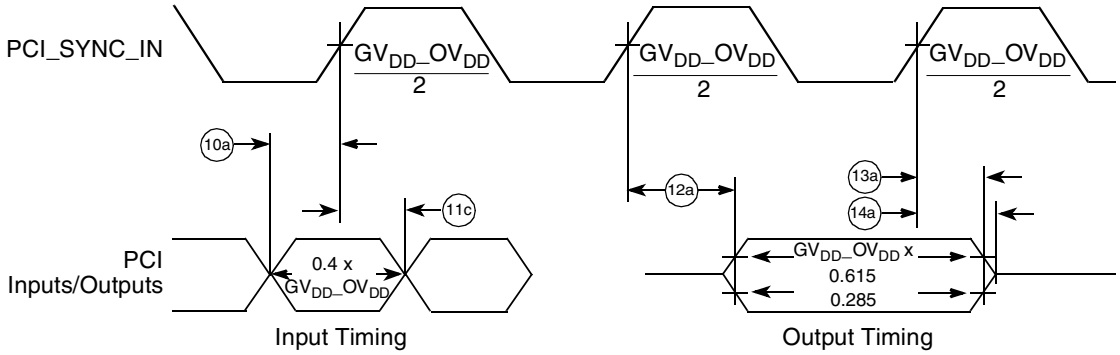


Figure 12. Input/Output Timing Diagram Referenced to PCI_SYNC_IN

Table 11. Output AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
14b	*sys_logic_clk* to output high impedance (for all others)	—	4.0	ns	2

Notes:

1. All PCI signals are measured from $GV_{DD}\_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times GV_{DD}\_OV_{DD}$ or $0.615 \times GV_{DD}\_OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 12.
2. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk* to the TTL level (0.8 or 2.0 V) of the signal in question. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. PCI bused signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[3:0], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[31:0], $\overline{\text{REQ}}$[4:0], $\overline{\text{GNT}}$[4:0], $\overline{\text{IDSEL}}$, and $\overline{\text{INTA}}$.
4. To meet minimum output hold specifications relative to PCI_SYNC_IN for both 33- and 66-MHz PCI systems, the MPC8241 has a programmable output hold delay for PCI signals (the PCI_SYNC_IN to output valid timing is also affected). The initial value of the output hold delay is determined by the values on the $\overline{\text{MCP}}$ and CKE reset configuration signals; the values on these two signals are inverted and subsequently stored as the initial settings of PCI_HOLD_DEL = PMCR2[5, 4] (power management configuration register 2 <0x72>), respectively. Because $\overline{\text{MCP}}$ and CKE have internal pull-up resistors, the default value of PCI_HOLD_DEL after reset is 0b00. Additional output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register. See Figure 15 for PCI_HOLD_DEL effect on output valid and hold time.

Figure 14 provides the AC test load for the MPC8241.

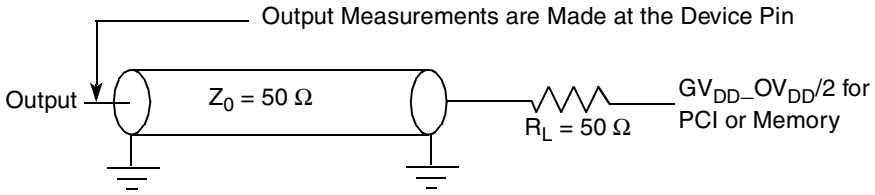
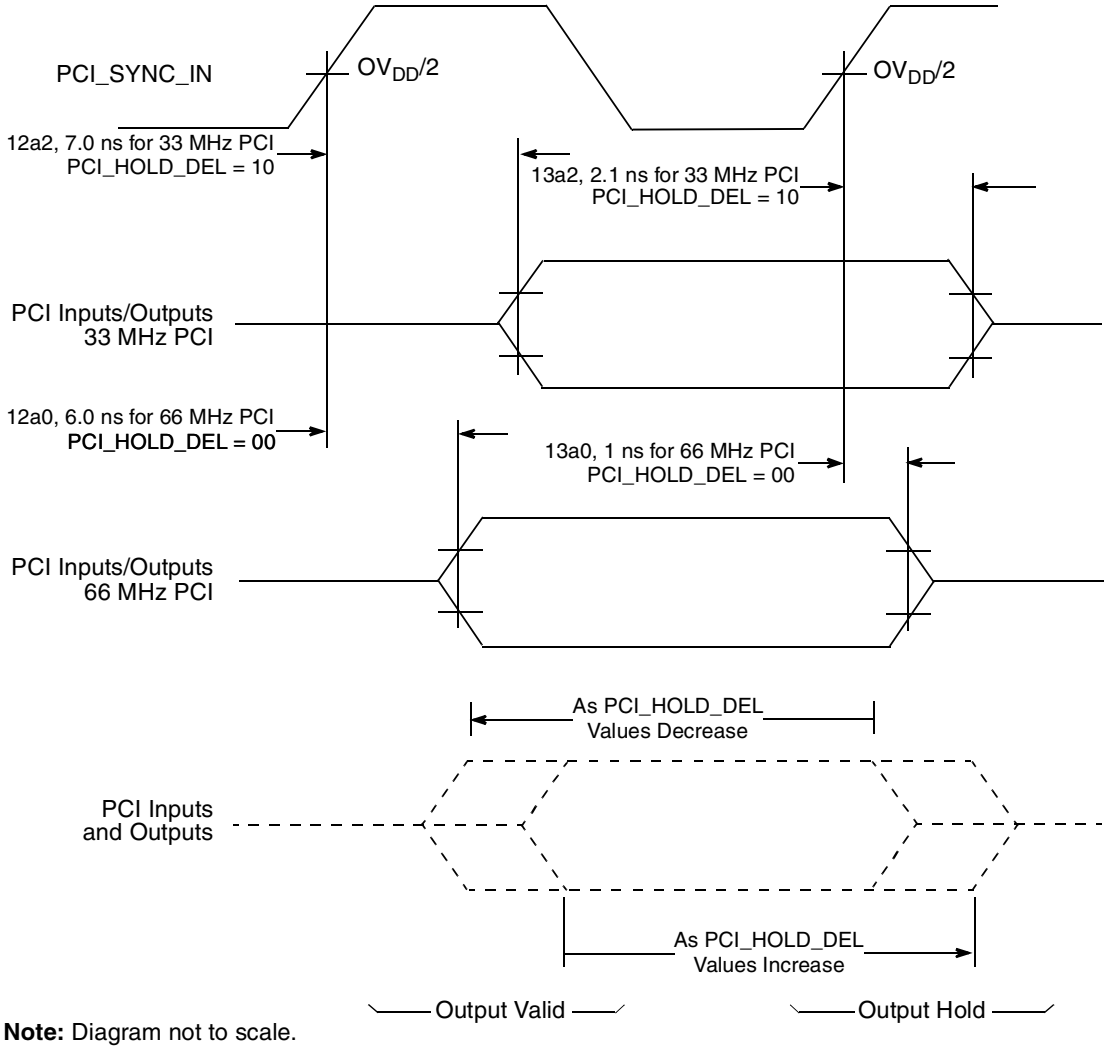


Figure 14. AC Test Load for the MPC8241



Note: Diagram not to scale.

Figure 15. PCI_HOLD_DEL Effect on Output Valid and Hold Time

4.6 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8241.

4.6.1 I²C DC Electrical Characteristics

Table 12 provides the DC electrical characteristics for the I²C interfaces.

Table 12. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
11	TMS, TDI data hold time	15	—	ns	—
12	TCK to TDO data valid	0	15	ns	—
13	TCK to TDO high impedance	0	15	ns	—

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
3. Nontest (other than TDO) signal output timing with respect to TCK.

Figure 20 through Figure 23 show the different timing diagrams for JTAG.

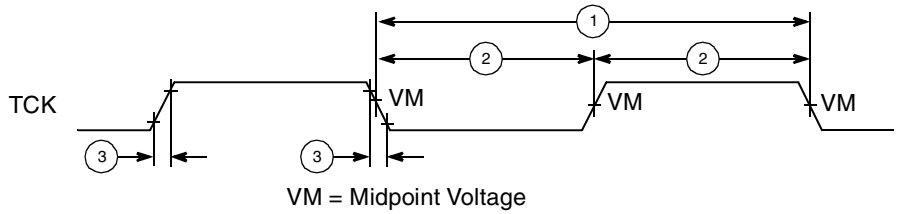


Figure 20. JTAG Clock Input Timing Diagram

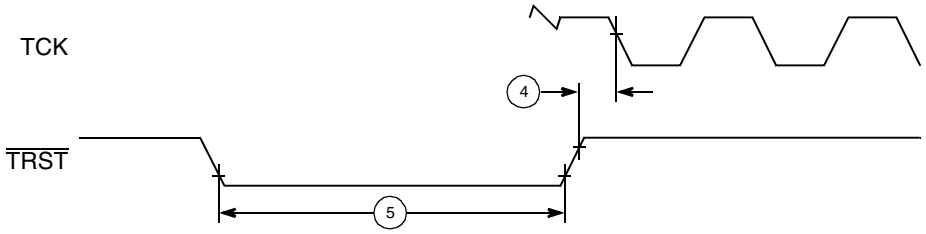


Figure 21. JTAG $\overline{\text{TRST}}$ Timing Diagram

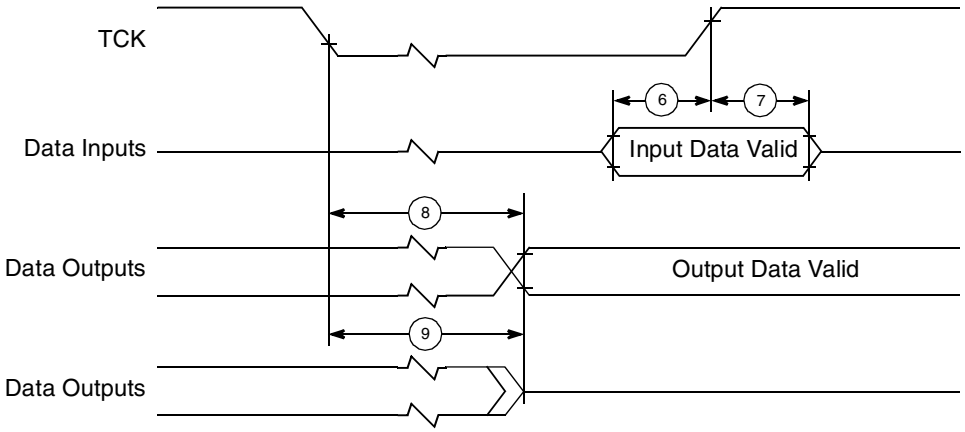


Figure 22. JTAG Boundary Scan Timing Diagram

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
TMS	T18	Input	GV_{DD}_OV_{DD}	—	6, 13
$\overline{TRST}$	R16	Input	GV_{DD}_OV_{DD}	—	6, 13
Power and Ground Signals					
GNDRING/GND	F07 F08 F09 F10 F11 F12 F13 G07 G08 G09 G10 G11 G12 G13 H07 H08 H09 H10 H11 H12 H13 J07 J08 J09 J10 J11 J12 J13 K07 K08 K09 K10 K11 K12 K13 L07 L08 L09 L10 L11 L12 L13 M07 M08 M09 M10 M11 M12 M13 N07 N08 N09 N10 N11 N12 N13 P08 P09 P10 P11 P12 P13 R15	Ground	—	—	17
LV_{DD}	R18 U18 T1 U4 T6 W11 T14	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	—
GV_{DD}_OV_{DD}/PWRRING	D09 D10 D11 E06 E07 E08 E09 E10 E11 E12 E13 E14 F06 F14 G06 G14 H06 H14 J06 J14 K06 K14 L06 L14 M06 M14 N06 N14 P06 P07 P14 R08 R09 R10 R11 R12	Power for memory drivers and PCI/Stnd 3.3 V	GV_{DD}_OV_{DD}	—	18
V_{DD}	F03 H3 L5 N4 P5 V5 U8 W12 W16 R13 P19 L19 H19 F19 F15 C15 A13 A8 B5 A2	Power for core 1.8 V	V_{DD}	—	—
No Connect	N5 W2 B1	—	—	—	—
AV_{DD}	M5	Power for PLL (CPU core logic) 1.8 V	AV_{DD}	—	—
$AV_{DD}2$	R14	Power for PLL (peripheral logic) 1.8 V	$AV_{DD}2$	—	—
Debug/Manufacturing Pins					
DA0/$\overline{QACK}$	A3	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5, 11, 12
DA1/CKO	L1	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5
DA2	R5	Output	GV_{DD}_OV_{DD}	DRV_PCI	19
DA3/PCI_CLK4	V17	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5
DA4/$\overline{REQ4}$	W13	I/O	GV_{DD}_OV_{DD}	—	5, 6
DA5/$\overline{GNT4}$	T11	Output	GV_{DD}_OV_{DD}	DRV_PCI	2, 4, 5

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
DA[10:6]/ PLL_CFG[0:4]	N3 N2 N1 M4 M3	I/O	GV_{DD}_OV_{DD}	—	1, 5, 20
DA[11]	T13	Output	GV_{DD}_OV_{DD}	DRV_PCI	1, 19
DA[12:13]	M16 N16	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	19
DA[14:15]	B6 D8	Output	GV_{DD}_OV_{DD}	DRV_MEM_CTRL	1, 19

Notes:

1. Multi-pin signals such as AD[31:0] or MDL[0:31] physical package pin numbers are listed in order corresponding to the signal names. Ex: AD0 is on pin U1, AD1 is on pin U2,..., AD31 is on pin U13.
2. This pin is affected by a programmable PCI_HOLD_DEL parameter.
3. A weak pull-up resistor (2–10 kΩ) should be placed on this PCI control pin to LV_{DD}.
4. $\overline{\text{GNT4}}$ is a reset configuration pin with an internal pull-up resistor that is enabled only when in the reset state.
5. This pin is a multiplexed signal and appears more than once in this table.
6. This pin has an internal pull-up resistor that is enabled at all times. The value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
7. This pin is a sustained three-state pin as defined by the *PCI Local Bus Specification* (Rev. 2.2).
8. This pin is an open-drain signal.
9. DL[0] is a reset configuration pin with an internal pull-up resistor that is enabled only when in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
10. This pin has an internal pull-up resistor that is enabled only when in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
11. This pin is a reset configuration pin.
12. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to GV_{DD}_OV_{DD}.
13. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 3.
14. External PCI clocking source or fanout buffer may be required for system if using the MPC8241 DUART functionality because PCI_CLK[0:3] are not available in DUART mode. Only PCI_CLK4 is available in DUART mode.
15. OSC_IN uses the 3.3-V PCI interface driver, which is 5-V tolerant. See Table 2 for details.
16. This pin can be programmed as driven (default) or as open-drain (in MIOCR 1).
17. All grounded pins are connected together. Connections should not be made to individual pins. The list represents the balls that are connected to ground.
18. GV_{DD}_OV_{DD} must not exceed V_{DD}/AV_{DD}/AV_{DD}2 by more than 1.8 V at any time including during power-on reset. Note that GV_{DD}_OV_{DD} pins are all shorted together, PWRRING. The list represents the balls that are connected to PWRRING. Connections should not be made to individual PWRRING pins.
19. Treat these pins as no connects unless debug address functionality is used.
20. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ in order to be latched.
21. Place a pull-up resistor of 120 Ω or less on the $\overline{\text{TEST0}}$ pin.
22. SDRAM_CLK[0:3] and SDRAM_SYNC_OUT signals use DRV_MEM_CTRL for chip Rev. 1.1 (A). These signals use DRV_MEM_CLK for chip Rev. 1.2B.
23. The driver capability of this pin is hardwired to 40 Ω and cannot be changed.
24. Freescale typically expects that customers using the serial port will have sufficient drivers available in the RS232 transceiver to drive the $\overline{\text{CTS}}$ pin actively as an input if they are using that mode. No pullups would be needed in these circumstances.
25. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state

7.6 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port, with additional status monitoring signals. The COP port must independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 27 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 27, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 27. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 27 is common to all known emulators.

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

7.7.3 Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (ψ_{JT}) measures the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\psi_{JT} \times P_D)$$

8.1 Part Numbers Fully Addressed by This Document

Table 19 provides the Freescale part numbering nomenclature for the MPC8241. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number. Read the Revision ID register at address offset 0x08 to determine the revision level.

Table 19. Part Numbering Nomenclature

MPC	*nnnn*	L	*xx*	*nnn*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency [2] (MHz)**	**Revision Level**
MPC	8241	L = Standard spec. 0° to 105°C	ZQ = thick substrate and thick mold cap PBGA (two layers)	166, 200 1.8 V ± 100 mV	D:1.4 = Rev. ID:0x14
			ZQ = thick substrate and thick mold cap PBGA (four layers, thermally enhanced)	266 1.8 V ± 100 mV	
			VR = Lead-free version of package	166, 200, 266 1.8 V ± 100 mV	

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by hardware specifications addendums may support other maximum core frequencies.

8.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specifications addendums that supplement and supersede this document (see Table 20).

Table 20. Part Numbers Addressed by MPC8241TXXPNS Series (Document No. MPC8241ECSO1AD))

MPC	*nnnn*	T	*xx*	*nnn*	*x*	
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency [2] (MHz)**	**Revision Level**	**Processor Version Register Value**

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
8	12/19/2005	Document—Imported new template and made minor editoral corrections. Section 4.3.1—Before Figure 7, added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3. Section 4.3.2—After Figure 12, added a sentence to introduce Figure 13. Section 4.3.3—After Table 11, added a sentence to introduce Figure 14. Section 4.3.4—After Table 13, added to the sentence to introduce Figures 16 thru 19. Section 4.3.6—After Table 16, added a sentence to introduce Figures 22 thru 25. Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2. Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated Section 9.2 to reflect what we offer for new orders. Updated Figure 34 to match with current part marking format. Section 8.3—Added new section for part marking information.
7	05/11/2004	Section 4.1.4 —Table 4: Changed the default for drive strength of DRV_STD_MEM. Section 4.3.1 —Table 8: Changed the wording for item 15 description. Section 4.3.4 —Table 10: Changed T_{os} range and wording in note 7; Figure 11: changed wording for SDRAM_SYNC_IN description relative to T_{OS}.
6.1	—	Section 4.3.1 — Table 9: Corrected last row to state the correct description for the bit setting: Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay”
6	—	Section 4.1.2 — Figure 2: Added note 6 and related label for latching of the PLL_CFG signals. Section 4.1.3 — Updated specifications for the input high and input low voltages of PCI_SYNC_IN. Section 4.3.1 — Table 8: Corrected typo for first number 1a to 1; Updated characteristics for the DLL lock range for the default and remaining three DLL locking modes; Reworded note description for note 6. Replaced contents of Table 9 with bit descriptions for the four DLL locking modes. In Figures 7 through 10, updated the DLL locking mode graphs. Section 4.3.2 — Table 10: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 4.3.3— Table 11: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 5.3 — Table 17: Removed extra listing of DRDY in test/configuration signal list and updated relevant notes for signal in memory Interface signal listing. Updated note #20. Added note 24 for the signals of the UART interface. Section 7.6 — Added relevant notes to this section and updated Figure 29.
5	—	Section 5.1— Updated package information to include all package offerings. Section 5.2 — Included package case outline for ZP (Rev. B) packaging parts. Section 9 — Updated Part markings for the offerings of the MPC8241. All sections — Nontechnical reformatting