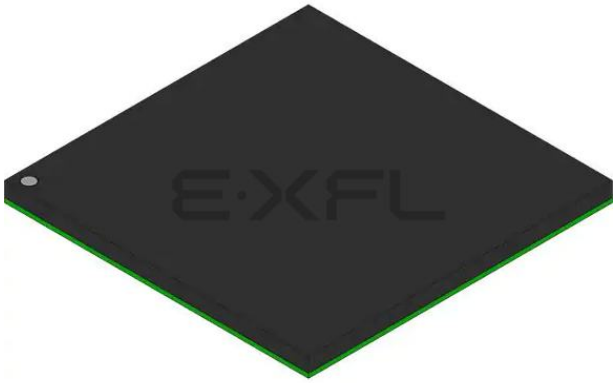

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8241tzq166d

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I_2O interface), and an I^2C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, 16-Kbyte instruction cache, 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

An internal peripheral logic bus interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade performance for power consumption. The processor core is clocked from a separate PLL that is referenced to the peripheral logic PLL, allowing the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8241 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The general-purpose processor core and peripheral logic serve a variety of embedded applications. The MPC8241 can be used as either a PCI host or PCI agent controller.

2 Features

Major features of the MPC8241 are as follows:

- Processor core
  - — High-performance, superscalar processor core
  - — Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and a branch processing unit (BPU)
  - — 16-Kbyte instruction cache
  - — 16-Kbyte data cache
  - — Lockable L1 caches—entire cache or on a per-way basis up to three of four ways
  - — Dynamic power management—supports 60x nap, doze, and sleep modes
- Peripheral logic
  - — Peripheral logic bus
    - – Various operating frequencies and bus divider ratios
    - – 32-bit address bus, 64-bit data bus
    - – Full memory coherency
    - – Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - – Store gathering on peripheral logic bus-to-PCI writes
  - — Memory interface
    - – Up to 2 Gbytes of SDRAM memory
    - – High-bandwidth data bus (32- or 64-bit) to SDRAM
    - – Programmable timing for SDRAM
    - – One to 8 banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices

  - I^2C controller with full master/slave support that accepts broadcast messages
  - Programmable interrupt controller (PIC)
    - Five hardware interrupts (IRQs) or 16 serial interrupts
    - Four programmable timers with cascade
  - Two (dual) universal asynchronous receiver/transmitters (UARTs)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI bus and memory interface output drivers
- System level performance monitor facility
- Debug features
  - Memory attribute and PCI attribute signals
  - Debug address signals
  - $\overline{\text{MIV}}$ signal—marks valid address and data bus cycles on the memory bus
  - Programmable input and output signals with watchpoint capability
  - Error injection/capture on data path
  - IEEE Std. 1149.1 (JTAG)/test interface

3 General Parameters

The following list summarizes the general parameters of the MPC8241:

Technology	0.25 µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully static
Packages	Surface-mount 357 (thick substrate and thick mold cap) plastic ball grid array (PBGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 2 for details and recommended operating conditions)
I/O power supply	3.0 to 3.6 V DC

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8241.

Table 2. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply voltage		V_{DD}	1.8 ± 100 mV	V	2
I/O buffer supply for PCI and standard; supply voltages for memory bus drivers		$GV_{DD}\_OV_{DD}$	3.3 ± 0.3	V	2
CPU PLL supply voltage		AV_{DD}	1.8 ± 100 mV		2
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8 ± 100 mV	V	2
PCI reference		LV_{DD}	5.0 ± 5%	V	4, 5, 6
			3.3 ± 0.3	V	5, 6, 7
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	4, 7
	All other inputs		0 to 3.6	V	8
Die-junction temperature		T_j	0 to 105	•C	

Notes:

1. Freescale has tested these operating conditions and recommends them. Proper device operation outside of these conditions is not guaranteed.
2. **Caution:** $GV_{DD}\_OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 1.8 V at any time including during power-on reset. Note that $GV_{DD}\_OV_{DD}$ pins are all shorted together: This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. Connections should not be made to individual PWRRING pins.
3. **Caution:** $V_{DD}/AV_{DD}/AV_{DD}2$ must not exceed $GV_{DD}\_OV_{DD}$ by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 5.0 V DC power supply.
5. **Caution:** LV_{DD} must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** LV_{DD} must not exceed $GV_{DD}\_OV_{DD}$ by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3 V DC power supply.
8. **Caution:** Input voltage (V_{in}) must not be greater than the supply voltage ($V_{DD}/AV_{DD}/AV_{DD}2$) by more than 2.5 V at all times including during power-on reset. Input voltage (V_{in}) must not be greater than $GV_{DD}\_OV_{DD}$ by more than 0.6 V at all times including during power-on reset.

Table 3. DC Electrical Specifications (continued)

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Capacitance	V_{in} = 0 V, f = 1 MHz	C_{in}	—	16.0	pF	

Notes:
1. See Table 16 for pins with internal pull-up resistors.
2. All grounded pins are connected together.
3. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} or both GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} must vary in the same direction.
4. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 16.

4.2.1 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 16. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8241 Output Pins [5, 6]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20 (default)	GV_{DD}_OV_{DD} = 3.3 V	36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)		89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) where table entry voltage = GV_{DD}_OV_{DD} – PCI V_{OH}.
2. For all others with GV_{DD}_ OV_{DD} = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = GV_{DD}_OV_{DD} – V_{OH}.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.
4. For all others with GV_{DD}_OV_{DD} = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4-V table entry.
5. See driver bit details for output driver control register (0x73) in the *MPC8245 Integrated Processor Reference Manual*.
6. See Chip Errata No. 19 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*.

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 through 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines,* for details on MPC8241 memory clock design.
7. Rise and fall times for the OSC_IN input are guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram, and Figure 7 through Figure 10 show the DLL locking range loop delay versus frequency of operation.

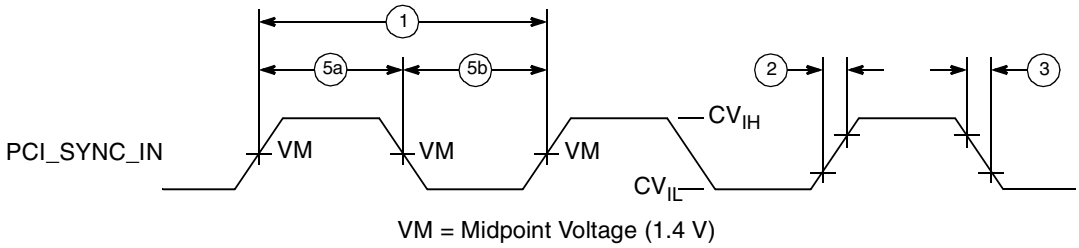


Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

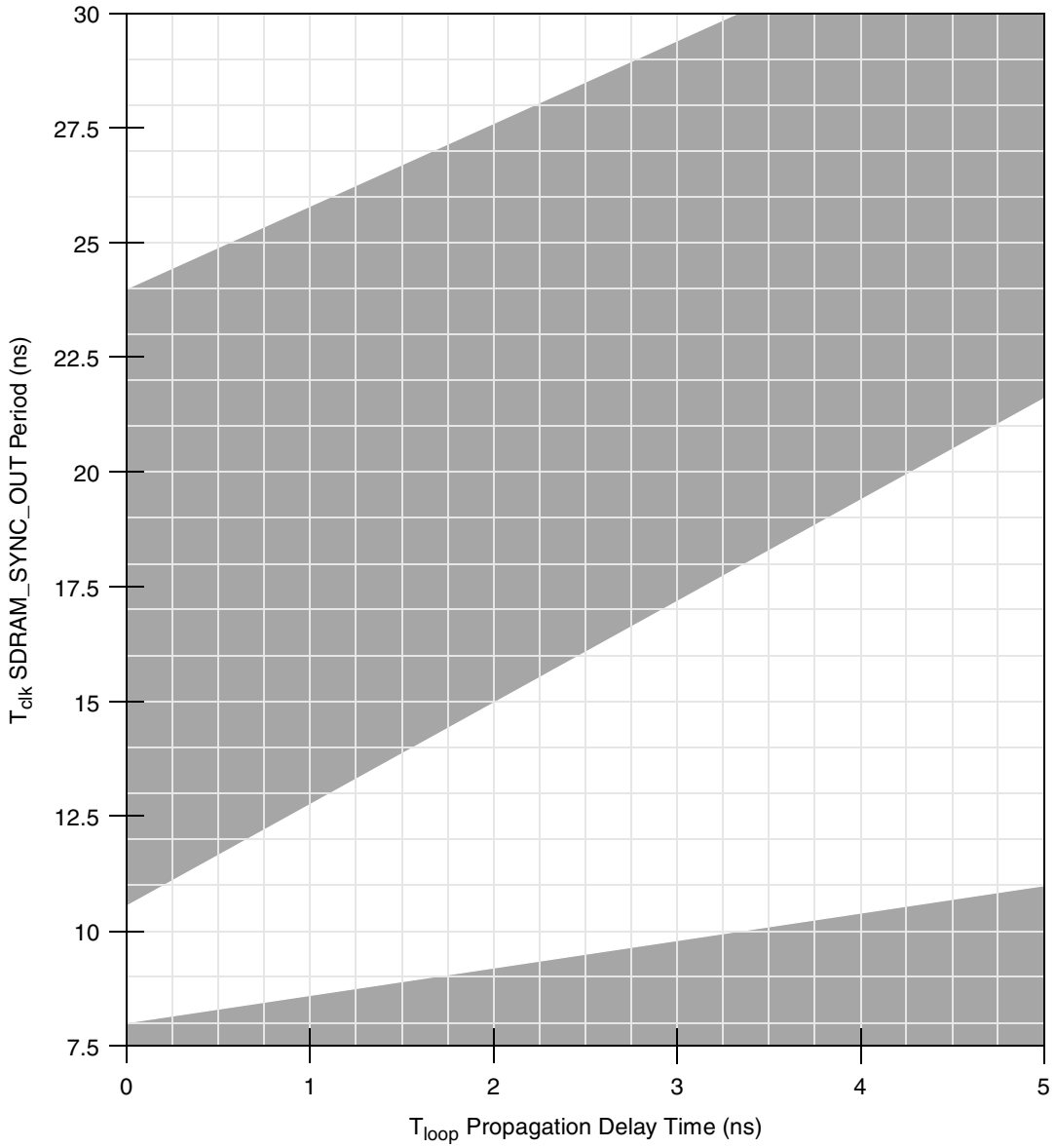


Figure 8. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=1 and Normal Tap Delay

Figure 13 shows the input timing diagram for mode select signals.

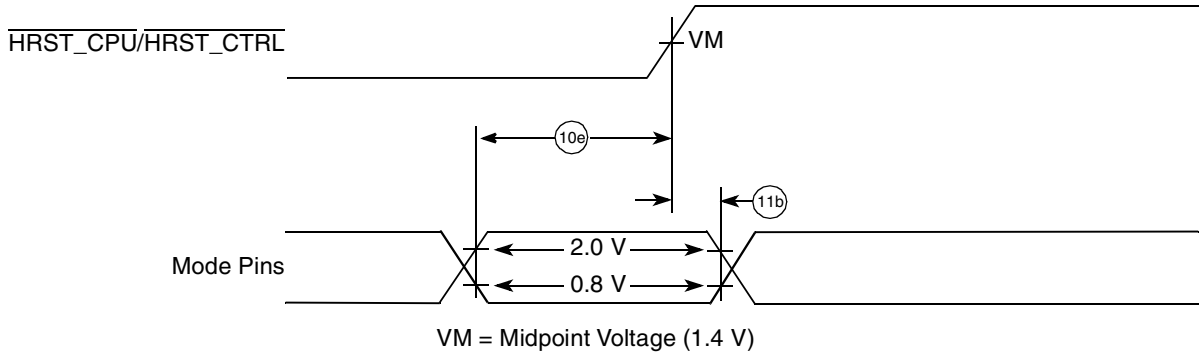


Figure 13. Input Timing Diagram for Mode Select Signals

4.5.3 Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V (see Figure 11). All output timings assume a purely resistive 50-Ω load (see Figure 14). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths that Table 4 indicates.

Table 11. Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, see Figure 15				
12a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{\text{MCP}}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{\text{MCP}}$,CKE] = 00	—	7.5		
12b	*sys_logic_clk* to output valid (memory address, control, and data signals)	—	4.5	ns	2
12c	*sys_logic_clk* to output valid (for all others)	—	7.0	ns	2
12d	*sys_logic_clk* to output valid (for I^2C)	—	5.0	ns	2
12e	*sys_logic_clk* to output valid (ROM/Flash/Port X)	—	6.0	ns	2
13a	Output hold (PCI), see Figure 15				
13a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{\text{MCP}}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{\text{MCP}}$,CKE] = 00	3.5	—		
13b	Output hold (all others)	1.0	—	ns	2
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	1, 3

Table 12. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8245 Integrated Processor Reference Manual* for information on the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if the OV_{DD} is switched off.

4.6.2 I^2C AC Electrical Specifications

Table 13 provides the AC timing parameters for the I^2C interfaces.

Table 13. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	µs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	µs
Data output delay time:	t_{I2OVKL}	—	0.9[3]	
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

Figure 17 shows the AC timing diagram for the I^2C bus.

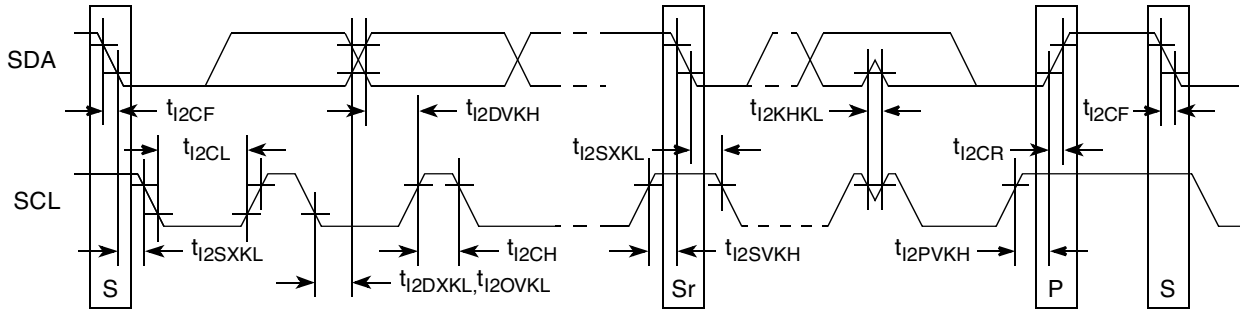


Figure 17. I^2C Bus AC Timing Diagram

4.7 PIC Serial Interrupt Mode AC Timing Specifications

Table 14 provides the PIC serial interrupt mode AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with GV_{DD}–OV_{DD} = 3.3 V ± 5% and LV_{DD} = 3.3 V ± 0.3 V.

Table 14. PIC Serial Interrupt Mode AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	S_CLK frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	1
2	S_CLK duty cycle	40	60	%	—
3	S_CLK output valid time	—	6	ns	—
4	Output hold time	0	—	ns	—
5	$\overline{\text{S\_FRAME}}$, S_RST output valid time	—	1 *sys_logic_clk* period + 6	ns	2
6	S_INT input setup time to S_CLK	1 *sys_logic_clk* period + 2	—	ns	2
7	S_INT inputs invalid (hold time) to S_CLK	—	0	ns	2

Notes:

1. See the *MPC8245 Integrated Processor Reference Manual* for a description of the PIC interrupt control register (ICR) and S_CLK frequency programming.
2. S_RST, $\overline{\text{S\_FRAME}}$, and S_INT shown in Figure 18 and Figure 19, depict timing relationships to *sys_logic_clk* and S_CLK and do not describe functional relationships between S_RST, $\overline{\text{S\_FRAME}}$, and S_INT. The *MPC8245 Integrated Processor Reference Manual* describes the functional relationships between these signals.
3. The *sys_logic_clk* waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; *sys_logic_clk* is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the *MPC8245 Integrated Processor Reference Manual* for a complete clocking description.

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
TMS	T18	Input	GV_{DD}_OV_{DD}	—	6, 13
$\overline{TRST}$	R16	Input	GV_{DD}_OV_{DD}	—	6, 13
Power and Ground Signals					
GNDRING/GND	F07 F08 F09 F10 F11 F12 F13 G07 G08 G09 G10 G11 G12 G13 H07 H08 H09 H10 H11 H12 H13 J07 J08 J09 J10 J11 J12 J13 K07 K08 K09 K10 K11 K12 K13 L07 L08 L09 L10 L11 L12 L13 M07 M08 M09 M10 M11 M12 M13 N07 N08 N09 N10 N11 N12 N13 P08 P09 P10 P11 P12 P13 R15	Ground	—	—	17
LV_{DD}	R18 U18 T1 U4 T6 W11 T14	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	—
GV_{DD}_OV_{DD}/PWRRING	D09 D10 D11 E06 E07 E08 E09 E10 E11 E12 E13 E14 F06 F14 G06 G14 H06 H14 J06 J14 K06 K14 L06 L14 M06 M14 N06 N14 P06 P07 P14 R08 R09 R10 R11 R12	Power for memory drivers and PCI/Stnd 3.3 V	GV_{DD}_OV_{DD}	—	18
V_{DD}	F03 H3 L5 N4 P5 V5 U8 W12 W16 R13 P19 L19 H19 F19 F15 C15 A13 A8 B5 A2	Power for core 1.8 V	V_{DD}	—	—
No Connect	N5 W2 B1	—	—	—	—
AV_{DD}	M5	Power for PLL (CPU core logic) 1.8 V	AV_{DD}	—	—
$AV_{DD}2$	R14	Power for PLL (peripheral logic) 1.8 V	$AV_{DD}2$	—	—
Debug/Manufacturing Pins					
DA0/$\overline{QACK}$	A3	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5, 11, 12
DA1/CKO	L1	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5
DA2	R5	Output	GV_{DD}_OV_{DD}	DRV_PCI	19
DA3/PCI_CLK4	V17	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5
DA4/$\overline{REQ4}$	W13	I/O	GV_{DD}_OV_{DD}	—	5, 6
DA5/$\overline{GNT4}$	T11	Output	GV_{DD}_OV_{DD}	DRV_PCI	2, 4, 5

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
DA[10:6]/ PLL_CFG[0:4]	N3 N2 N1 M4 M3	I/O	GV_{DD}_OV_{DD}	—	1, 5, 20
DA[11]	T13	Output	GV_{DD}_OV_{DD}	DRV_PCI	1, 19
DA[12:13]	M16 N16	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	19
DA[14:15]	B6 D8	Output	GV_{DD}_OV_{DD}	DRV_MEM_CTRL	1, 19

Notes:

1. Multi-pin signals such as AD[31:0] or MDL[0:31] physical package pin numbers are listed in order corresponding to the signal names. Ex: AD0 is on pin U1, AD1 is on pin U2,..., AD31 is on pin U13.
2. This pin is affected by a programmable PCI_HOLD_DEL parameter.
3. A weak pull-up resistor (2–10 kΩ) should be placed on this PCI control pin to LV_{DD}.
4. $\overline{\text{GNT4}}$ is a reset configuration pin with an internal pull-up resistor that is enabled only when in the reset state.
5. This pin is a multiplexed signal and appears more than once in this table.
6. This pin has an internal pull-up resistor that is enabled at all times. The value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
7. This pin is a sustained three-state pin as defined by the *PCI Local Bus Specification* (Rev. 2.2).
8. This pin is an open-drain signal.
9. DL[0] is a reset configuration pin with an internal pull-up resistor that is enabled only when in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
10. This pin has an internal pull-up resistor that is enabled only when in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
11. This pin is a reset configuration pin.
12. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to GV_{DD}_OV_{DD}.
13. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 3.
14. External PCI clocking source or fanout buffer may be required for system if using the MPC8241 DUART functionality because PCI_CLK[0:3] are not available in DUART mode. Only PCI_CLK4 is available in DUART mode.
15. OSC_IN uses the 3.3-V PCI interface driver, which is 5-V tolerant. See Table 2 for details.
16. This pin can be programmed as driven (default) or as open-drain (in MIOCR 1).
17. All grounded pins are connected together. Connections should not be made to individual pins. The list represents the balls that are connected to ground.
18. GV_{DD}_OV_{DD} must not exceed V_{DD}/AV_{DD}/AV_{DD}2 by more than 1.8 V at any time including during power-on reset. Note that GV_{DD}_OV_{DD} pins are all shorted together, PWRRING. The list represents the balls that are connected to PWRRING. Connections should not be made to individual PWRRING pins.
19. Treat these pins as no connects unless debug address functionality is used.
20. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ in order to be latched.
21. Place a pull-up resistor of 120 Ω or less on the $\overline{\text{TEST0}}$ pin.
22. SDRAM_CLK[0:3] and SDRAM_SYNC_OUT signals use DRV_MEM_CTRL for chip Rev. 1.1 (A). These signals use DRV_MEM_CLK for chip Rev. 1.2B.
23. The driver capability of this pin is hardwired to 40 Ω and cannot be changed.
24. Freescale typically expects that customers using the serial port will have sufficient drivers available in the RS232 transceiver to drive the $\overline{\text{CTS}}$ pin actively as an input if they are using that mode. No pullups would be needed in these circumstances.
25. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state

6 PLL Configuration

The PLL_CFG[0:4] are configured by the internal PLLs. For a specific PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations are shown in Table 17 and Table 18.

Table 17. PLL Configurations (166- and 200-MHz)

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	Not available			25-26[5]	75-78	188-195	3 (2)	2.5 (2)
2	00010	34[4]–37[5]	34–37	153–166	34[4]–44[5]	34–44	153–200	1 (4)	4.5 (2)
3	00011[6]	50[7]–66[3]	50–66	100–132	50[7]–66[3]	50–66	100–132	1 (Bypass)	2 (4)
4	00100	25–41[5]	50–82	100–164	25–44[8,10]	50–88	100–176	2 (4)	2 (4)
6	00110[9]	Bypass			Bypass			Bypass	Bypass
7 Rev. B	00111[6]	50[4]–55 [5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (Bypass)	3 (2)
7 Rev. D	00111	Not available							
8	01000	50[4]–55[5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (4)	3 (2)
9	01001	38[4]–41[5,11]	76–82	152–164	38[4]–50[5,12]	76–100	152–200	2 (2)	2 (2)
B	01011	Not available			44[5]	66	198	2(2)	2.5(2)
C	01100	30[4]–33[5]	60–66	150–165	30[4]–40[5]	60–80	150–200	2 (4)	2.5 (2)
E	01110	25–27[5]	50–54	150–162	25–33[5]	60–66	150–198	2 (4)	3 (2)
10	10000	25–27[5,11]	75–83	150–166	25–33[5,12]	75–100	150–200	3 (2)	2 (2)
12	10010	50[4]–55[5,11]	75–83	150–166	50[4]–66[3]	75–99	150–198	1.5 (2)	2 (2)
14	10100	Not available			25–28[5]	50–56	175–196	2 (4)	3.5 (2)
16	10110				25[5]	50	200	2(4)	4(2)
17	10111				25[5]	100	200	4(2)	2(2)
19	11001	33[5,13]	66	165	33[13]–40[5]	66–80	165–200	2(2)	2.5(2)
1A	11010	37[4]–41[5]	37–41	150–166	37[4]–50[5]	37–50	150–200	1 (4)	4 (2)
1B	11011	Not available			33[5,13]	66	198	2(2)	3(2)
1C	11100				44[5,13]	66	198	1.5(2)	3(2)
1D	11101	44[5,13]	66	166	44[13]–53[5]	66–80	165–200	1.5 (2)	2.5 (2)

Table 17. PLL Configurations (166- and 200-MHz) (continued)

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1E	11110[14]	Not usable			Not usable			Off	Off
1F	11111[14]	Not usable			Not usable			Off	Off

Notes:

1. PLL_CFG[0:4] settings not listed are reserved. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value. Note the impact of the relevant revisions for mode 7.
2. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
3. Limited by maximum PCI input frequency (66 MHz).
4. Limited by minimum CPU VCO frequency (300 MHz).
5. Limited by maximum CPU operating frequency.
6. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
7. Limited by minimum CPU operating frequency (100 MHz).
8. Limited due to maximum memory VCO frequency (352 MHz).
9. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
10. Limited by maximum CPU VCO frequency (704 MHz).
11. Limited by maximum system memory interface operating frequency (83 MHz @ 166 MHz CPU bus speed).
12. Limited by maximum system memory interface operating frequency (100 MHz @ 200 MHz CPU bus speed).
13. Limited by minimum memory VCO frequency (132 MHz).
14. In clock off mode, no clocking occurs inside the MPC8241, regardless of the PCI_SYNC_IN input.

Table 18. PLL Configurations (266-MHz Parts)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	25–35[5]	75–105	188–263	3 (2)	2.5 (2)
1	00001	25–29[5]	75–88	225–264	3 (2)	3 (2)
2	00010	50[15]–59[5]	50–59	225–266	1 (4)	4.5 (2)
3	00011[12]	50[14]–66[1]	50–66	100–133	1 (Bypass)	2 (4)
4	00100	25–44[4]	50–88	100–176	2 (4)	2 (4)

Table 18. PLL Configurations (266-MHz Parts) (continued)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Off	Off

Notes:

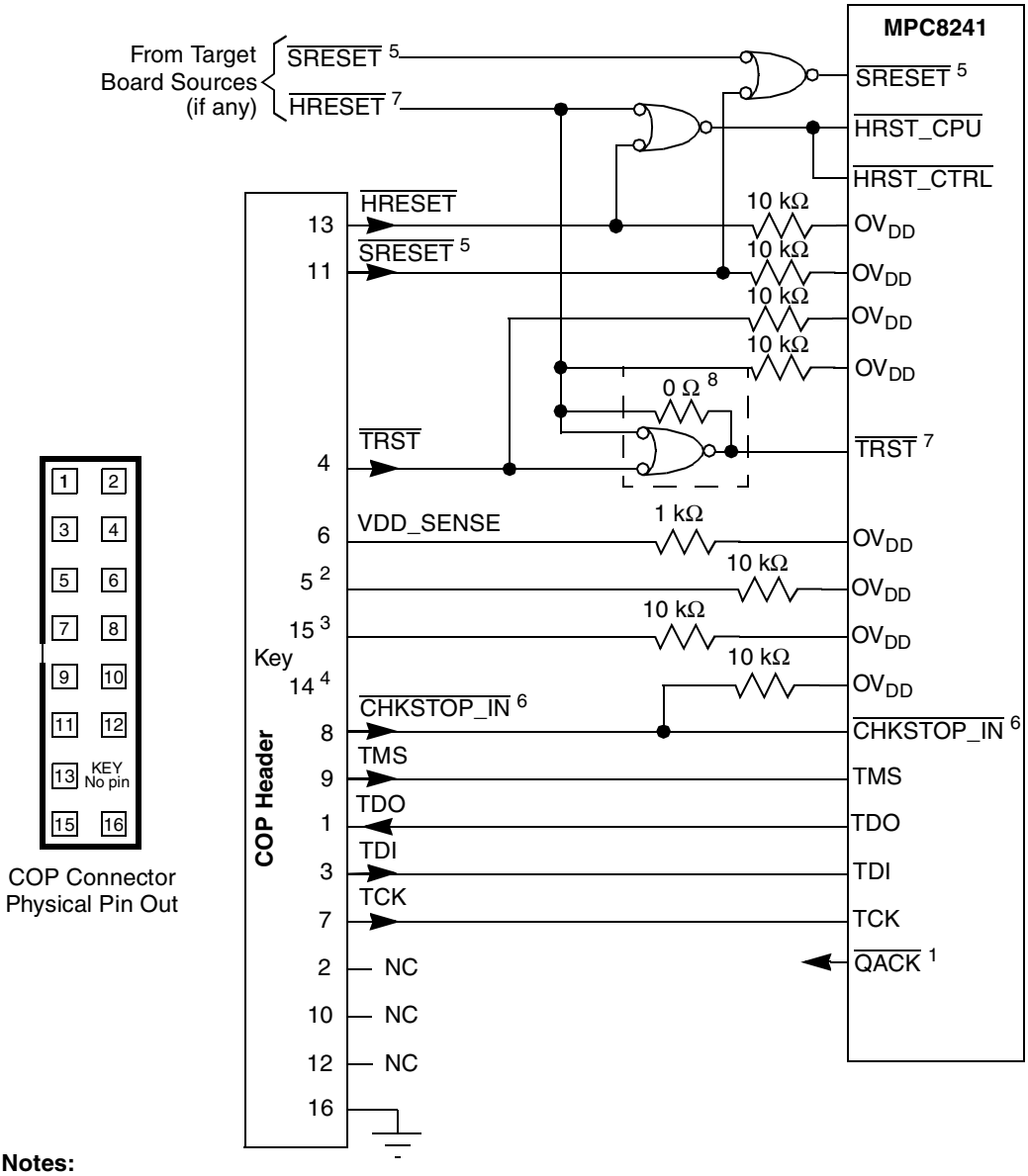
1. Limited by maximum PCI input frequency (66 MHz).
2. Note the impact of the relevant revisions for modes 7 and 1E.
3. Limited by minimum memory VCO frequency (132 MHz).
4. Limited due to maximum memory VCO frequency (352 MHz).
5. Limited by maximum CPU operating frequency.
6. Limited by minimum CPU VCO frequency (300 MHz).
7. Limited by maximum CPU VCO frequency (704 MHz).
8. In clock off mode, no clocking occurs inside the MPC8241, regardless of the PCI_SYNC_IN input.
9. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
10. PLL_CFG[0:4] settings that are not listed are reserved.
11. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
12. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
13. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
14. Limited by minimum CPU operating frequency (100 MHz).
15. Limited by minimum memory bus frequency (50 MHz).

7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8241.

7.1 PLL Power Supply Filtering

The AV_{DD} and $AV_{DD}2$ power signals on the MPC8241 provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and $AV_{DD}2$ input signals should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 26 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD} and $AV_{DD}2$ power signal pins. In *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), Dr. Howard Johnson recommends using multiple small capacitors of equal value instead of multiple values.



Notes:

1. $\overline{\text{QACK}}$ is an output and is not required at the COP header for emulation.
2. RUN/$\overline{\text{STOP}}$ normally on pin 5 of the COP header is not implemented on the MPC8241. Connect pin 5 of the COP header to OV_{DD} with a 1- kΩ pull-up resistor.
3. $\overline{\text{CKSTP\_OUT}}$ normally on pin 15 of the COP header is not implemented on the MPC8241. Connect pin 15 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
4. Pin 14 is not physically present on the COP header.
5. $\overline{\text{SRESET}}$ functions as output SDMA12 in extended ROM mode.
6. $\overline{\text{CHKSTOP\_IN}}$ functions as output SDMA14 in extended ROM mode.
7. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown.
8. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header through an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.

Figure 27. COP Connector Diagram

7.7 Thermal Management

This section provides thermal management information for the plastic ball grid array (PBGA) package for air-cooled applications. Depending on the application environment and the operating frequency, a heat sink may be required to maintain junction temperature within specifications. Proper thermal control design primarily depends on the system-level design: heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks can be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, or mounting clip and screw assembly (see Figure 28).

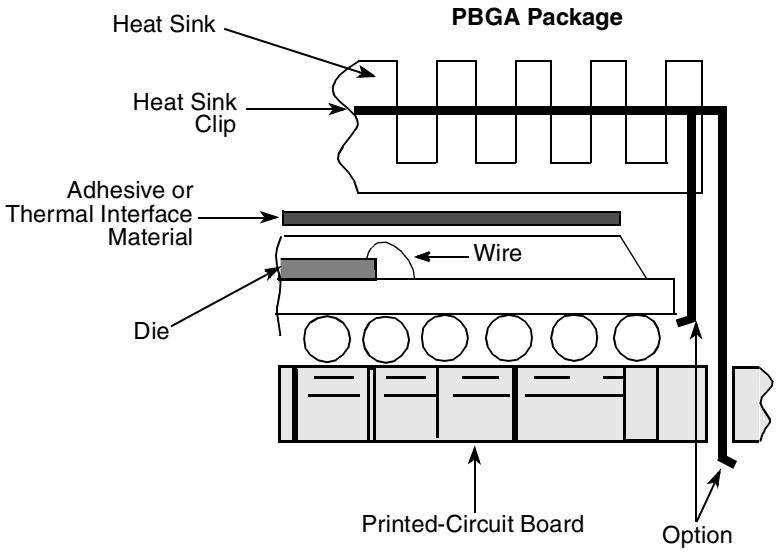


Figure 28. Package Exploded Cross-Sectional View with Several Heat Sink Options

Figure 29 depicts the die junction-to-ambient thermal resistance for four typical cases:

- A heat sink is not attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s).
- A heat sink is not attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s/sink).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p/sink).

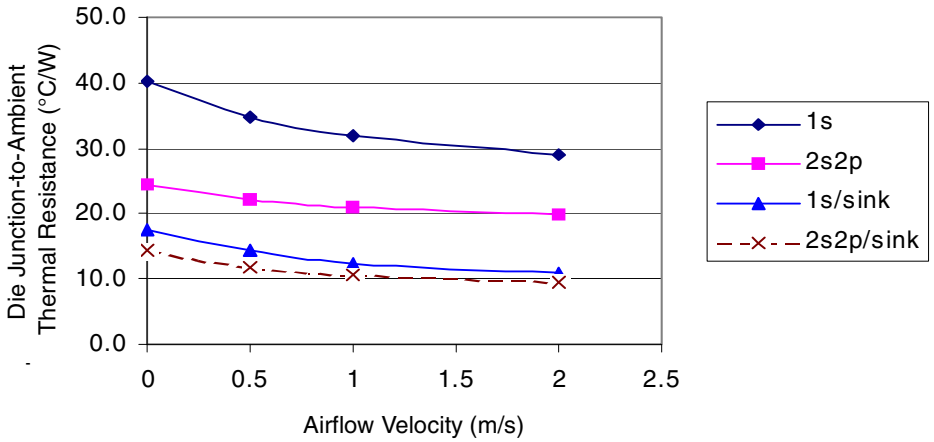


Figure 29. Die Junction-to-Ambient Resistance

The board designer can choose among several types of heat sinks to place on the MPC8241. Several commercially available heat sinks for the MPC8241 are provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

7.7.3 Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (ψ_{JT}) measures the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature atop the package (°C)
ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance minimizes the change in thermal performance that is caused by removing part of the thermal interface to the heat sink. Considering the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

In many cases, it is appropriate to simulate the system environment using a computational fluid dynamics thermal simulation tool. In such a tool, the simplest thermal model of a package that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board.

7.8 References

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

8 Ordering Information

Ordering information for the parts that this document fully covers is provided in Section 8.1, “Part Numbers Fully Addressed by This Document.” Section 8.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
8	12/19/2005	Document—Imported new template and made minor editoral corrections. Section 4.3.1—Before Figure 7, added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3. Section 4.3.2—After Figure 12, added a sentence to introduce Figure 13. Section 4.3.3—After Table 11, added a sentence to introduce Figure 14. Section 4.3.4—After Table 13, added to the sentence to introduce Figures 16 thru 19. Section 4.3.6—After Table 16, added a sentence to introduce Figures 22 thru 25. Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2. Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated Section 9.2 to reflect what we offer for new orders. Updated Figure 34 to match with current part marking format. Section 8.3—Added new section for part marking information.
7	05/11/2004	Section 4.1.4 —Table 4: Changed the default for drive strength of DRV_STD_MEM. Section 4.3.1 —Table 8: Changed the wording for item 15 description. Section 4.3.4 —Table 10: Changed T_{os} range and wording in note 7; Figure 11: changed wording for SDRAM_SYNC_IN description relative to T_{OS}.
6.1	—	Section 4.3.1 — Table 9: Corrected last row to state the correct description for the bit setting: Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay”
6	—	Section 4.1.2 — Figure 2: Added note 6 and related label for latching of the PLL_CFG signals. Section 4.1.3 — Updated specifications for the input high and input low voltages of PCI_SYNC_IN. Section 4.3.1 — Table 8: Corrected typo for first number 1a to 1; Updated characteristics for the DLL lock range for the default and remaining three DLL locking modes; Reworded note description for note 6. Replaced contents of Table 9 with bit descriptions for the four DLL locking modes. In Figures 7 through 10, updated the DLL locking mode graphs. Section 4.3.2 — Table 10: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 4.3.3— Table 11: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 5.3 — Table 17: Removed extra listing of DRDY in test/configuration signal list and updated relevant notes for signal in memory Interface signal listing. Updated note #20. Added note 24 for the signals of the UART interface. Section 7.6 — Added relevant notes to this section and updated Figure 29.
5	—	Section 5.1— Updated package information to include all package offerings. Section 5.2 — Included package case outline for ZP (Rev. B) packaging parts. Section 9 — Updated Part markings for the offerings of the MPC8241. All sections — Nontechnical reformatting