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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8241tzq200d

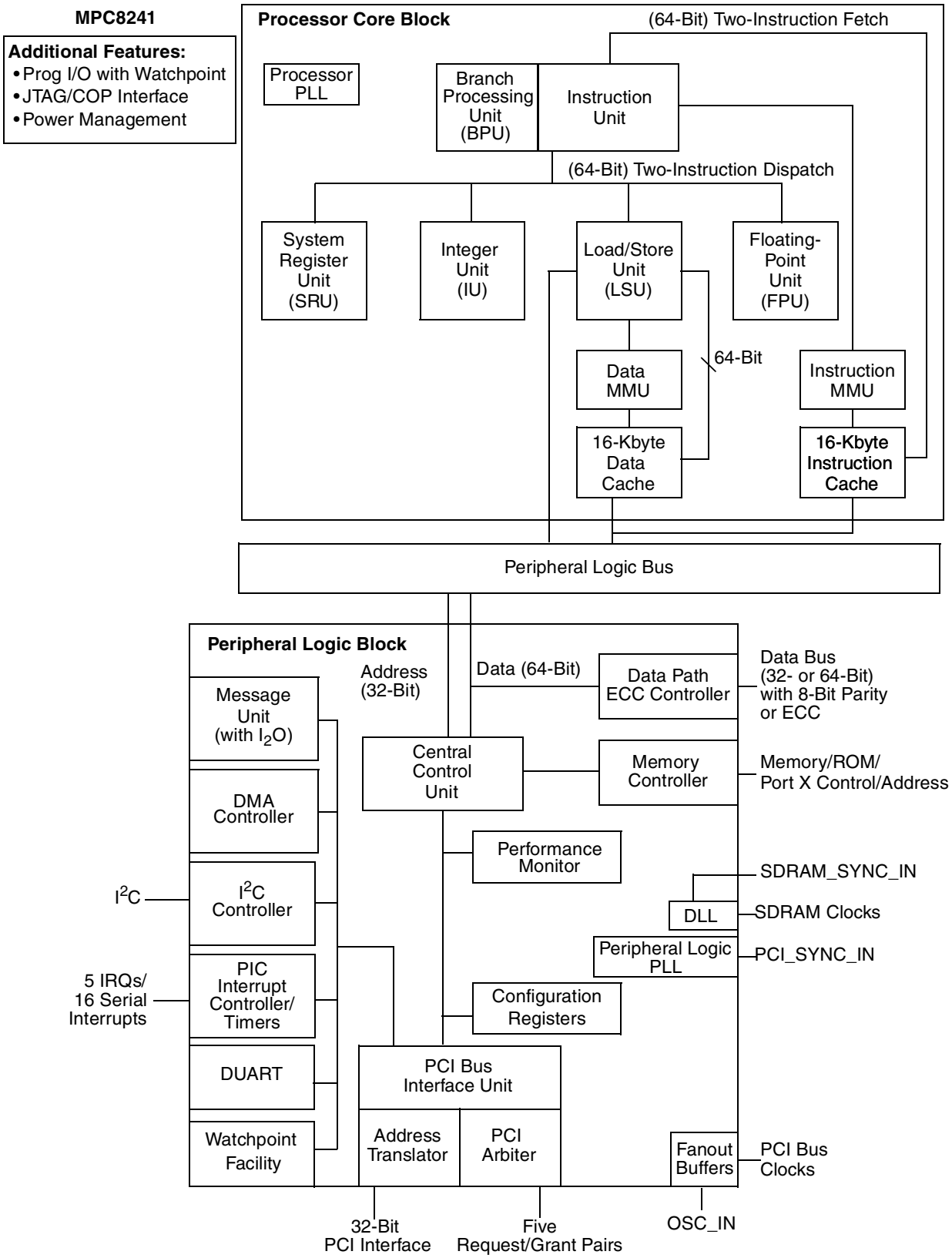


Figure 1. MPC8241 Block Diagram

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I_2O interface), and an I^2C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, 16-Kbyte instruction cache, 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

An internal peripheral logic bus interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade performance for power consumption. The processor core is clocked from a separate PLL that is referenced to the peripheral logic PLL, allowing the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8241 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The general-purpose processor core and peripheral logic serve a variety of embedded applications. The MPC8241 can be used as either a PCI host or PCI agent controller.

2 Features

Major features of the MPC8241 are as follows:

- Processor core
  - — High-performance, superscalar processor core
  - — Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and a branch processing unit (BPU)
  - — 16-Kbyte instruction cache
  - — 16-Kbyte data cache
  - — Lockable L1 caches—entire cache or on a per-way basis up to three of four ways
  - — Dynamic power management—supports 60x nap, doze, and sleep modes
- Peripheral logic
  - — Peripheral logic bus
    - – Various operating frequencies and bus divider ratios
    - – 32-bit address bus, 64-bit data bus
    - – Full memory coherency
    - – Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - – Store gathering on peripheral logic bus-to-PCI writes
  - — Memory interface
    - – Up to 2 Gbytes of SDRAM memory
    - – High-bandwidth data bus (32- or 64-bit) to SDRAM
    - – Programmable timing for SDRAM
    - – One to 8 banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices

- Write buffering for PCI and processor accesses
- Normal parity, read-modify-write (RMW), or ECC
- Data-path buffering between memory interface and processor
- Low-voltage TTL logic (LVTTL) interfaces
- 272 Mbytes of base and extended ROM/Flash/PortX space
- Base ROM space for 8-bit data path or same size as the SDRAM data path (32- or 64-bit)
- Extended ROM space for 8-, 16-, 32-bit gathering data path, 32- or 64-bit (wide) data path
- PortX: 8-, 16-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing, data ready input signal ($\overline{\text{DRDY}}$), and 4 chip selects

— 32-bit PCI interface
- Operates up to 66 MHz
- PCI 2.2-compatible
- PCI 5.0-V tolerance
- Dual address cycle (DAC) for 64-bit PCI addressing (master only)
- PCI locked accesses to memory
- Accesses to PCI memory, I/O, and configuration spaces
- Selectable big- or little endian operation
- Store gathering of processor-to-PCI write and PCI-to-memory write accesses
- Memory prefetching of PCI read accesses
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)
- PCI agent mode capability
- Address translation with two inbound and outbound units (ATU)
- Internal configuration registers accessible from PCI

— Two-channel integrated DMA controller (writes to ROM/PortX not supported)
- Direct mode or chaining mode (automatic linking of DMA transfers)
- Scatter gathering—read or write discontinuous memory
- 64-byte transfer queue per channel
- Interrupt on completed segment, chain, and error
- Local-to-local memory
- PCI-to-PCI memory
- Local-to-PCI memory
- PCI memory-to-local memory

— Message unit
- Two doorbell registers
- Two inbound and two outbound messaging registers
- I_2O message interface

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8241.

4.1 DC Electrical Characteristics

This section covers ratings, conditions, and other characteristics.

4.1.1 Absolute Maximum Ratings

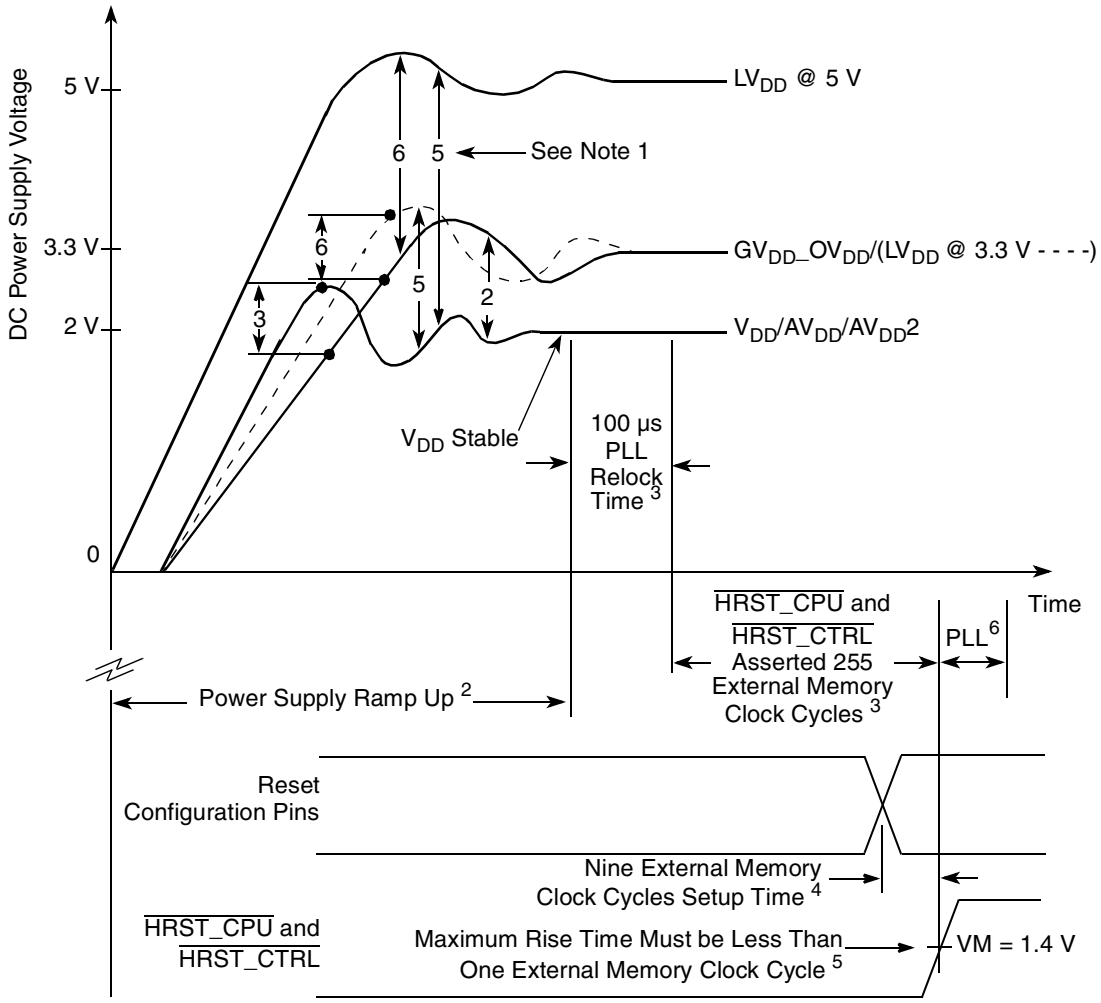
This section describes the MPC8241 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	–0.3 to 2.1	V
Supply voltage—memory bus drivers, PCI and standard I/O buffers	$GV_{DD\_}OV_{DD}$	–0.3 to 3.6	V
Supply voltage—PLLs	$AV_{DD}/AV_{DD}2$	–0.3 to 2.1	V
Supply voltage—PCI reference	LV_{DD}	–0.3 to 5.4	V
Input voltage [2]	V_{in}	–0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105	•C
Storage temperature range	T_{stg}	–55 to 150	•C

Notes:
1. Table 2 provides functional and tested operating conditions. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.

Figure 2 shows supply voltage sequencing and separation cautions.



Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. See the Cautions section of Table 2 for details on this topic.
3. Refer to Table 8 for details on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for details on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.
6. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ negate in order to be latched.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Table 7 provides the operating frequency information for the MPC8241 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V.

Table 7. Operating Frequency

Characteristic	166 MHz		200 MHz		266 MHz		Unit
	$V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 ± 100 mV						
	Min	Max	Min	Max	Min	Max	
Processor frequency (CPU)	100	166	100	200	100	266	MHz
Memory bus frequency	33	83	33	100	33	133	MHz
PCI input frequency	25–66						MHz

Caution: The PCI_SYNC_IN frequency and PLL_CFG[0:4] settings must be chosen such that the resulting peripheral logic/memory bus frequency and CPU (core) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 6, "PLL Configuration," for valid PLL_CFG[0:4] settings and PCI_SYNC_IN frequencies.

4.5.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications at recommended operating conditions, as defined in Section 4.5.2, "Input AC Timing Specifications." These specifications are for the default driver strengths indicated in Table 4. Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
1	Frequency of operation (PCI_SYNC_IN)	25	66	MHz	
2, 3	PCI_SYNC_IN rise and fall times	—	2.0	ns	1
4	PCI_SYNC_IN duty cycle measured at 1.4 V	40	60	%	
5a	PCI_SYNC_IN pulse width high measured at 1.4 V	6	9	ns	2
5b	PCI_SYNC_IN pulse width low measured at 1.4 V	6	9	ns	2
7	PCI_SYNC_IN jitter	—	200	ps	
8a	PCI_CLK[0:4] skew (pin-to-pin)	—	250	ps	
8b	SDRAM_CLK[0:3] skew (pin-to-pin)	—	190	ps	3
10	Internal PLL relock time	—	100	µs	2, 4, 5
15	DLL lock range with DLL_EXTEND = 0 (disabled) and normal tap delay; (default DLL mode)	See Figure 7		ns	6
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	

Register settings that define each DLL mode are shown in Table 9.

Table 9. DLL Mode Definition

DLL Mode	Bit 2 of Configuration Register at 0x76	Bit 7 of Configuration Register at 0x72
Normal tap delay, No DLL extend	0	0
Normal tap delay, DLL extend	0	1
Max tap delay, No DLL extend	1	0
Max tap delay, DLL extend	1	1

The DLL_MAX_DELAY bit can lengthen the amount of time through the delay line by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock is within the DLL lock range, there may be slightly more jitter in the output clock of the DLL if the phase comparator shifts the clock between adjacent tap points. Refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1*, for details on DLL modes and memory design.

The value of the current tap point after the DLL locks can be determined by reading bits 6–0 (DLL_TAP_COUNT) of the DLL tap count register (DTCR, located at offset 0xE3). These bits store the value (binary 0 through 127) of the current tap point and can indicate whether the DLL advances or decrements as it maintains the DLL lock. Therefore, for evaluation purposes, DTCR can be read for all DLL modes that support the T_{loop} value used for the trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN. The DLL mode with the smallest tap point value in the DTCR should be used because the bigger the tap point value, the more jitter that can be expected for clock signals. Keeping a DLL mode locked below tap point decimal 12 is not recommended.

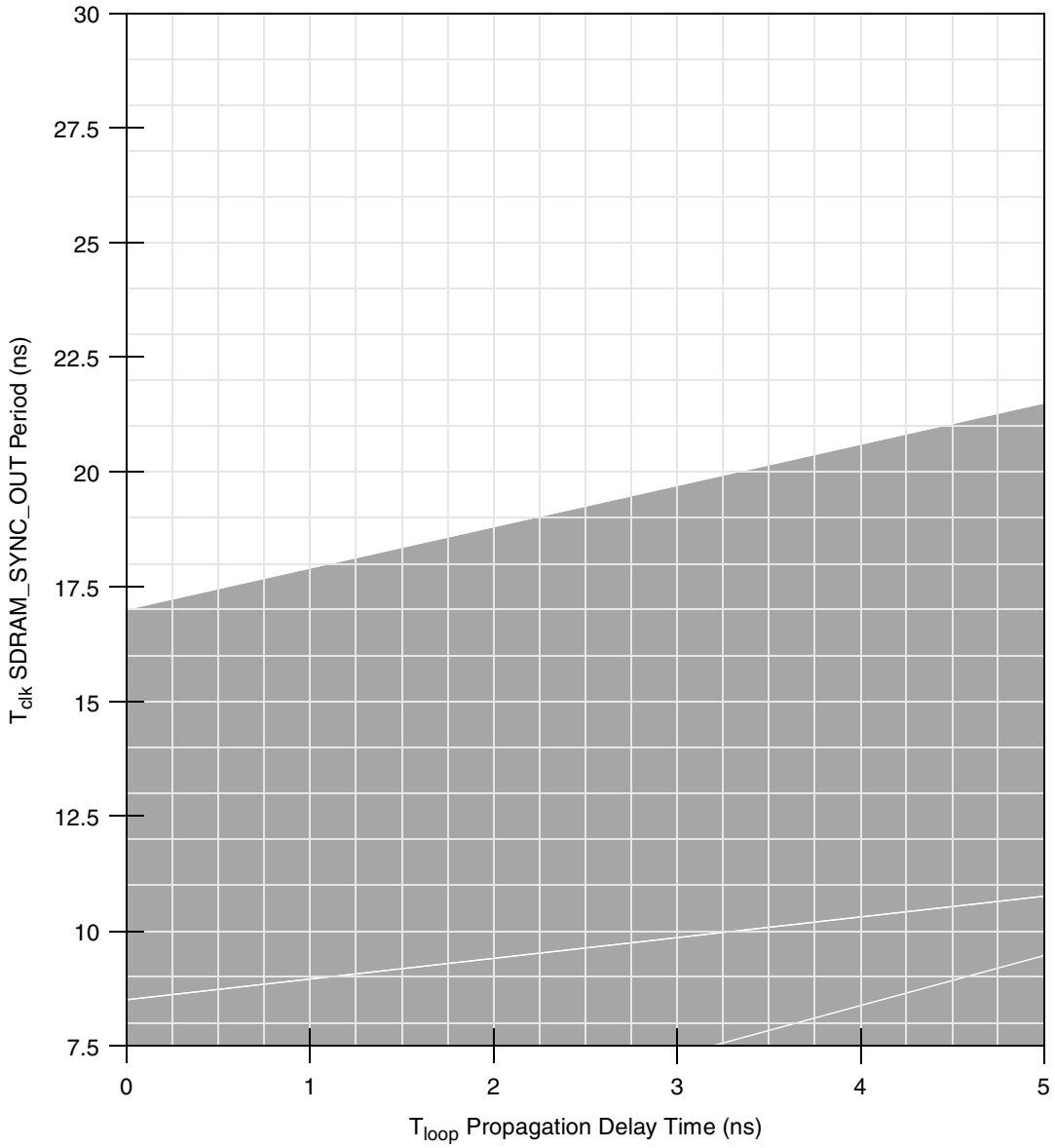


Figure 9. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=0 and Max Tap Delay

Table 10. Input AC Timing Specifications (continued)

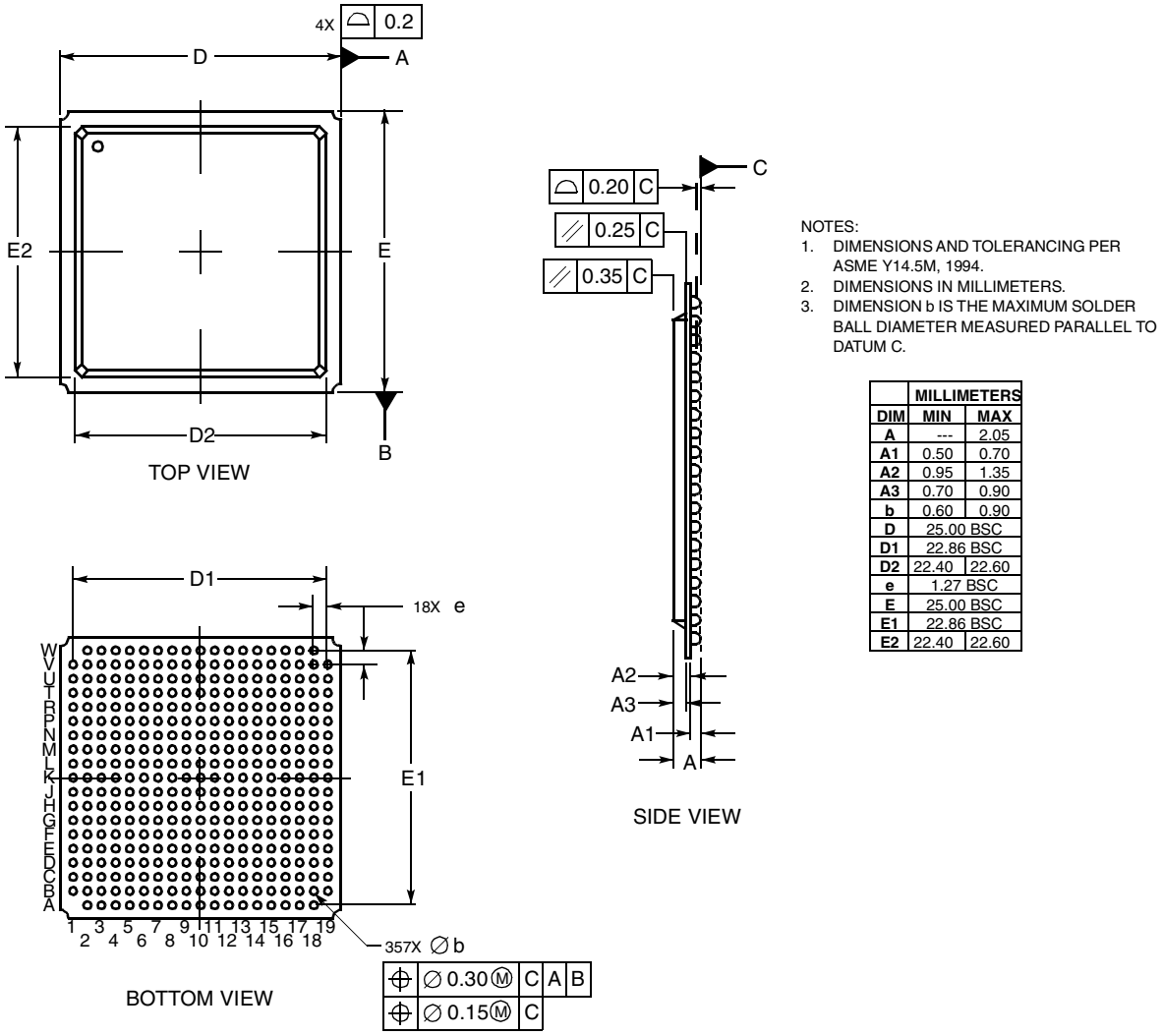
Num	Characteristic	Min	Max	Unit	Notes
10b0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	2.6	—	ns	2, 3, 6
10b1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	1.9	—		
10b2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.2	—		
10b3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	0.5	—		
10c	PIC miscellaneous debug input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10d	I^2C input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10e	Mode select inputs valid to $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ (input setup)	$9 \times t_{CLK}$	—	ns	2, 3–5
11	T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* offset time	0.4	1.0	ns	7
11a	*sys_logic_clk* to memory signal inputs invalid (input hold)				
11a0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	0	—	ns	2, 3, 6
11a1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	0.7	—		
11a2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.4	—		
11a3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	2.1	—		
11b	$\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ to mode select inputs invalid (input hold)	0	—	ns	2, 3, 5
11c	PCI_SYNC_IN to inputs invalid (input hold)	1.0	—	ns	1, 2, 3

Notes:

1. All PCI signals are measured from $GV_{DD}\_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times GV_{DD}\_OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 12.
2. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock. *sys_logic_clk*. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ signal. See Figure 13.
6. The memory interface input setup and hold times are programmable to four possible combinations by programming bits 5:4 of register offset <0x77> to select the desired input setup and hold times.
7. T_{os} represents a timing adjustment for SDRAM_SYNC_IN with respect to *sys_logic_clk*. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the *sys_logic_clk* inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. The feedback trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN must be shortened to accommodate this range relative to the SDRAM clock output trace lengths to maintain phase-alignment of the memory clocks with respect to *sys_logic_clk*. It is recommended that the length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN be shortened by 0.7 ns because that is the midpoint of the range of T_{os} and allows the impact from the range of T_{os} to be reduced. Additional analyses of trace lengths and SDRAM loading must be performed to optimize timing. For details on trace measurements and the T_{os} problem, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*.

5.2 Pin Assignments and Package Dimensions

Figure 24 shows the top surface, side profile, and pinout of the MPC8241, 357 PBGA ZP package. Note that this is available for Rev. B parts only.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.05
A1	0.50	0.70
A2	0.95	1.35
A3	0.70	0.90
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	22.40	22.60
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	22.40	22.60

Figure 24. MPC8241 Package Dimensions and Pinout Assignments (ZP Package)

Figure 25 shows the top surface, side profile, and pinout of the MPC8241, 357 PBGA ZQ and VR packages.

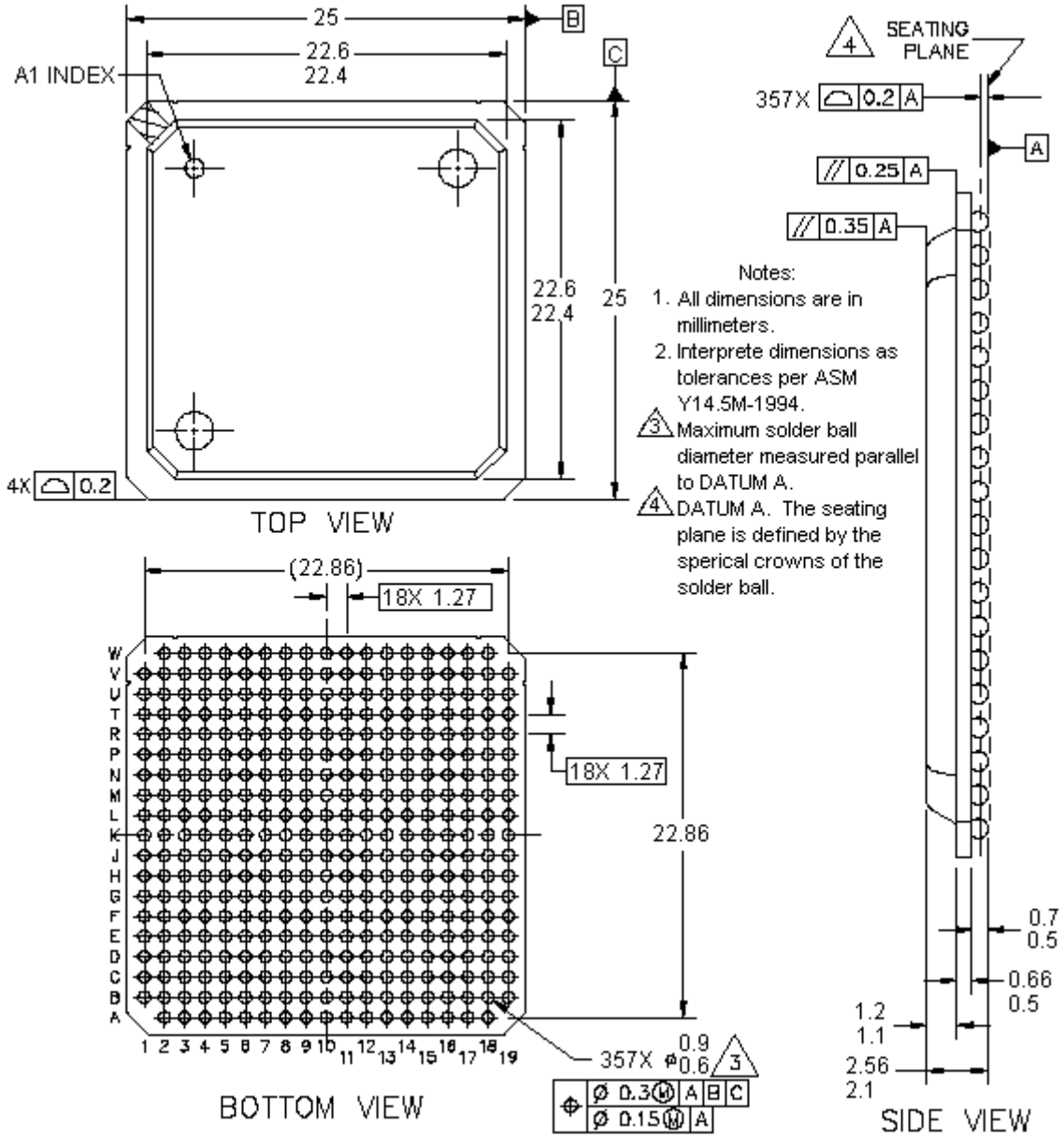


Figure 25. MPC8241 Package Dimensions and Pinout Assignments (ZQ and VR Packages)

5.3 Pinout Listings

Table 16 provides the pinout listing for the MPC8241, 357 PBGA package.

Table 16. MPC8241 Pinout Listing

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
$\overline{\text{C/BE}}$[3:0]	V11 V7 W3 R3	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 2
$\overline{\text{DEVSEL}}$	U6	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{FRAME}}$	T8	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{IRDY}}$	U7	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{LOCK}}$	V6	Input	$GV_{DD}\_OV_{DD}$	—	3
AD[31:0]	U13 V13 U11 W14 V14 U12 W10 T10 V10 U9 V9 W9 W8 T9 W7 V8 V4 W4 V3 V2 T5 R6 V1 T2 U3 P3 T4 R1 T3 R4 U2 U1	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 2
PAR	R7	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2
$\overline{\text{GNT}}$[3:0]	W15 U15 W17 V12	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 2
$\overline{\text{GNT4}}$/DA5	T11	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 4, 5
$\overline{\text{REQ}}$[3:0]	V16 U14 T15 V15	Input	$GV_{DD}\_OV_{DD}$	—	1, 6
$\overline{\text{REQ4}}$/DA4	W13	I/O	$GV_{DD}\_OV_{DD}$	—	5, 6
$\overline{\text{PERR}}$	T7	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3, 7
$\overline{\text{SERR}}$	U5	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3, 8
$\overline{\text{STOP}}$	W5	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{TRDY}}$	W6	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{INTA}}$	T12	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 8
IDSEL	U10	Input	$GV_{DD}\_OV_{DD}$	—	—
Memory Interface Signals					
MDL[0:31]	M19 M17 L16 L17 K18 J18 K17 K16 J15 J17 H18 F16 H16 H15 G17 D19 B3 C4 C2 D3 G5 E1 H5 E2 F1 F2 G2 J5 H1 H4 J4 J1	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1, 9
MDH[0:31]	M18 L18 L15 K19 K15 J19 J16 H17 G19 G18 G16 D18 F18 E18 G15 E15 C3 D4 E5 F5 D1 E4 D2 E3 F4 G3 G4 G1 H2 J3 J2 K5	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1
DQM[0:7]	A18 B18 A6 C7 D15 D14 A9 B8	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1
$\overline{\text{CS}}$[0:7]	A17 B17 C16 C17 C9 C8 A10 B10	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1
FOE	A7	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{\text{RCS0}}$	C10	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
$\overline{\text{RCS1}}$	B9	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
$\overline{\text{RCS2}}$/TRIG_IN	P18	I/O	$GV_{DD}\_OV_{DD}$	—	5, 12
$\overline{\text{RCS3}}$/TRIG_OUT	N18	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	5
SDMA[1:0]	A15 B15	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1, 10, 11
SDMA[11:2]	A11 B12 A12 C12 B13 C13 D12 A14 C14 B14	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1
$\overline{\text{DRDY}}$	P1	Input	$GV_{DD}\_OV_{DD}$	—	12, 13
SDMA12/$\overline{\text{SRESET}}$	L3	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA13/TBEN	K3	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA14/$\overline{\text{CHKSTOP\_IN}}$	K2	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDBA1	C11	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
SDBA0	B11	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
PAR[0:7]	E19 C19 D5 D6 E16 F17 B2 C1	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1
$\overline{\text{SDRAS}}$	B19	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10
$\overline{\text{SDCAS}}$	D16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10
CKE	C6	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{\text{WE}}$	B16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	—
$\overline{\text{AS}}$	A16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
PIC Control Signals					
IRQ0/S_INT	P4	Input	$GV_{DD}\_OV_{DD}$	—	—
IRQ1/S_CLK	R2	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
IRQ2/S_RST	U19	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
IRQ3/$\overline{\text{S\_FRAME}}$	P15	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
IRQ4/$\overline{\text{L\_INT}}$	P2	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	—
I^2C Control Signals					
SDA	P17	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	8, 12
SCL	R19	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	8, 12
DUART Control Signals					
SOUT1/PCI_CLK0	T16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14
SIN1/PCI_CLK1	U16	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14, 24
SOUT2/$\overline{\text{RTS1}}$/PCI_CLK2	W18	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14
SIN2/$\overline{\text{CTS1}}$/PCI_CLK3	V19	I	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 14, 24
Clock-Out Signals					
PCI_CLK0/SOUT1	T16	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI_CLK	5, 14

6 PLL Configuration

The PLL_CFG[0:4] are configured by the internal PLLs. For a specific PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations are shown in Table 17 and Table 18.

Table 17. PLL Configurations (166- and 200-MHz)

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	Not available			25-26[5]	75-78	188-195	3 (2)	2.5 (2)
2	00010	34[4]–37[5]	34–37	153–166	34[4]–44[5]	34–44	153–200	1 (4)	4.5 (2)
3	00011[6]	50[7]–66[3]	50–66	100–132	50[7]–66[3]	50–66	100–132	1 (Bypass)	2 (4)
4	00100	25–41[5]	50–82	100–164	25–44[8,10]	50–88	100–176	2 (4)	2 (4)
6	00110[9]	Bypass			Bypass			Bypass	Bypass
7 Rev. B	00111[6]	50[4]–55 [5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (Bypass)	3 (2)
7 Rev. D	00111	Not available							
8	01000	50[4]–55[5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (4)	3 (2)
9	01001	38[4]–41[5,11]	76–82	152–164	38[4]–50[5,12]	76–100	152–200	2 (2)	2 (2)
B	01011	Not available			44[5]	66	198	2(2)	2.5(2)
C	01100	30[4]–33[5]	60–66	150–165	30[4]–40[5]	60–80	150–200	2 (4)	2.5 (2)
E	01110	25–27[5]	50–54	150–162	25–33[5]	60–66	150–198	2 (4)	3 (2)
10	10000	25–27[5,11]	75–83	150–166	25–33[5,12]	75–100	150–200	3 (2)	2 (2)
12	10010	50[4]–55[5,11]	75–83	150–166	50[4]–66[3]	75–99	150–198	1.5 (2)	2 (2)
14	10100	Not available			25–28[5]	50–56	175–196	2 (4)	3.5 (2)
16	10110				25[5]	50	200	2(4)	4(2)
17	10111				25[5]	100	200	4(2)	2(2)
19	11001	33[5,13]	66	165	33[13]–40[5]	66–80	165–200	2(2)	2.5(2)
1A	11010	37[4]–41[5]	37–41	150–166	37[4]–50[5]	37–50	150–200	1 (4)	4 (2)
1B	11011	Not available			33[5,13]	66	198	2(2)	3(2)
1C	11100				44[5,13]	66	198	1.5(2)	3(2)
1D	11101	44[5,13]	66	166	44[13]–53[5]	66–80	165–200	1.5 (2)	2.5 (2)

Table 18. PLL Configurations (266-MHz Parts) (continued)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Off	Off

Notes:

1. Limited by maximum PCI input frequency (66 MHz).
2. Note the impact of the relevant revisions for modes 7 and 1E.
3. Limited by minimum memory VCO frequency (132 MHz).
4. Limited due to maximum memory VCO frequency (352 MHz).
5. Limited by maximum CPU operating frequency.
6. Limited by minimum CPU VCO frequency (300 MHz).
7. Limited by maximum CPU VCO frequency (704 MHz).
8. In clock off mode, no clocking occurs inside the MPC8241, regardless of the PCI_SYNC_IN input.
9. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
10. PLL_CFG[0:4] settings that are not listed are reserved.
11. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
12. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
13. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
14. Limited by minimum CPU operating frequency (100 MHz).
15. Limited by minimum memory bus frequency (50 MHz).

7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8241.

7.1 PLL Power Supply Filtering

The AV_{DD} and $AV_{DD}2$ power signals on the MPC8241 provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and $AV_{DD}2$ input signals should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 26 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD} and $AV_{DD}2$ power signal pins. In *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), Dr. Howard Johnson recommends using multiple small capacitors of equal value instead of multiple values.

7.7 Thermal Management

This section provides thermal management information for the plastic ball grid array (PBGA) package for air-cooled applications. Depending on the application environment and the operating frequency, a heat sink may be required to maintain junction temperature within specifications. Proper thermal control design primarily depends on the system-level design: heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks can be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, or mounting clip and screw assembly (see Figure 28).

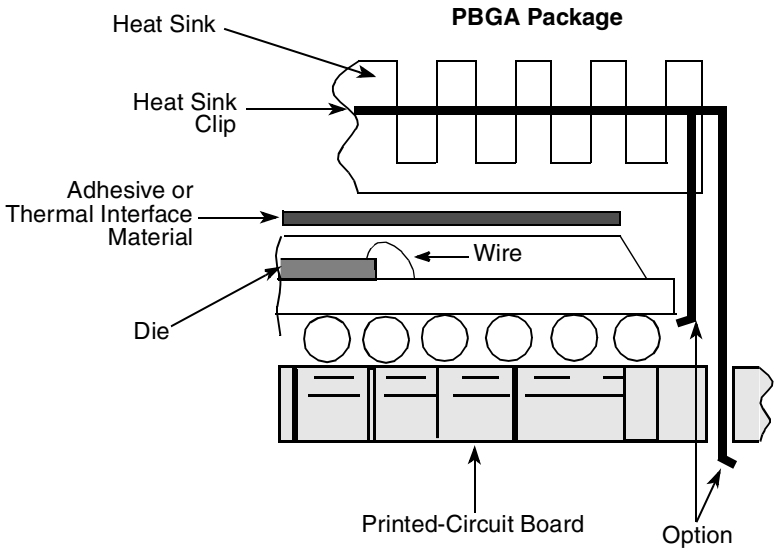


Figure 28. Package Exploded Cross-Sectional View with Several Heat Sink Options

Figure 29 depicts the die junction-to-ambient thermal resistance for four typical cases:

- A heat sink is not attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s).
- A heat sink is not attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s/sink).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p/sink).

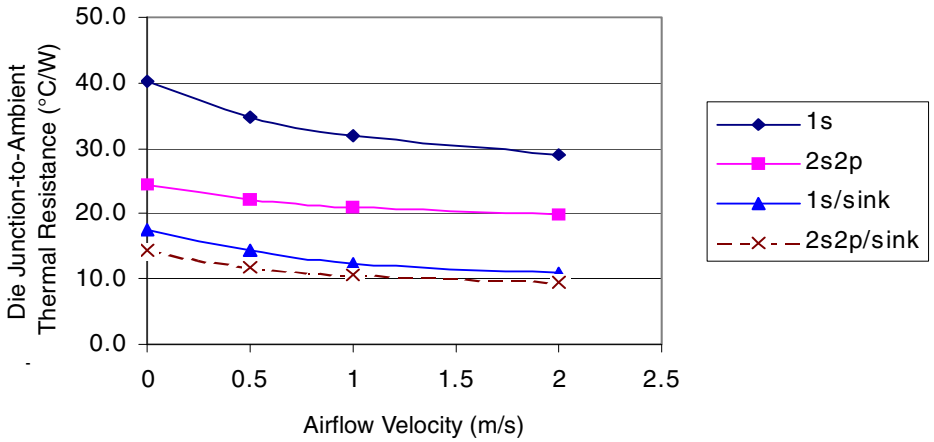


Figure 29. Die Junction-to-Ambient Resistance

The board designer can choose among several types of heat sinks to place on the MPC8241. Several commercially available heat sinks for the MPC8241 are provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

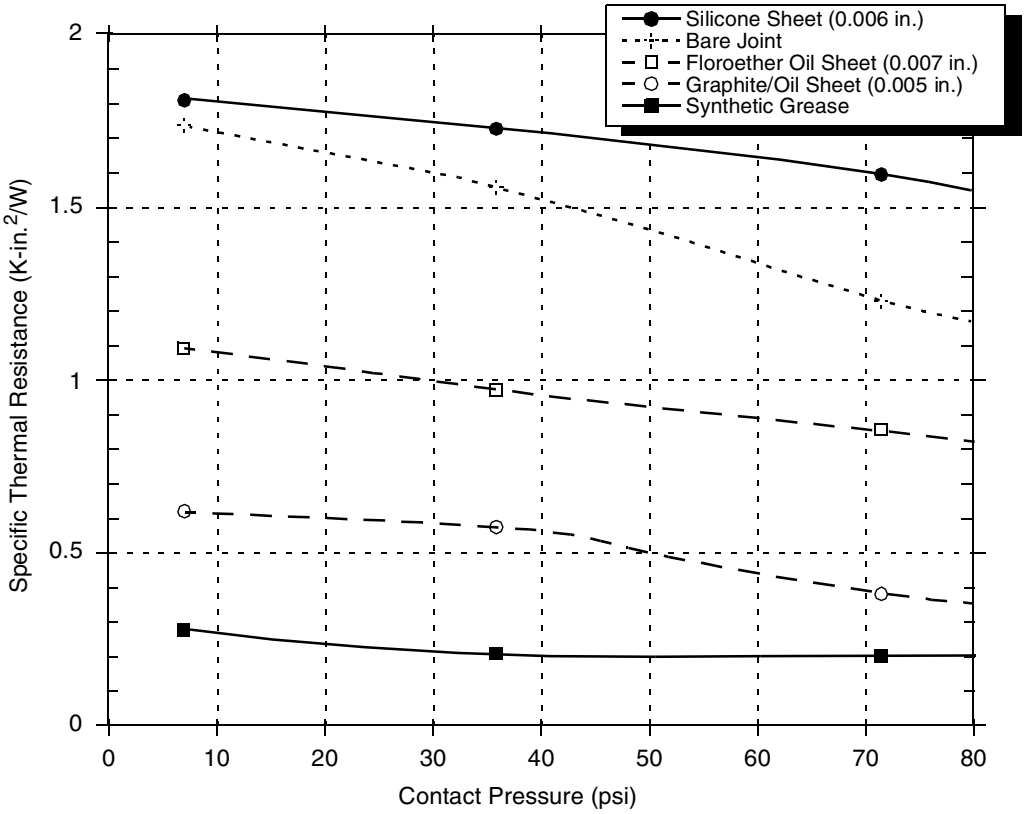


Figure 31. Thermal Performance of Select Thermal Interface Material

The board designer can choose among several types of thermal interface. Heat sink adhesive materials are selected on the basis of high conductivity and adequate mechanical strength to meet equipment shock/vibration requirements. Several commercially-available thermal interfaces and adhesive materials are provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

7.7.3 Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (ψ_{JT}) measures the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\psi_{JT} \times P_D)$$

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
1	—	Updated document template. Section 1.4.1.5—Updated driver type names in Table 4 so that they are consistent with the driver types referred to in the *MPC8245 Integrated Processor Reference Manual*. Added notes 5 and 6 to Table 4. Section 1.4.3.1—Added reference to AN2164 in note 7. Labeled N value in Figures 5 through 8. Section 1.4.3.2—Updated Figure 9 to show T_{os}. Table 9—Changed default for 0x77 bits 5:4 to 0b10. Section 1.4.3.3—Added item 12e to Table 10 for SDRAM_SYNC_IN to Output Valid Timing. Updated Figure 13 to state GV_{DD}_OV_{DD} instead of OV_{DD}. Section 1.5.3—Updated driver type names to match those used in Table 4. Updated notes for the following signals: $\overline{\text{DRDY}}$, SDRAM_CLK[0:3], $\overline{\text{MIV}}$, RTC, TDO, and DA[11]. Section 1.6—Updated PLL table and notes. Removed old Section 1.7.2 on voltage sequencing requirements. Added cautions regarding voltage sequencing to the end of Table 2 in Section 1.4.1.2. Section 1.7.3—Changed sentence recommendation regarding decoupling capacitors. Section 1.7.5—Added reference to AN2164. Section 1.7.6—Added sentence regarding the PLL_CFG signals. Removed old Section 1.7.8 since the MPC8241 cannot be used as a drop in replacement for the MPC8240 because of pin compatibility issues. Section 1.7.8—Updated $\overline{\text{TRST}}$ information in this section and Figure 26. Section 1.7.9—Updated list for heat sink and thermal interface vendors. Section 1.9—Changed format of ordering information section. Added tables to reflect part number specifications also available. Added Sections 1.9.2 and 1.9.3.
0.3	—	Corrected solder ball information in Section 1.5.1 to 62 Sn/36 Pb/2 Ag. Section 1.4.3.1—Corrected DLL_EXTEND labeling in Figures 5 through 8. Removed note for pin TRIG_OUT/RCS3 in Table 16, as well as from the list of pins needing to be pulled up to IV_{DD} in Section 1.7.6. Corrected order information labeling in Section 1.9 to MPC8241XZPXXXX. Also corrected label description of ZU = PBGA to ZP = PBGA.
0.2	—	Table 16—Corrected pin number for PLL_CFG0/DA10 to N3. The pin was already correctly listed for DA10/PLL_CFG0. Updated note 1 to reflect pin assignments for the MPC8241. Updated footnotes throughout document. Section 1.4.3.3—Updated note 4 to correct bit values of PCI_HOLD_DEL in PMCR2. Section 1.6—Updated notes in Table 17. Included memory VCO minimum and maximum numbers. Section 1.7.8—Updated description of bits PCI_HOLD_DEL in PMCR2. Section 1.7.10.3—Replaced thermal characterization parameter (YJT) with correct thermal characterization parameter (Ψ_{JT}). Changed Ψ_{π} symbol to Ψ_{JT}.
0.1	—	Updated Features list in Section 1.2. Corrected pin assignments in Table 16 for DA[15] and DQM[3] signals. Added vendor (Cool Innovations, Inc.) to list of heat sink vendors.
0	—	Initial release.