Renesas Electronics America Inc - UPD78F1152AGK-GAK-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1152agk-gak-ax

(2/2)

Item		μPD78F1152, μPD78F1152A	μPD78F1153, μPD78F1153A	μPD78F1154, μPD78F1154A	μPD78F1155, μPD78F1155A	μPD78F1156, μPD78F1156A
Serial interface		• UART supporting LIN-bus: 1 channel • CSI: 2 channels/UART: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • I^2C bus: 1 channel				
Multiplier		16 bits × 16 bits = 32 bits				
DMA controller		2 channels				
Vectored interrupt sources	Internal	28				
	External	13				
Key interrupt		Key interrupt (INTKR) occurs by detecting falling edge of the key input pins (KR0 to KR7).				
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector • Internal reset by illegal instruction execution[Note]				
On-chip debug function		Provided				
Power supply voltage		V_{DD} = 1.8 to 5.5 V				
Operating ambient temperature		T_A = −40 to +85°C				
Package		80-pin plastic LQFP (14 × 14) (0.65 mm pitch) 80-pin plastic LQFP (fine pitch) (12 × 12) (0.5 mm pitch)				

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Caution To use P02/SO10/TxD1 and P04/$\overline{\text{SCK10}}$/SCL10 as general-purpose ports, set serial communication operation setting register 02 (SCR02) to the default status (0087H). In addition, clear port output mode register 0 (POM0) to 00H.

2.2.2 P10 to P17 (port 1)

P10 to P17 function as an 8-bit I/O port. These pins also function as external interrupt request input, serial interface data I/O, clock I/O, timer I/O, and real-time counter clock output.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an 8-bit I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

(2) Control mode

P10 to P17 function as external interrupt request input, serial interface data I/O, clock I/O, timer I/O, and real-time counter clock output.

(a) SI00

This is a serial data input pin of serial interface CSI00.

(b) SO00

This is a serial data output pin of serial interface CSI00.

(c) $\overline{\text{SCK00}}$

This is a serial clock I/O pin of serial interface CSI00.

(d) RxD0

This is a serial data input pin of serial interface UART0.

(e) RxD3

This is a serial data input pin of serial interface UART3.

(f) TxD0

This is a serial data output pin of serial interface UART0.

(g) TxD3

This is a serial data output pin of serial interface UART3.

(h) TI01, TI02

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 01 and 02.

2.2.19 V_{DD}, EV_{DD}

V_{DD} is the positive power supply pin for P121 to P124 and pins other than ports (excluding the $\overline{\text{RESET}}$ and FLMD0 pins).

EV_{DD} is the positive power supply pin for ports other than P20 to P27, P110, P111 and P121 to P124 as well as for the $\overline{\text{RESET}}$ and FLMD0 pins.

2.2.20 V_{SS}, EV_{SS}

V_{SS} is the ground potential pin for P121 to P124 and pins other than ports (excluding the $\overline{\text{RESET}}$ and FLMD0 pins).

EV_{SS} is the ground potential pin for ports other than P20 to P27, P110, P111 and P121 to P124 as well as for the $\overline{\text{RESET}}$ and FLMD0 pins.

2.2.21 FLMD0

This is a pin for setting flash memory programming mode.

Perform either of the following processing.

(a) In normal operation mode

It is recommended to leave this pin open during normal operation.

The FLMD0 pin must always be kept at the V_{SS} level before reset release but does not have to be pulled down externally because it is internally pulled down by reset. However, pulling it down must be kept selected (i.e., FLMDPUP = “0”, default value) by using bit 7 (FLMDPUP) of the background event control register (BECTL) (see **24.5 (1) Back ground event control register**). To pull it down externally, use a resistor of 200 kΩ or smaller.

Self programming and the rewriting of flash memory with the programmer can be prohibited using hardware, by directly connecting this pin to the V_{SS} pin.

(b) In self programming mode

It is recommended to leave this pin open when using the self programming function. To pull it down externally, use a resistor of 100 kΩ to 200 kΩ.

In the self programming mode, the setting is switched to pull up in the self programming library.

(c) In flash memory programming mode

Directly connect this pin to a flash memory programmer when data is written by the flash memory programmer. This supplies a writing voltage of the V_{DD} level to the FLMD0 pin.

The FLMD0 pin does not have to be pulled down externally because it is internally pulled down by reset. To pull it down externally, use a resistor of 1 kΩ to 200 kΩ.

3.1.1 Internal program memory space

The internal program memory space stores the program and table data. Normally, it is addressed with the program counter (PC).

78K0R/KF3 products incorporate internal ROM (flash memory), as shown below.

Table 3-2. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
μPD78F1152, 78F1152A	Flash memory	65536 × 8 bits (00000H to 0FFFFH)
μPD78F1153, 78F1153A		98304 × 8 bits (00000H to 17FFFH)
μPD78F1154, 78F1154A		131072 × 8 bits (00000H to 1FFFFH)
μPD78F1155, 78F1155A		196608 × 8 bits (00000H to 2FFFFH)
μPD78F1156, 78F1156A		262144 × 8 bits (00000H to 3FFFFH)

The internal program memory space is divided into the following areas.

(1) Vector table area

The 128-byte area 00000H to 0007FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area. Furthermore, the interrupt jump address is a 64 K address of 00000H to 0FFFFH, because the vector code is assumed to be 2 bytes.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

<R> **Figure 3-8. Correspondence Between Data Memory and Addressing (μPD78F1153, 78F1153A)**

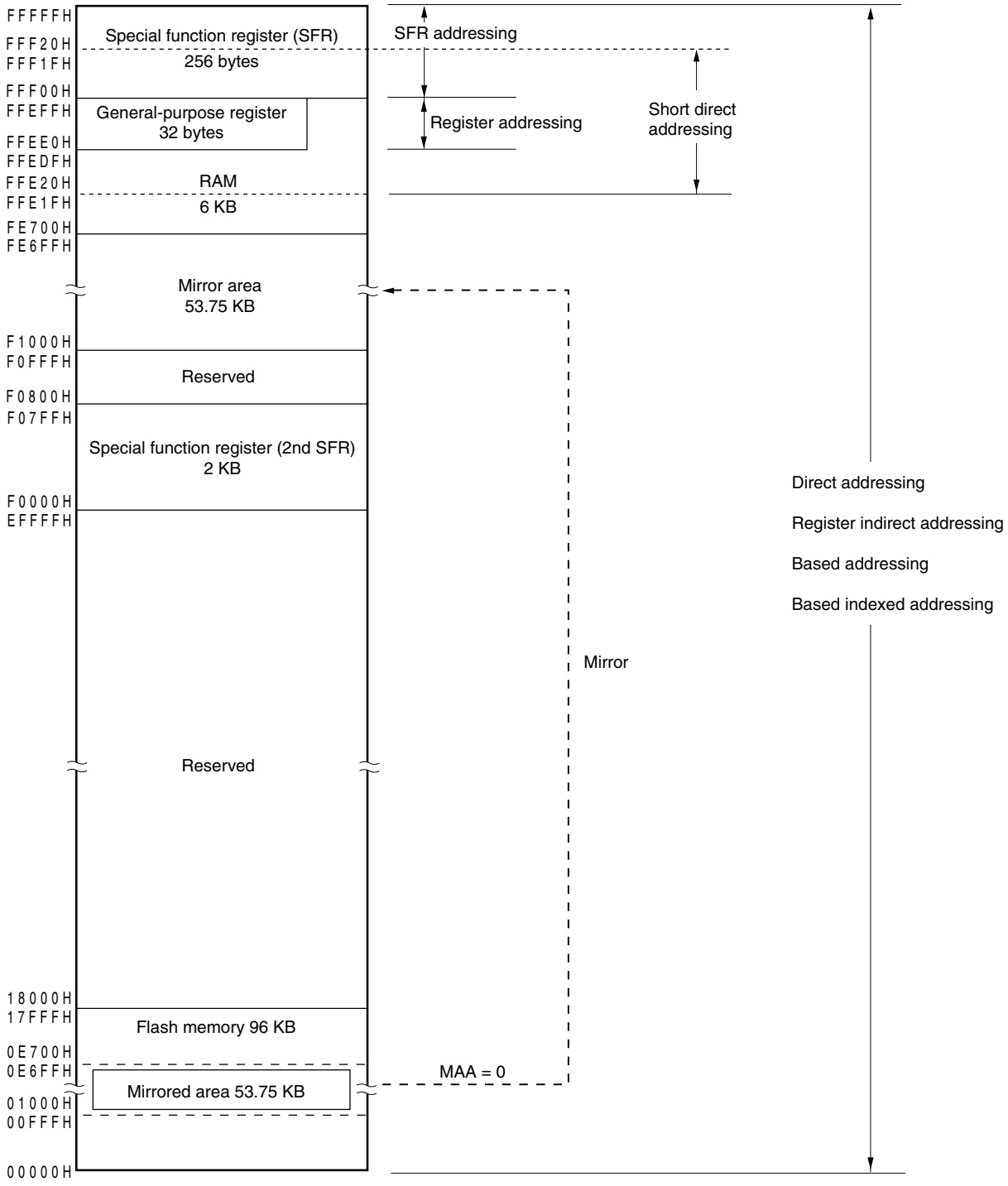
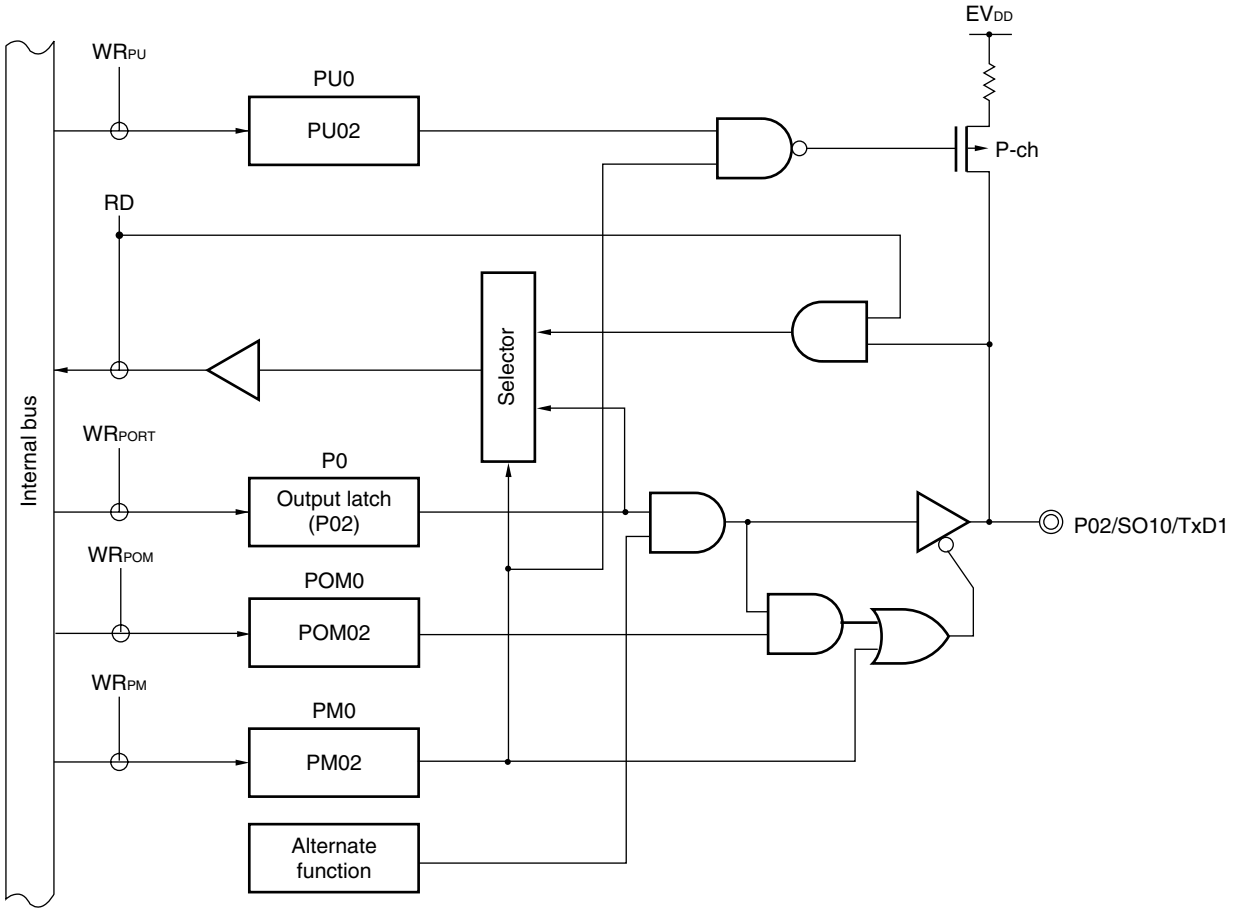


Figure 4-4. Block Diagram of P02



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
POM0: Port output mode register 0
RD: Read signal
WR××: Write signal

(e) Start timing in capture & one-count mode

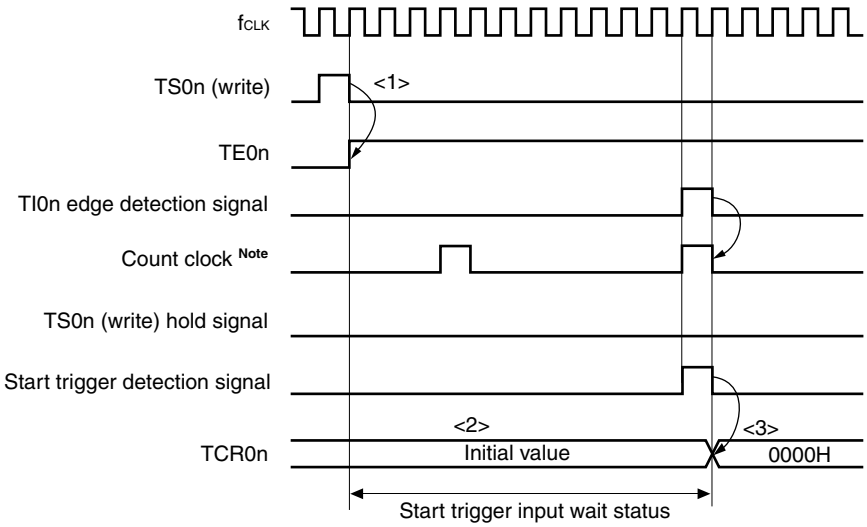
<1> Writing 1 to TS0n sets TE0n = 1

<2> Enters the start trigger input wait status, and TCR0n holds the initial value.

<3> On start trigger detection, 0000H is loaded to TCR0n and count starts.

Figure 6-14. Start Timing (In Capture & One-count Mode)

<R>



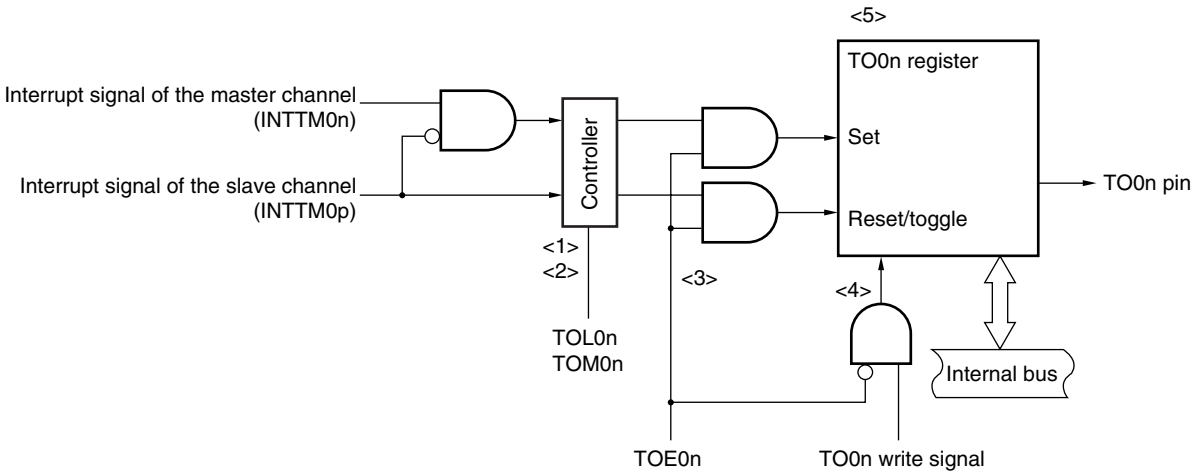
Note When the capture & one-count mode is set, the operation clock (MCK) is selected as count clock (CCS0n = 0).

Caution An input signal sampling error is generated since operation starts upon start trigger detection (The error is one count clock when TI0n is used).

6.4 Channel Output (TO0n pin) Control

6.4.1 TO0n pin output circuit configuration

Figure 6-24. Output Circuit Configuration



The following describes the TO0n pin output circuit.

<1> When TOM0n = 0 (toggle mode), the set value of the TOL0n register is ignored and only INTTM0p (slave channel timer interrupt) is transmitted to the TO0n register.

<2> When TOM0n = 1 (combination-operation mode), both INTTM0n (master channel timer interrupt) and INTTM0p (slave channel timer interrupt) are transmitted to the TO0n register.
At this time, the TOL0n register becomes valid and the signals are controlled as follows:

When TOL0n = 0: Forward operation (INTTM0 → set, INTTM0p → reset)
When TOL0n = 1: Reverse operation (INTTM0 → reset, INTTM0p → set)

When INTTM0n and INTTM0p are simultaneously generated, (0% output of PWM), INTTM0p (reset signal) takes priority, and INTTM0n (set signal) is masked.

<3> When TOE0n = 1, INTTM0n (master channel timer interrupt) and INTTM0p (slave channel timer interrupt) are transmitted to the TO0n register. Writing to the TO0n register (TO0n write signal) becomes invalid.
When TOE0n = 1, the TO0n pin output never changes with signals other than interrupt signals.
To initialize the TO0n pin output level, it is necessary to set TOE0n = 0 and to write a value to TO0n.

<4> When TOE0n = 0, writing to TO0n bit to the target channel (TO0n write signal) becomes valid. When TOE0n = 0, neither INTTM0n (master channel timer interrupt) nor INTTM0p (slave channel timer interrupt) is transmitted to TO0n register.

<5> The TO0n register can always be read, and the TO0n pin output level can be checked.

Remarks 1. n = 0 to 7 (n = 0, 2, 4, or 6 for master channel)

2. p = n + 1, n + 2, n + 3 ... (where p ≤ 7)

Figure 7-4. Format of Real-Time Counter Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag
0	Constant-period interrupt is not generated.
1	Constant-period interrupt is generated.
This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

RWST	Wait status flag of real-time counter
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of RWAIT is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.	

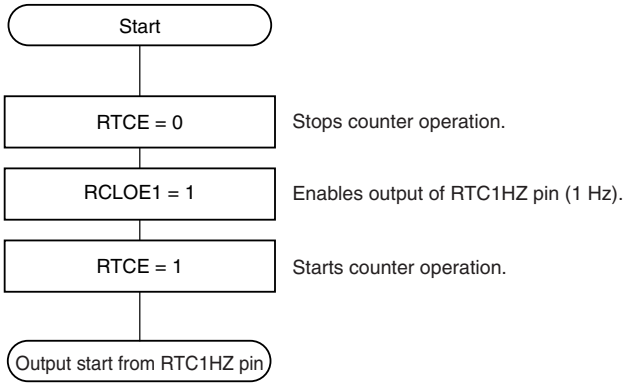
RWAIT	Wait control of real-time counter
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write “1” to it to read or write the counter value. Because RSUBC continues operation, complete reading or writing of it in 1 second, and clear this bit back to 0. When RWAIT = 1, it takes up to 1 clock (32.768 kHz) until the counter value can be read or written. If RSUBC overflows when RWAIT = 1, it counts up after RWAIT = 0. If the second count register is written, however, it does not count up because RSUBC is cleared.	

Caution The RIFG and WAFG flags may be cleared when the RTCC1 register is written by using a 1-bit manipulation instruction. Use, therefore, an 8-bit manipulation instruction in order to write to the RTCC1 register. To prevent the RIFG and WAFG flags from being cleared during writing, disable writing by setting “1” to the corresponding bit. When the value may be rewritten because the RIFG and WAFG flags are not being used, the RTCC1 register may be written by using a 1-bit manipulation instruction.

Remark Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

7.4.5 1 Hz output of real-time counter

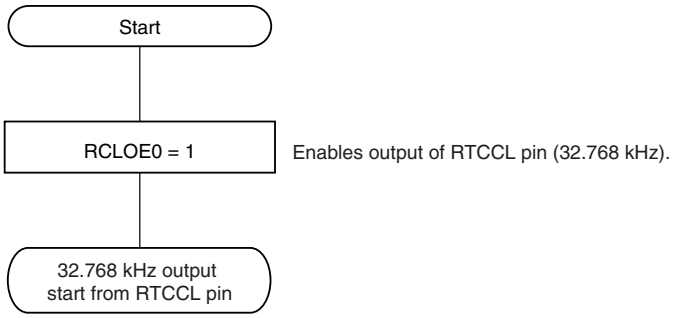
Figure 7-24. 1 Hz Output Setting Procedure



<R> **Caution First set RTCEN to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.**

<R> ### 7.4.6 32.768 kHz output of real-time counter

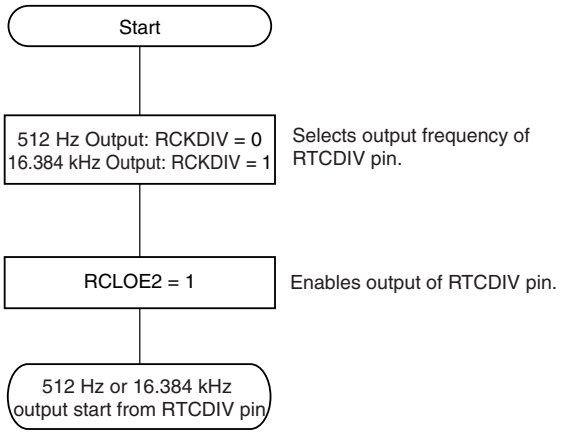
Figure 7-25. 32.768 kHz Output Setting Procedure



Caution First set RTCEN to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.

<R> ### 7.4.7 512 Hz, 16.384 kHz output of real-time counter

Figure 7-26. 512 Hz, 16.384 kHz output Setting Procedure



Caution First set RTCEN to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.

(12) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 10-28. Internal Equivalent Circuit of ANIn Pin

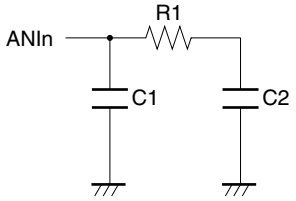


Table 10-6. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{REF0}	R1	C1	C2
4.0 V ≤ V_{DD} ≤ 5.5 V	8.1 kΩ	8 pF	5 pF
2.7 V ≤ V_{DD} < 4.0 V	31 kΩ	8 pF	5 pF
2.3 V ≤ V_{DD} < 2.7 V	381 kΩ	8 pF	5 pF

Remarks 1. The resistance and capacitance values shown in Table 10-6 are not guaranteed values.

2. n = 0 to 7

<R> **(13) Starting the A/D converter**

Start the A/D converter after the AV_{REF0} and AV_{REF1} voltages (the reference voltages for the D/A converter) stabilize.

11.4.3 Cautions

Observe the following cautions when using the D/A converter of the 78K0R/KF3.

(1) The digital port I/O function, which is the alternate function of the ANO0 and ANO1 pins, does not operate during D/A conversion.

<R> During D/A conversion, 0 is read from the P11 register in input mode.

(2) Do not read/write the P11 register and do not change the setting of the PM11 register during D/A conversion (otherwise the conversion accuracy may decrease).

(3) It is recommended that both the ANO0 and ANO1 pins be used as analog output pins or digital I/O pins, that is, use these two channels for the same application (if these pins are used for the different applications, the conversion accuracy may decrease).

(4) In the real-time output mode, set the DACSn register value before the timer trigger is generated. In addition, do not change the set value of the DACSn register while the trigger signal is output.

(5) Before changing the operation mode, be sure to clear the DACEn bit of the DAM register to 0 (D/A conversion stop).

(6) When using the port that functions alternately as the ANO0 or ANO1 pin, use it as the port input with few level changes.

<R> (7) Stop the conversion performed by the D/A converter when supplying AV_{REF1} or AV_{REF0} (the reference voltages for the A/D converter) starts or stops.

(8) Because the D/A converter stops operation in the STOP mode, the ANO0 and ANO1 pins go into a high-impedance state, and the power consumption can be reduced.
In the standby modes other than the STOP mode, however, the operation continues. To lower the power consumption, therefore, clear the DACEn bit of the DAM register to 0 (D/A conversion stop).

(9) Since the output impedance of the D/A converter is high, the current cannot be obtained from the ANOn pin (n = 0, 1). When the input impedance of the load is low, insert a follower amplifier between the load and ANOn pin keeping the wiring length as short as possible (for high impedance). If the wiring becomes too long, take necessary actions such as surrounding with a ground pattern.

(1) Peripheral enable register 0 (PER0)

PER0 is used to enable or disable use of each peripheral hardware macro. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When serial array unit 0 is used, be sure to set bit 2 (SAU0EN) of this register to 1.

When serial array unit 1 is used, be sure to set bit 3 (SAU1EN) of this register to 1.

PER0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12-4. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCEN	DACEN	ADCEN	IIC0EN	SAU1EN	SAU0EN	0	TAU0EN

SAUmEN	Control of serial array unit m input clock
0	Stops supply of input clock. • SFR used by serial array unit m cannot be written. • Serial array unit m is in the reset status.
1	Supplies input clock. • SFR used by serial array unit m can be read/written.

Cautions 1. When setting serial array unit m, be sure to set SAUmEN to 1 first. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read (except for input switch control register (ISC), noise filter enable register (NFEN0), port input mode registers (PIM0, PIM4, PIM14), port output mode registers (POM0, POM4, POM14), port mode registers (PM0, PM1, PM4, PM14), and port registers (P0, P1, P4, P14)).

2. After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

3. Be sure to clear bit 1 of PER0 register to 0.

Remark m: Unit number (m = 0, 1)

(2) Serial clock select register m (SPSm)

SPSm is a 16-bit register that is used to select two types of operation clocks (CKm0, CKm1) that are commonly supplied to each channel. CKm1 is selected by bits 7 to 4 of SPSm, and CKm0 is selected by bits 3 to 0.

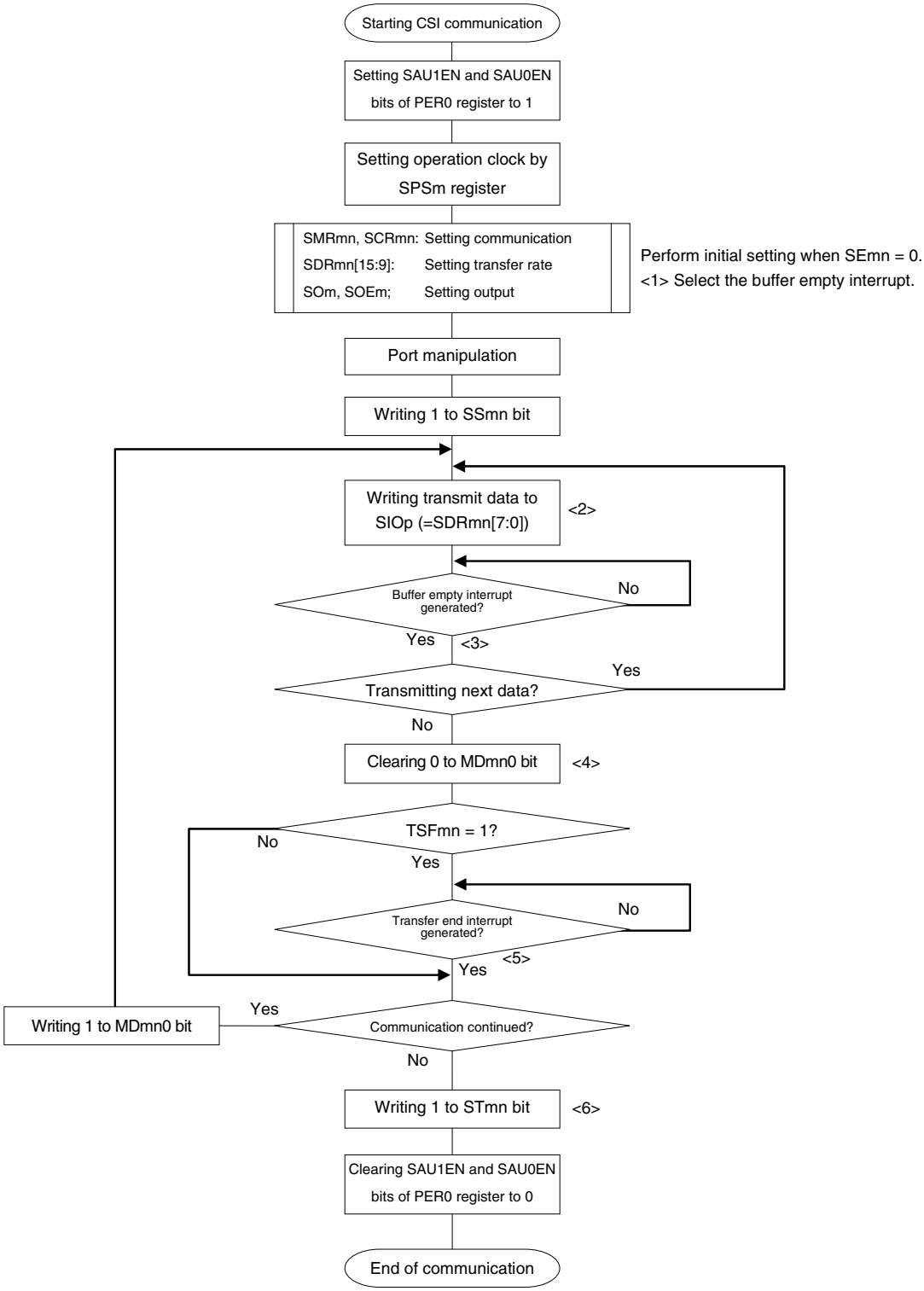
Rewriting SPSm is prohibited when the register is in operation (when SEmn = 1).

SPSm can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of SPSm can be set with an 8-bit memory manipulation instruction with SPSmL.

Reset signal generation clears this register to 0000H.

Figure 12-31. Flowchart of Master Transmission (in Continuous Transmission Mode)



Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 12-30 Timing Chart of Master Transmission (in Continuous Transmission Mode)**.

14.2 Configuration of Multiplier

(1) 16-bit higher multiplication result storage register and 16-bit lower multiplication result storage register (MULOH, MULOL)

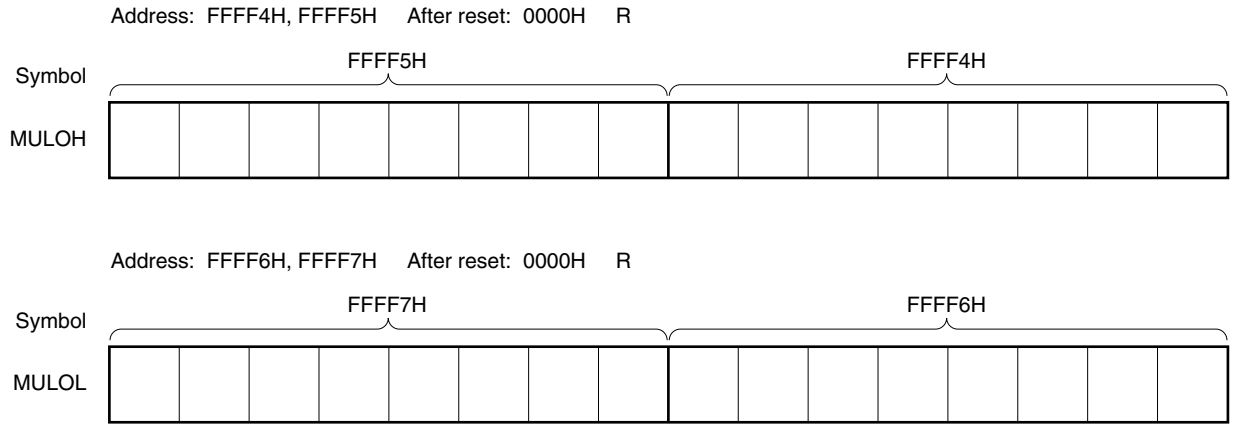
These two registers, MULOH and MULOL, are used to store a 32-bit multiplication result. The higher 16 bits of the multiplication result are stored in MULOH and the lower 16 bits, in MULOL, so that a total of 32 bits of the multiplication result can be stored.

These registers hold the result of multiplication after the lapse of one CPU clock.

MULOH and MULOL can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 14-2. Format of 16-bit higher multiplication result storage register and 16-bit lower multiplication result storage register (MULOH, MULOL)



(2) Multiplication input data registers A, B (MULA, MULB)

These are 16-bit registers that store data for multiplication. The multiplier multiplies the values of MULA and MULB.

MULA and MULB can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 14-3. Format of Multiplication input data registers A, B (MULA, MULB)

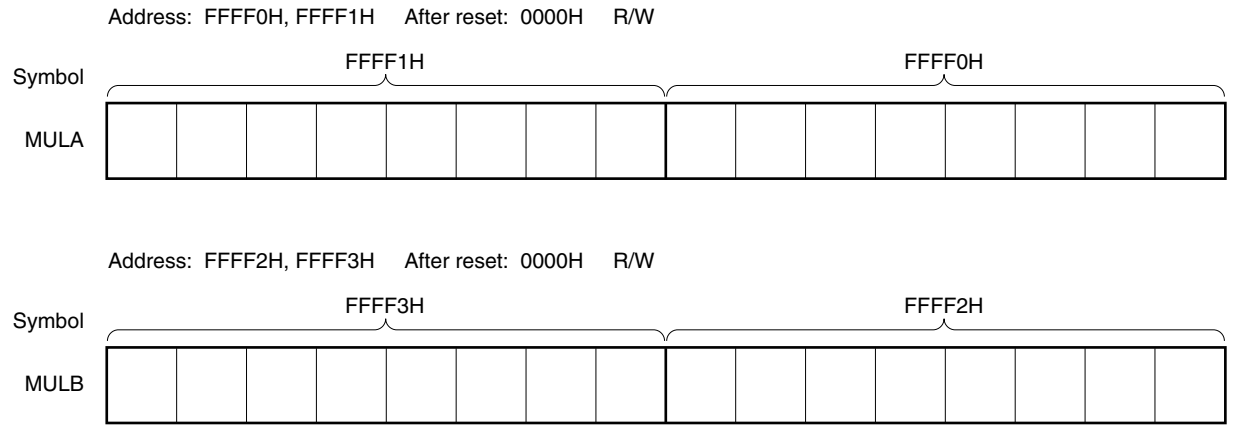
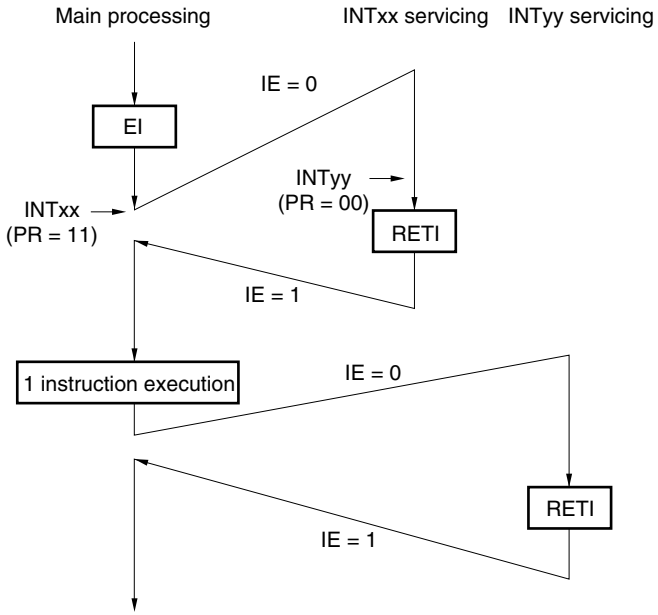


Figure 16-10. Examples of Multiple Interrupt Servicing (2/2)

Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled



Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0
PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

CHAPTER 18 STANDBY FUNCTION

18.1 Standby Function and Configuration

18.1.1 Standby function

The standby function reduces the operating current of the system, and the following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, internal high-speed oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions 1. The STOP mode can be used only when the CPU is operating on the main system clock. The STOP mode cannot be set while the CPU operates with the subsystem clock. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.

2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.

3. The following sequence is recommended for operating current reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

4. It can be selected by the option byte whether the internal low-speed oscillator continues oscillating or stops in the HALT or STOP mode. For details, see CHAPTER 23 OPTION BYTE.

18.1.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

Remark For the registers that start, stop, or select the clock, see **CHAPTER 5 CLOCK GENERATOR**.

(1) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter.

The X1 clock oscillation stabilization time can be checked in the following case,

- If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating.

OSTC can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, WDT, and executing an illegal instruction), the STOP instruction and MSTOP (bit 7 of CSC register) = 1 clear this register to 00H.

Figure 18-1. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFFA2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18

MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18	Oscillation stabilization time status		
									f_X = 10 MHz	f_X = 20 MHz
0	0	0	0	0	0	0	0	$2^8/f_X$ max.	25.6 μs max.	12.8 μs max.
1	0	0	0	0	0	0	0	$2^8/f_X$ min.	25.6 μs min.	12.8 μs min.
1	1	0	0	0	0	0	0	$2^9/f_X$ min.	51.2 μs min.	25.6 μs min.
1	1	1	0	0	0	0	0	$2^{10}/f_X$ min.	102.4 μs min.	51.2 μs min.
1	1	1	1	0	0	0	0	$2^{11}/f_X$ min.	204.8 μs min.	102.4 μs min.
1	1	1	1	1	0	0	0	$2^{13}/f_X$ min.	819.2 μs min.	409.6 μs min.
1	1	1	1	1	1	0	0	$2^{15}/f_X$ min.	3.27 ms min.	1.64 ms min.
1	1	1	1	1	1	1	0	$2^{17}/f_X$ min.	13.11 ms min.	6.55 ms min.
1	1	1	1	1	1	1	1	$2^{18}/f_X$ min.	26.21 ms min.	13.11 ms min.

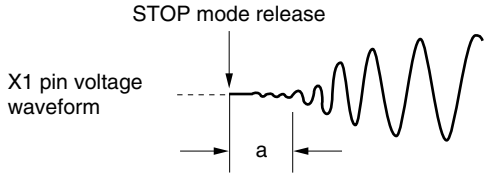
Cautions 1. After the above time has elapsed, the bits are set to 1 in order from MOST8 and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_X: X1 clock oscillation frequency

Figure 21-2. Format of Low-Voltage Detection Register (LVIM)

Address: FFFA9H After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	<2>	<1>	<0>
LVIM	LVION	0	0	0	0	LVISEL	LVIMD	LVIF

LVION[Notes 3, 4]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

LVISEL[Note 3]	Voltage detection selection
0	Detects level of supply voltage (V_{DD})
1	Detects level of input voltage from external input pin (EXLVI)

LVIMD	Low-voltage detection operation mode (interrupt/reset) selection
0	• LVISEL = 0: Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the detection voltage (V_{LVI}) ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$). • LVISEL = 1: Generates an interrupt signal when the input voltage from an external input pin (EXLVI) drops lower than the detection voltage (V_{EXLVI}) (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).
1	• LVISEL = 0: Generates an internal reset signal when the supply voltage (V_{DD}) < detection voltage (V_{LVI}) and releases the reset signal when $V_{DD} \geq V_{LVI}$. • LVISEL = 1: Generates an internal reset signal when the input voltage from an external input pin (EXLVI) < detection voltage (V_{EXLVI}) and releases the reset signal when EXLVI ≥ V_{EXLVI}.

LVIF	Low-voltage detection flag
0	• LVISEL = 0: Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}), or when LVI operation is disabled • LVISEL = 1: Input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI}), or when LVI operation is disabled
1	• LVISEL = 0: Supply voltage (V_{DD}) < detection voltage (V_{LVI}) • LVISEL = 1: Input voltage from external input pin (EXLVI) < detection voltage (V_{EXLVI})

Notes 1. The reset value changes depending on the reset source and the setting of the option byte.
This register is not cleared (00H) by LVI reset.
It is set to “82H” when a reset signal other than LVI is applied if option byte LVIOFF = 0, and to “00H” if option byte LVIOFF = 1.

2. Bit 0 is read-only.

3. LVION, LVIMD, and LVISEL are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

[MEMO]