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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1153agk-gak-ax

RENESAS

User's Manual

78K0R/KF3

16-bit Single-Chip Microcontrollers

μPD78F1152, 78F1152A, 78F1152A(A)
μPD78F1153, 78F1153A, 78F1153A(A)
μPD78F1154, 78F1154A, 78F1154A(A)
μPD78F1155, 78F1155A, 78F1155A(A)
μPD78F1156, 78F1156A, 78F1156A(A)

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1.3 Applications

- Home appliances
  - Laser printer motors
  - Clothes washers
  - Air conditioners
  - Refrigerators
- Home audio systems
- Digital cameras, digital video cameras

1.4 Ordering Information

- **Flash memory version (lead-free products)**

Part Number	Package	Quality Grade
μPD78F1152GC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1152AGC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1153GC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1153AGC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1154GC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1154AGC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1155GC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1155AGC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1156GC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1156AGC-GAD-AX	80-pin plastic LQFP (14 × 14)	Standard
μPD78F1152AGC(A)-GAD-AX	80-pin plastic LQFP (14 × 14)	Special
μPD78F1153AGC(A)-GAD-AX	80-pin plastic LQFP (14 × 14)	Special
μPD78F1154AGC(A)-GAD-AX	80-pin plastic LQFP (14 × 14)	Special
μPD78F1155AGC(A)-GAD-AX	80-pin plastic LQFP (14 × 14)	Special
μPD78F1156AGC(A)-GAD-AX	80-pin plastic LQFP (14 × 14)	Special
μPD78F1152GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1152AGK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1153GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1153AGK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1154GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1154AGK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1155GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1155AGK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1156GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1156AGK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F1152AGK(A)-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Special
μPD78F1153AGK(A)-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Special
μPD78F1154AGK(A)-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Special
μPD78F1155AGK(A)-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Special
μPD78F1156AGK(A)-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	Special

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

(2) Non-port functions (2/3)

Function Name	I/O	Function	After Reset	Alternate Function
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P04/$\overline{SCK10}$
SCL20	I/O	Clock input/output for simplified I^2C	Input port	P142/$\overline{SCK20}$
SDA0	I/O	Serial data I/O for I^2C	Input port	P61
SDA10		Serial data I/O for simplified I^2C	Input port	P03/SI10/RxD1
SDA20		Serial data I/O for simplified I^2C	Input port	P143/SI20/RxD2
SI00	Input	Serial data input to CSI00, CSI01, CSI10, and CSI20	Input port	P11/RxD0
SI01				P44
SI10				P03/RxD1/SDA10
SI20				P143/RxD2/SDA20
SO00	Output	Serial data output from CSI00, CSI01, CSI10, and CSI20	Input port	P12/TxD0
SO01				P45
SO10				P02/TxD1
SO20				P144/TxD2
TI00	Input	External count clock input to 16-bit timer 00	Input port	P00
TI01		External count clock input to 16-bit timer 01		P16/TO01/INTP5
TI02		External count clock input to 16-bit timer 02		P17/TO02
TI03		External count clock input to 16-bit timer 03		P31/TO03/INTP4
TI04		External count clock input to 16-bit timer 04		P42/TO04
TI05		External count clock input to 16-bit timer 05		P05/TO05
TI06		External count clock input to 16-bit timer 06		P06/TO06
TI07		External count clock input to 16-bit timer 07		P145/TO07
TO00	Output	16-bit timer 00 output	Input port	P01
TO01		16-bit timer 01 output		P16/TI01/INTP5
TO02		16-bit timer 02 output		P17/TI02
TO03		16-bit timer 03 output		P31/TI03/INTP4
TO04		16-bit timer 04 output		P42/TI04
TO05		16-bit timer 05 output		P05/TI05
TO06		16-bit timer 06 output		P06/TI06
TO07		16-bit timer 07 output		P145/TI07
TxD0	Output	Serial data output from UART0	Input port	P12/SO00
TxD1	Output	Serial data output from UART1	Input port	P02/SO10
TxD2	Output	Serial data output from UART2	Input port	P144/SO20
TxD3	Output	Serial data output from UART3	Input port	P13
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124

Figure 3-35. Example of ES:[HL + byte], ES:[DE + byte]

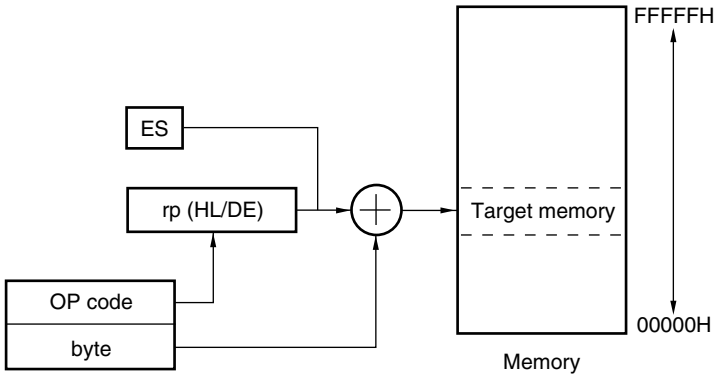


Figure 3-36. Example of ES:word[B], ES:word[C]

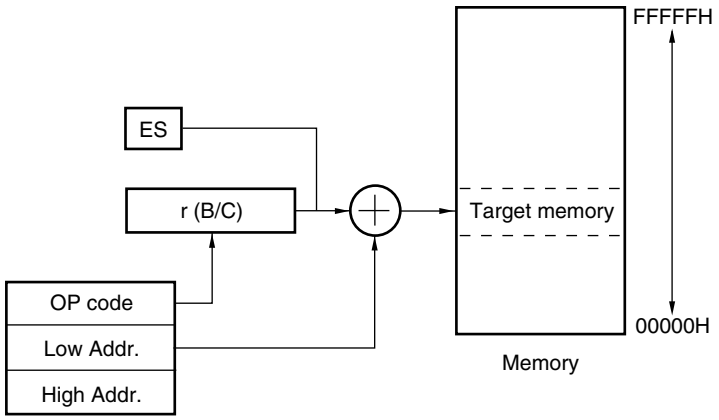


Figure 3-37. Example of ES:word[BC]

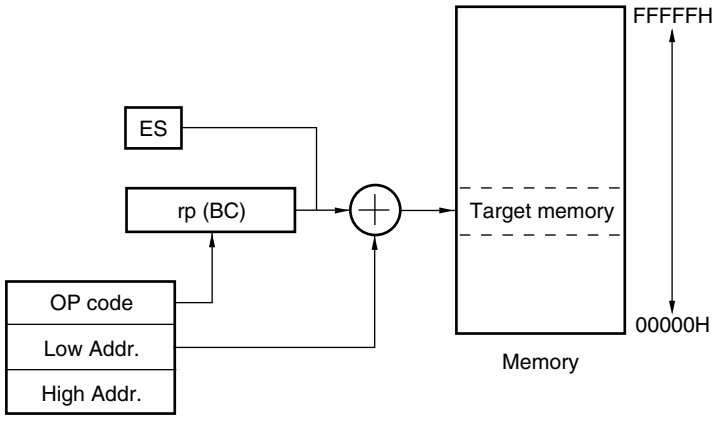


Figure 6-37. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (2/3)

(2) When f_{SUB}/4 is selected as count clock

(a) Timer mode register 0n (TMR0n)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR0n	CKS0n			CCS0n	MASTER0n	STS0n2	STS0n1	STS0n0	CIS0n1	CIS0n0			MD0n3	MD0n2	MD0n1	MD0n0
	1/0	0	0	1	0	0	0	0	1/0	1/0	0	0	0	0	0	1/0

Operation mode of channel n
000B: Interval timer

Setting of operation when counting is started
0: Neither generates INTTM0n nor inverts timer output when counting is started.
1: Generates INTTM0n and inverts timer output when counting is started.

f_{SUB}/4 edge selection
00B: Detects falling edge (counts on f_{SUB}/4 cycles).
01B: Detects rising edge (counts on f_{SUB}/4 cycles).
10B: Detects both edges (counts on f_{SUB}/2 cycles).
11B: Setting prohibited

Start trigger selection
000B: Selects only software start.

Slave/master selection
0: Cleared to 0 when single-operation function is selected.

Count clock selection
1: Selects subsystem clock divided by four (f_{SUB}/4).

Operation clock selection
0: Selects CK00 as operation clock of channel n.
1: Selects CK01 as operation clock of channel n.
f_{CLK} (no division) is selected as selected operation clock by TPS0 register.

(b) Timer clock select register 0 (TPS0)

	Bits 7 to 4, 3 to 0
TPS0	PRS0k3 to PRS0k0
	0000

0000B: Selects f_{CLK} (no division) as operation clock selected by CKS0n of TMR0n register.
k = 0 (bits 0 to 3) when CK00 is selected and k = 1 (bits 4 to 7) when CK01 is selected

(c) Timer input select register 0 (TIS0)

	Bit n
TIS0	TIS0n
	1

1: Selects subsystem clock divided by four (f_{SUB}/4).

(d) Timer output register 0 (TO0)

	Bit n
TO0	TO0n
	1/0

0: Outputs 0 from TO0n.
1: Outputs 1 from TO0n.

Remarks 1. n = 0 to 7, k = 0, 1

2. f_{SUB}: Subsystem clock oscillation frequency

(2) 2.3 V ≤ AV_{REF0} ≤ 5.5 V

A/D Converter Mode Register (ADM)					Conversion Time Selection			Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	
0	0	0	0	1	480/f_{CLK}	Setting prohibited	Setting prohibited	f_{CLK}/12
0	0	1	0	1	320/f_{CLK}		64.0 μs	f_{CLK}/8
0	1	0	0	1	240/f_{CLK}		48.0 μs	f_{CLK}/6
0	1	1	0	1	160/f_{CLK}		32.0 μs	f_{CLK}/4
1	0	0	0	1	120/f_{CLK}	60.0 μs	24.0 μs Note 1	f_{CLK}/3
1	0	1	0	1	80/f_{CLK}	40.0 μs	16.0 μs Note 2	f_{CLK}/2
1	1	1	0	1	40/f_{CLK}	20.0 μs Note 2	Setting prohibited	f_{CLK}
Other than above					Setting prohibited			

Notes 1. This can be set only when 2.7 V ≤ AV_{REF0} ≤ 5.5 V.

2. This can be set only when 4.0 V ≤ AV_{REF0} ≤ 5.5 V.

Cautions 1. Set the conversion times with the following conditions.

- **4.0 V ≤ AV_{REF0} ≤ 5.5 V: f_{AD} = 0.6 to 3.6 MHz**
- **2.7 V ≤ AV_{REF0} < 4.0 V: f_{AD} = 0.6 to 1.8 MHz**
- **2.3 V ≤ AV_{REF0} < 2.7 V: f_{AD} = 0.6 to 1.44 MHz**

2. When rewriting FR2 to FR0, LV1, and LV0 to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.

3. Change LV1 and LV0 from the default value, when 2.3 V ≤ AV_{REF0} < 2.7 V.

4. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

Figure 12-96. Flowchart of Address Field Transmission

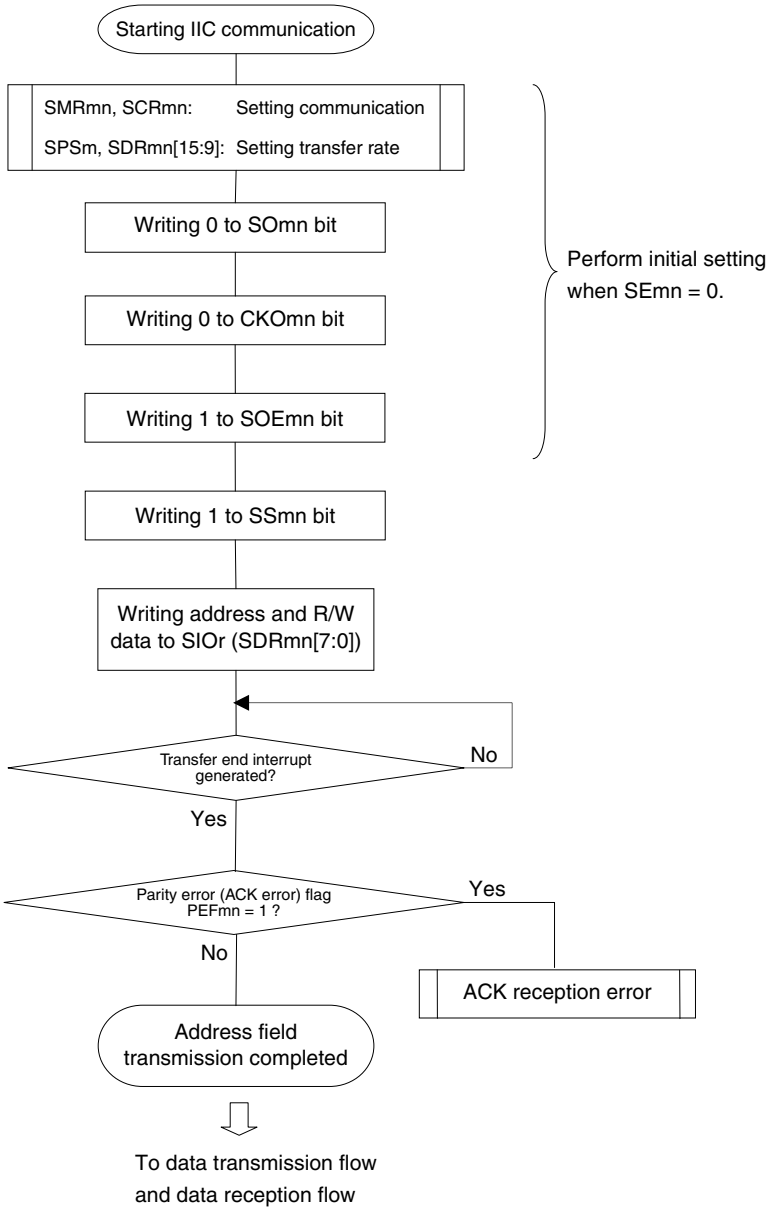


Figure 13-6. Format of IIC Control Register 0 (IICC0) (1/4)

Address: FFF52H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICC0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

IICE0	I^2C operation enable
0	Stop operation. Reset IIC status register 0 (IICS0)[Note 1]. Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCL0 and SDA0 lines are at high level.	
Condition for clearing (IICE0 = 0)	Condition for setting (IICE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL0[Note 2]	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCL0 and SDA0 lines are set to high impedance. The following flags of IIC control register 0 (IICC0) and IIC status register 0 (IICS0) are cleared to 0. • STT0 • SPT0 • MSTS0 • EXC0 • COI0 • TRC0 • ACKD0 • STD0
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL0 = 0)	Condition for setting (LREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WREL0[Note 2]	Wait cancellation
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.
When WREL0 is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC0 = 1), the SDA0 line goes into the high impedance state (TRC0 = 0).	
Condition for clearing (WREL0 = 0)	Condition for setting (WREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

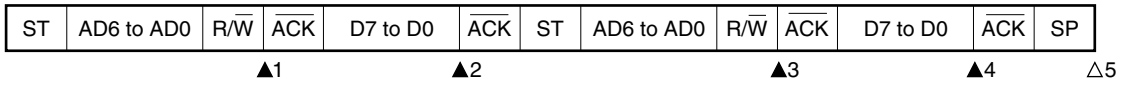
Notes 1. The IICS0 register, the STCF and IICBSY bits of the IICF0 register, and the CLD0 and DAD0 bits of the IICCL0 register are reset.

2. The signal of this bit is invalid while IICE0 is 0.

Caution The start condition is detected immediately after I^2C is enabled to operate (IICE0 = 1) while the SCL0 line is at high level and the SDA0 line is at low level. Immediately after enabling I^2C to operate (IICE0 = 1), set LREL0 (1) by using a 1-bit memory manipulation instruction.

(c) Start ~ Code ~ Data ~ Start ~ Code ~ Data ~ Stop

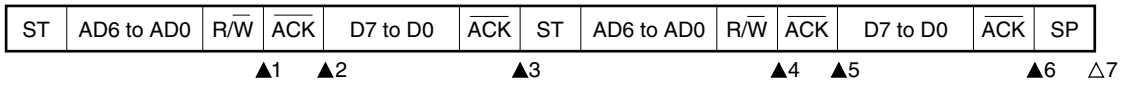
(i) When WTIM0 = 0 (after restart, extension code reception)



▲1: IICS0 = 0010×010B
▲2: IICS0 = 0010×000B
▲3: IICS0 = 0010×010B
▲4: IICS0 = 0010×000B
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, extension code reception)



▲1: IICS0 = 0010×010B
▲2: IICS0 = 0010×110B
▲3: IICS0 = 0010××00B
▲4: IICS0 = 0010×010B
▲5: IICS0 = 0010×110B
▲6: IICS0 = 0010××00B
△7: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

16.4 Interrupt Servicing Operations

16.4.1 Maskable interrupt acknowledgment

A maskable interrupt becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request.

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 16-4 below.

For the interrupt request acknowledgment timing, see **Figures 16-8** and **16-9**.

Table 16-4. Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
Servicing time	9 clocks	14 clocks

Note If an interrupt request is generated just before the RET instruction, the wait time becomes longer.

Remark 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

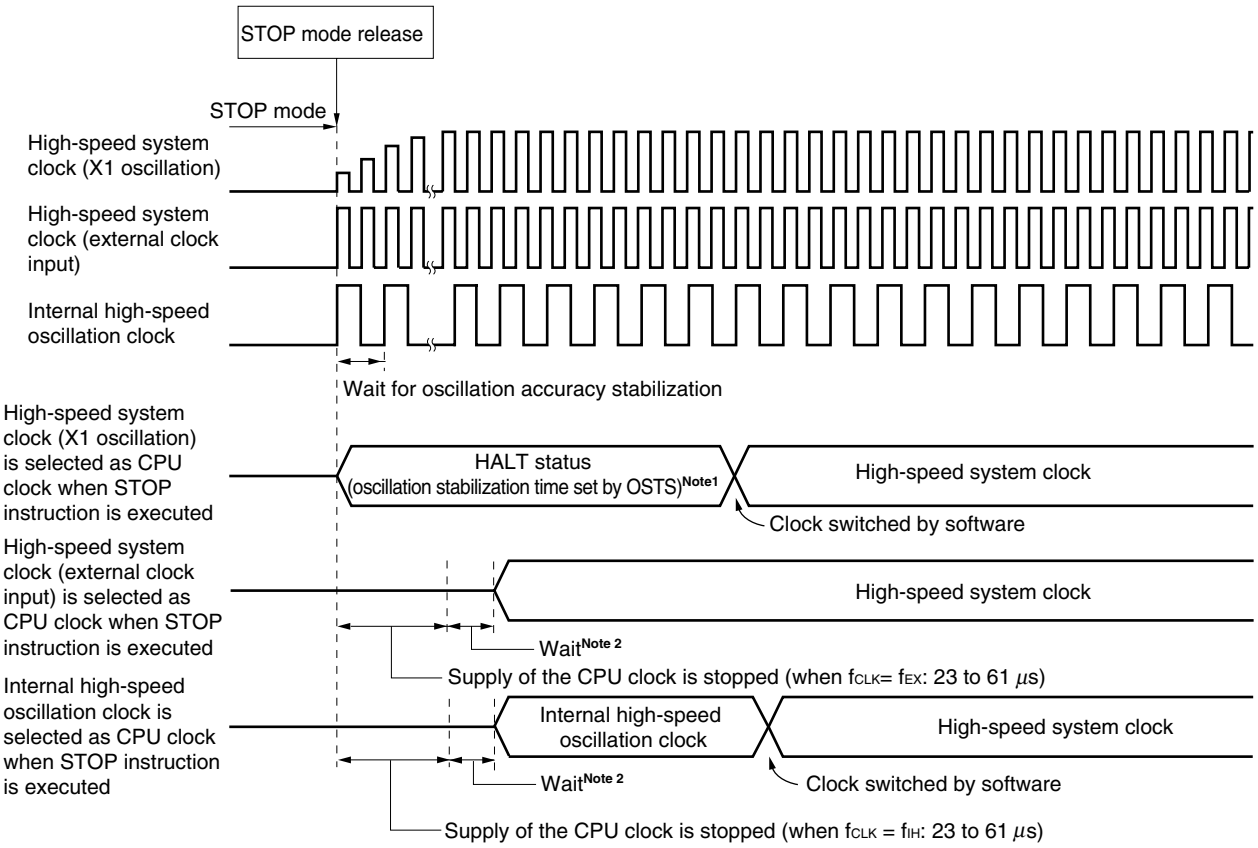
Figure 16-7 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP1 and ISP0 flags. The vector table data determined for each interrupt request is the loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

(2) STOP mode release

Figure 18-5. Operation Timing When STOP Mode Is Released (Release by Unmasked Interrupt Request)



Notes 1. When the oscillation stabilization time set by OSTS is equal to or shorter than 61 μs, the HALT status is retained to a maximum of "61μs + wait time."

2. The wait time is as follows:

- When vectored interrupt servicing is carried out: 10 to 12 clocks
- When vectored interrupt servicing is not carried out: 5 or 6 clocks

Remark f_{EX}: External main system clock frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

The STOP mode can be released by the following two sources.

Table 24-1. Wiring Between 78K0R/KF3 and Dedicated Flash Memory Programmer

Pin Configuration of Dedicated Flash Memory Programmer			Pin Name	Pin No.
Signal Name	I/O	Pin Function		
SI/RxD Notes 1, 2	Input	Receive signal	TOOL0/P40	9
SO/TxD Note 2	Output	Transmit signal		
SCK	Output	Transfer clock	–	–
CLK	Output	Clock output	–	–
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	10
FLMD0	Output	Mode signal	FLMD0	13
V_{DD}	I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	19
			EV_{DD}	20
			AV_{REF0}	59
			AV_{REF1}	56
GND	–	Ground	V_{SS}	17
			EV_{SS}	18
			AV_{SS}	60

Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

DC Characteristics (8/12)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Square wave input		7.0	12.2	mA
				Resonator connection		7.3	12.5	mA
			f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Square wave input		7.0	12.2	mA
				Resonator connection		7.3	12.5	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 5.0 V	Square wave input		3.8	6.2	mA
				Resonator connection		3.9	6.3	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		3.8	6.2	mA
				Resonator connection		3.9	6.3	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 3.0 V	Normal current mode, Square wave input		2.1	3.0	mA
				Normal current mode, Resonator connection		2.2	3.1	mA
				Low consumption current mode Note 4, Square wave input		1.5	2.1	mA
				Low consumption current mode Note 4, Resonator connection		1.5	2.1	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 2.0 V	Normal current mode, Square wave input		1.4	2.1	mA
				Normal current mode, Resonator connection		1.4	2.1	mA
				Low consumption current mode Note 4, Square wave input		1.4	2.0	mA
				Low consumption current mode Note 4, Resonator connection		1.4	2.0	mA
			f_{IH} = 8 MHz Note 5	V_{DD} = 5.0 V		3.1	5.0	mA
				V_{DD} = 3.0 V		3.1	5.0	mA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, AV_{REF0}, and AV_{REF1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. When internal high-speed oscillator and subsystem clock are stopped.

3. When AMPH (bit 0 of clock operation mode control register (CMC)) = 0 and FSEL (bit 0 of operation speed mode control register (OSMC)) = 0.

4. When the RMC register is set to 5AH.

5. When high-speed system clock and subsystem clock are stopped. When FSEL (bit 0 of operation speed mode control register (OSMC)) = 0 is set.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

f_{IH}: Internal high-speed oscillation clock frequency

2. For details on the normal current mode and low consumption current mode according to the regulator output voltage, refer to **CHAPTER 22 REGULATOR**.

<R> **3.** Temperature condition of the TYP. value is T_A = 25°C

DC Characteristics (4/12)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	P01, P02, P12, P13, P15, P41, P45, P52 to P55, P64 to P67, P90, P121 to P124, P144		0		$0.3V_{DD}$	V
	V_{IL2}	P00, P03 to P06, P10, P11, P14, P16, P17, P30, P31, P40, P42 to P44, P46, P47, P50, P51, P70 to P77, P120, P140 to P143, P145, EXCLK, $\overline{\text{RESET}}$	Normal input buffer	0		$0.2V_{DD}$	V
	V_{IL3}	P03, P04, P43, P44, P142, P143	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 2.7 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.8 V ≤ V_{DD} < 2.7 V	0		0.2	V
	V_{IL4}	P20 to P27	2.7 V ≤ AV_{REF0} ≤ V_{DD}	0		$0.3AV_{REF0}$	V
			AV_{REF0} = V_{DD} < 2.7 V				
	V_{IL5}	P110, P111	2.7 V ≤ AV_{REF1} ≤ V_{DD}	0		$0.3AV_{REF1}$	V
			AV_{REF1} = V_{DD} < 2.7 V				
	V_{IL6}	P60 to P63		0		$0.3V_{DD}$	V
	V_{IL7}	FLMD0 [Note]		0		$0.1V_{DD}$	V

Note When disabling writing of the flash memory, connect the FLMD0 pin processing directly to V_{SS}, and maintain a voltage less than $0.1V_{DD}$.

Caution For P122/EXCLK, the value of V_{IH} and V_{IL} differs according to the input port mode or external clock mode.
Make sure to satisfy the DC characteristics of EXCLK in external clock input mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

A.4.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This is a flash memory programmer dedicated to microcontrollers with on-chip flash memory. It is available also as on-chip debug emulator which serves to debug hardware and software when developing application systems using the 78K0R. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. To use 78K0R/KF3, use USB interface cable and 16-pin connection cable.

Remark Download the software for operating the QB-MINI2 from the download site for MINICUBE2 (http://www.necel.com/micro/en/development/asia/minicube2/minicube2.html).

A.5 Debugging Tools (Hardware)

A.5.1 When using in-circuit emulator QB-78K0RKX3

QB-78K0RKX3 In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0R/Kx3. It supports to the integrated debugger (ID78K0R-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-144-CA-01 Check pin adapter	This check pin adapter is used in waveform monitoring using the oscilloscope, etc.
QB-144-EP-02S Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
QB-80GC-EA-06T, QB-80GK-EA-06T Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector. • QB-80GC-EA-06T: 80-pin plastic LQFP (GC-GAD type) • QB-80GK-EA-06T: 80-pin plastic LQFP (GK-GAK type)
QB-80GC-YS-01T, QB-80GK-YS-01T Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator. • QB-80GC-YS-01T: 80-pin plastic LQFP (GC-GAD type) • QB-80GK-YS-01T: 80-pin plastic LQFP (GK-GAK type)
QB-80GC-YQ-01T, QB-80GK-YQ-01T YQ connector	This YQ connector is used to connect the target connector and exchange adapter. • QB-80GC-YQ-01T: 80-pin plastic LQFP (GC-GAD type) • QB-80GK-YQ-01T: 80-pin plastic LQFP (GK-GAK type)
QB-80GC-HQ-01T, QB-80GK-HQ-01T Mount adapter	This mount adapter is used to mount the target device with socket. • QB-80GC-HQ-01T: 80-pin plastic LQFP (GC-GAD type) • QB-80GK-HQ-01T: 80-pin plastic LQFP (GK-GAK type)
QB-80GC-NQ-01T, QB-80GK-NQ-01T Target connector	This target connector is used to mount on the target system. • QB-80GC-NQ-01T: 80-pin plastic LQFP (GC-GAD type) • QB-80GK-NQ-01T: 80-pin plastic LQFP (GK-GAK type)

Remarks 1. The QB-78K0RKX3 is supplied with a power supply unit and USB interface cable. As control software, integrated debugger ID78K0R-QB and on-chip debug emulator with programming function QB-MINI2 are supplied.

2. The packed contents differ depending on the part number, as follows.

Packed Contents / Part Number	In-Circuit Emulator	Emulation Probe	Exchange Adapter	YQ Connector	Target Connector
QB-78K0RKX3-ZZZ	QB-78K0RKX3	None			
QB-78K0RKX3-T80GC		QB-144-EP-02S	QB-80GC-EA-06T	QB-80GC-YQ-01T	QB-80GC-NQ-01T
QB-78K0RKX3-T80GK			QB-80GK-EA-06T	QB-80GK-YQ-01T	QB-80GK-NQ-01T

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 6	Soft	Operation of timer array unit as independent channel	Input pulse interval measurement	The TI0n pin input is sampled using the operating clock selected with the CKS0n bit of the TMR0n register, so an error equal to the number of operating clocks occurs.	p.244 ☐
			Input signal high-/low-level width measurement	The TI0n pin input is sampled using the operating clock selected with the CKS0n bit of the TMR0n register, so an error equal to the number of operating clocks occurs.	p.248 ☐
		Operation of plural channels of timer array unit	PWM function	To rewrite both TDR0n of the master channel and TDR0m of the slave channel, a write access is necessary two times. The timing at which the values of TDR0n and TDR0m are loaded to TCR0n and TRC0m is upon occurrence of INTTM0n of the master channel. Thus, when rewriting is performed split before and after occurrence of INTTM0n of the master channel, the TO0m pin cannot output the expected waveform. To rewrite both TDR0n of the master and TDR0m of the slave, therefore, be sure to write both the registers immediately after INTTM0n is generated from the master channel.	p.252 ☐
			One-shot pulse output function	The timing of loading of TDR0n of the master channel is different from that of TDR0m of the slave channel. If TDR0n and TDR0m are rewritten during operation, therefore, an illegal waveform is output. Rewrite the TDR0n after INTTM0n is generated and the TDR0m after INTTM0m is generated.	p.259 ☐
			Multiple PWM output function	To rewrite both TDR0n of the master channel and TDR0p of the slave channel 1, write access is necessary at least twice. Since the values of TDR0n and TDR0p are loaded to TCR0n and TCR0p after INTTM0n is generated from the master channel, if rewriting is performed separately before and after generation of INTTM0n from the master channel, the TO0p pin cannot output the expected waveform. To rewrite both TDR0n of the master and TDR0p of the slave, be sure to rewrite both the registers immediately after INTTM0n is generated from the master channel. (This applies also to TDR0q of the slave channel 2.)	p.266 ☐
Chapter 7	Soft	Real-time counter	PER0: Peripheral enable register 0	When using the real-time counter, first set RTCEN to 1, while oscillation of the subsystem clock (f_{SUB}) is stable. If RTCEN = 0, writing to a control register of the real-time counter is ignored, and, even if the register is read, only the default value is read.	p.276 ☐
				Be sure to clear bit 1 of the PER0 register to 0.	p.276 ☐
			RTCC0: Real-time counter control register 0	If RCLOE0 and RCLOE1 are changed when RTCE = 1, glitches may occur in the 32.768 kHz and 1 Hz output signals.	p.277 ☐
			RTCC1: Real-time counter control register 1	The RIFG and WAFG flags may be cleared when the RTCC1 register is written by using a 1-bit manipulation instruction. Use, therefore, an 8-bit manipulation instruction in order to write to the RTCC1 register. To prevent the RIFG and WAFG flags from being cleared during writing, disable writing by setting “1” to the corresponding bit. When the value may be rewritten because the RIFG and WAFG flags are not being used, the RTCC1 register may be written by using a 1-bit manipulation instruction.	p.279 ☐
			RTCC2: Real-time counter control register 2	Change ICT2, ICT1, and ICT0 when RINTE = 0.	p.280 ☐
				When the output from RTCDIV pin is stopped, the output continues after a maximum of two clocks of f_{XT} and enters the low level. While 512 Hz is output, and when the output is stopped immediately after entering the high level, a pulse of at least one clock width of f_{XT} may be generated.	p.280 ☐
				After the real-time counter starts operating, the output width of the RTCDIV pin may be shorter than as set during the first interval period.	p.280 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 10	Soft	A/D converter	A/D conversion time selection (2.3 V ≤ AV_{REF0} ≤ 5.5 V)	Set the conversion times with the following conditions. • 4.0 V ≤ AV_{REF0} ≤ 5.5 V: f_{AD} = 0.6 to 3.6 MHz • 2.7 V ≤ AV_{REF0} < 4.0 V: f_{AD} = 0.6 to 1.8 MHz • 2.3 V ≤ AV_{REF0} < 2.7 V: f_{AD} = 0.6 to 1.44 MHz	p.318 ☐
				When rewriting FR2 to FR0, LV1, and LV0 to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.	p.318 ☐
				Change LV1 and LV0 from the default value, when 2.3 V ≤ AV_{REF0} < 2.7 V.	p.318 ☐
				The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.	p.318 ☐
			ADCR: 10-bit A/D conversion result register	When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using timing other than the above may cause an incorrect conversion result to be read.	p.320 ☐
			ADCRH: 8-bit A/D conversion result register	When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using timing other than the above may cause an incorrect conversion result to be read.	p.320 ☐
			ADS: Analog input channel specification register	Be sure to clear bits 3 to 6 to “0”.	p.321 ☐
				Set a channel to be used for A/D conversion in the input mode by using port mode registers 2 (PM2).	p.321 ☐
				Do not set the pin that is set by ADPC as digital I/O by ADS.	p.321 ☐
			ADPC: A/D port configuration register	Set a channel to be used for A/D conversion in the input mode by using port mode registers 2 (PM2).	p.322 ☐
				Do not set the pin that is set by ADPC as digital I/O by ADS.	p.322 ☐
				When all pins of ANI0/P20 to ANI7/P27 are used as digital I/O (D), ADPC4 to ADPC0 can be set by either 01000 or 10000.	p.322 ☐
				P20/ANI0 to P27/ANI7 are set as analog inputs in the order of P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 as analog inputs, start designing from P27/ANI7.	p.322 ☐
			PM2: Port mode registers 2	If a pin is set as an analog input port, not the pin level but “0” is always read.	p.323 ☐
			Basic operations of A/D converter	Make sure the period of <2> to <6> is 1 μs or more.	p.324 ☐
			A/D conversion operation	Make sure the period of <2> to <6> is 1 μs or more.	p.328 ☐
				<2> may be done between <3> and <5>.	p.328 ☐
				The period from <7> to <10> differs from the conversion time set using bits 5 to 1 (FR2 to FR0, LV1, LV0) of ADM. The period from <9> to <10> is the conversion time set using FR2 to FR0, LV1, and LV0.	p.328 ☐
			Temperature sensor function	The temperature sensor cannot be used when low current consumption mode is set (RMC = 5AH) or when the internal high-speed oscillator has been stopped (HIOSTOP = 1 (bit 0 of CSC register)). The temperature sensor can operate as long as the internal high-speed oscillator operates (HIOSTOP = 0), even if it is not selected as the CPU/peripheral hardware clock source.	p.329 ☐
			Registers used by temperature sensors	Setting of the A/D port configuration register (ADPC), port mode register 2 (PM2) and port register 2 (P2) is not required when using the temperature sensor. There is no problem if the pin function is set as digital I/O.	p.330 ☐
				Set the conversion times so as to satisfy the following condition. f_{AD} = 0.6 to 1.8 MHz	p.330 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 11	Soft	D/A converter	Reducing power consumption in STOP mode	Because the D/A converter stops operation in the STOP mode, the ANO0 and ANO1 pins go into a high impedance state, and the power consumption can be reduced. In the standby modes other than the STOP mode, however, the operation continues. To lower the power consumption, therefore, clear the DACEn bit of the DAM register to 0 (D/A conversion stop).	p.351 ☐
	Hard		Output impedance of D/A converter	Since the output impedance of the D/A converter is high, the current cannot be obtained from the ANOn pin (n = 0, 1). When the input impedance of the load is low, insert a follower amplifier between the load and ANOn pin keeping the wiring length as short as possible (for high impedance). If the wiring becomes too long, take necessary actions such as surrounding with a ground pattern.	p.351 ☐
Chapter 12	Soft	Configuration of serial array unit	SDRmn: Lower 8 bits of the serial data register mn	Be sure to clear bit 8 to “0”.	p.359 ☐
		Registers controlling serial array unit	PER0: Peripheral enable register 0	When setting serial array unit m, be sure to set SAUmEN to 1 first. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read (except for input switch control register (ISC), noise filter enable register (NFEN0), port input mode registers (PIM0, PIM4, PIM14), port output mode registers (POM0, POM4, POM14), port mode registers (PM0, PM1, PM4, PM14), and port registers (P0, P1, P4, P14)).	p.361 ☐
				After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	p.361 ☐
				Be sure to clear bit 1 of the PER0 register to 0.	p.361 ☐
			SPSm: Serial clock select register m	Be sure to clear bits 15 to 8 to “0”.	p.362 ☐
				After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	p.362 ☐
			SMRmn: Serial mode register mn	Be sure to clear bits 13 to 9, 7, 4, and 3 to “0”. Be sure to set bit 5 to “1”.	p.363 ☐
			SCRmn: Serial communication operation setting register mn	Be sure to clear bits 3, 6, and 11 to “0”. Be sure to set bit 2 to “1”.	pp.365 to 367 ☐
			SDRmn: Higher 7 bits of the serial data register mn	Be sure to clear bit 8 to “0”.	p.368 ☐
				Setting SDRmn[15:9] = (0000000B, 0000001B) is prohibited when UART is used.	p.368 ☐
				Setting SDRmn[15:9] = 0000000B is prohibited when simplified I^2C is used. Set SDRmn[15:9] to 0000001B or greater.	p.368 ☐
				Do not write eight bits to the lower eight bits if operation is stopped (SEmn = 0). (If these bits are written to, the higher seven bits are cleared to 0.)	p.368 ☐
			SIRmn: Serial flag clear trigger register mn	Be sure to clear bits 15 to 3 to “0”.	p.371 ☐
			SSm: Serial channel start register m	Be sure to clear bits 15 to 4 to “0”.	p.373 ☐
			STm: Serial channel stop register m	Be sure to clear bits 15 to 4 to “0”.	p.374 ☐

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Edition	Description	Chapter
3rd edition	**DC characteristics** • Change of Condition and Note 1 in Output current, high (I_{OH1}) • Change of Condition and Note 2 in Output current, low (I_{OL1}) • Change of Condition of Input voltage, high (V_{IH2}) • Change of Condition of Input voltage, low (V_{IL2}) • Change of Condition of Output voltage, low (V_{OL1}) • Addition of Supply current • Addition of Watchdog Timer operating current (I_{WDT}) • Addition of A/D Converter operating current (I_{ADC}) • Addition of D/A Converter operating current(I_{DAC}) • Addition of DMA Controller operating current (I_{DMA}) • Addition of LVI operating current (I_{LVI})	CHAPTER 28 ELECTRICAL SPECIFICATIONS (TARGET)
	Change of MIN. value of Conversion time (t_{CONV})of **A/D Converter Characteristics**	
	Addition of **POC Circuit Characteristics**	
	Addition of **Supply Voltage Rise Time**	
	Addition of **LVI Circuit Characteristics**	
	Addition of **Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics**	
	Revision of chapter	APPENDIX A DEVELOPMENT TOOLS
4th edition	Deletion of target from the capacitance value of the capacitor connected to the REGC pin	Throughout
	Change of description in **2.2.18 REGC**	CHAPTER 2 PIN FUNCTIONS
	Modification of P60 to P64, P110 and P111 in **Table 2-2 Connection of Unused Pins**	
	Modification of 12-D to 12-G in **Figure 2-1 Pin I/O Circuit List (2/2)**	
	Addition (address change) of the BCDADJ register to **Table 3-6 Extended SFR (2nd SFR) List (1/5)**	CHAPTER 3 CPU ARCHITECTURE
	Change of **Figure 4-6 Block Diagram of P05 and P06**	CHAPTER 4 PORT FUNCTIONS
	Change of **Figure 4-28 Block Diagram of P110 and P111**	
	Change of **Figure 4-42 Bit Manipulation Instruction (P10)**	
	Change of **Caution 2** in **Figure 5-6 Format of System Clock Control Register (CKC)**	CHAPTER 5 CLOCK GENERATOR
	Change of description in **5.3 (8) Internal high-speed oscillator trimming register (HIOTRM)** and addition of **Caution**	
	Change of **Figure 5-9 Format of Internal High-Speed Oscillator Trimming Register (HIOTRM)** and addition of **Caution**	
	Change of **Figure 5-13 Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Stopped Is Set (Option Byte: LVIOFF = 1))**	
	Addition of **Note** to **Figure 6-5 Format of Timer Clock Select Register 0 (TPS0)**	CHAPTER 6 TIMER ARRAY UNIT
	Change of **Table 6-3 OVF Bit Operation and Set/Clear Conditions in Each Operation Mode** and addition of **Remark**	
	Addition of **Caution 2** to **Figure 6-18 Format of Timer Output Register 0 (TO0)**	

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Edition	Description	Chapter
7th edition	Change of **Figure 12-93 Timing Chart of Data Transmission**	CHAPTER 12 SERIAL ARRAY UNIT
	Addition of **Note** to **12.7.3 Data reception**	
	Change of **Figure 12-96 Timing Chart of Data Reception**	
	Change of **Figure 12-97 Flowchart of Data Reception** and change of **Caution**	
	Change of **Figure 12-98 Timing Chart of Stop Condition Generation**	
	Change of **Note 2** in **Table 12-4 Selection of Operation Clock**	
	Change of **Cautions 1** in **Figure 13-5. Format of Peripheral Enable Register 0 (PER0)**	CHAPTER 13 SERIAL INTERFACE IIC0
	Change of **Note** in **Figure 13-6 Format of IIC Control Register 0 (IICC0)**	
	Change of **Table 13-2 Selection Clock Setting**	
	Change of **Table 13-3 Selection Clock Setting**	
	Change of **Table 13-5 Extension Code Bit Definitions**	
	Change of **Figure 13-24 Master Operation in Single-Master System**	
	Change of **Figure 13-25 Master Operation in Multi-Master System**	
	Change of **Figure 13-26 Slave Operation Flowchart**	
	Change of **Figures 13-28** and **13-29**	
	Change of **Figure 15-5 Format of DMA Operation Control Register n (DRCn)**	CHAPTER 15 DMA CONTROLLER
	Addition of **Note** to **Table 15-2 Response Time of DMA Transfer**	
	Change of description in **16.2 Interrupt Sources and Configuration**	CHAPTER 16 INTERRUPT FUNCTIONS
	Change of **Table 16-1 Interrupt Source List**	
	Change of **Cautions 2** in **17.3 (1) Key return mode register (KRM)**	CHAPTER 17 KEY INTERRUPT FUNCTION
	Change of **Note** in **Figure 18-3 HALT Mode Release by Interrupt Request Generation**	CHAPTER 18 STANDBY FUNCTION
	Change of **Figure 18-5 Operation Timing When STOP Mode Is Released (Release by Unmasked Interrupt Request)**	
	Addition of **Note** to **Figure 18-6 STOP Mode Release by Interrupt Request Generation**	
	Change of **Table 19-1. Operation Statuses During Reset Period**	CHAPTER 19 RESET FUNCTION
	Deletion of **Note** in **20.1 Functions of Power-on-Clear Circuit**	CHAPTER 20 POWER-ON-CLEAR CIRCUIT
	Deletion of **Note** in **20.3 Operation of Power-on-Clear Circuit**	
	Deletion of **Note 6** in **(1) When LVI is OFF upon power application (option byte: LVIOFF = 1)** in **Figure 20-2 Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector**	
	Deletion of **Note 3** in **(2) When LVI is ON upon power application (option byte: LVIOFF = 0)** in **Figure 20-2 Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector**	
	Deletion of **Note** in **21.1 Functions of Low-Voltage Detector**	CHAPTER 21 LOW-VOLTAGE DETECTOR
	Deletion of **Note 2** in **Figure 21-3 Format of Low-Voltage Detection Level Select Register (LVIS)**	
	Deletion of **Note** in **21.4 Operation of Low-Voltage Detector**	